PC CARD STANDARD

Volume 1

Overview and Glossary

PCMCIA
JEITA

PCMCIA (Personal Computer Memory Card International Association)
2635 North First Street, Suite 209
San Jose, CA 95134 USA
+1-408-433-2273
+1-408-433-9558 (Fax)
http://www.pcmcia.org

JEITA (Japan Electronics and Information Technology Industries Association)
Mitsui Kaijo Bldg. Annex 11
Kanda Surugadai 3-chome
Chiyoda-ku, Tokyo 101-0062
JAPAN
+81-3-3518-6426
+81-3-3295-8724 (Fax)
http://www.jeita.or.jp

Cover Design: Greg Barr

Document No. 0401-01-1500

First Printing, April 2001

CONTENTS

1. INTRODUCTION

This Overview describes the Personal Computer Memory Card International Association (PCMCIA) and the Japan Electronics and Information Technology Industries Association (JEITA), formerly known as JEIDA, PC Card™ Standard that is the result of countless hours of effort by the members of JEITA and PCMCIA. PCMCIA and JEITA are grateful for and acknowledge the dedicated efforts of the PCMCIA and JEITA staff and volunteer members in the creation and production of this Standard.

1.1 PC Card Standard Overview

The Personal Computer Memory Card International Association has an international membership comprising hundreds of member companies from all disciplines: computer manufacturers, semiconductor companies, peripheral vendors, software developers, and more. The Japan Electronics and Information Technology Industries Association was established in 1958 as a non-profit organization interested in contributing to Japan's economic prosperity by stimulating development in the electronics industry. PCMCIA and JEITA have developed a standard for a credit card-sized adapter, called a 'PC Card' that does for notebook and other portable computers what the AT bus did for desktop PCs — provide universal, non-proprietary expansion capability.

The ***Physical Specification*** defines a 68-pin interface between the peripheral card and the PC Card 'socket' into which it gets inserted. It also defines two standard form factors, full-size and Small PC Cards, each in three thicknesses, called Type I, Type II and Type III. Type I, the smallest form factor, often used for memory cards, measures 3.3 mm in thickness. Type II, available for those peripherals requiring taller components such as LAN cards and modems, measures 5 mm thick. Type III is the tallest form factor and measures 10.5 mm thick. Type III PC Cards can support small rotating disks and other tall components. Smaller size cards can always fit into larger sockets but the reverse is not true.

The ***Electrical Specification*** defines three basic classes of PC Cards: 16-bit PC Cards, 32-bit CardBus PC Cards, and CardBay™ PC Cards. Defined are characteristics of each interface including power, signaling, configuration, and timing requirements. Also, the ***PC Card Host System Specification*** describes host-side power management and a thermal ratings system.

In addition to specifying electrical and physical requirements, the ***PC Card Standard*** has also defined a software architecture to provide "plug and play" capability across the widest possible range of products. The ***Socket Services Specification*** defines a BIOS level interface that masks the hardware implementation from card vendors' drivers. It identifies how many sockets are in the host and when a card is inserted or removed from a socket. It prevents the card driver from having to talk directly to a specific chip. The ***Card Services Specification*** defines an Application Programming Interface that interfaces to Socket Services and automatically provides management of system resources, such as interrupt assignments and memory windows, for cards as they become active in the system. Also, the ***Metaformat Specification*** defines the structure and contents of card description information called the Card Information Structure.

The ***PC Card Standard*** also includes three application specific specifications. The ***PC Card ATA Specification*** defines the operation of mass storage devices using the ANSI ATA Interface for Disk Drives in the PC Card environment. The ***Media Storage Formats Specification*** defines how data are to be formatted on some PC Card storage devices. The ***XIP Specification*** defines a method to directly execute applications from ROM without loading the image into RAM.

Also included is a set of ***Guidelines*** intended to assist developers with implementation examples along with further explanations of the ***PC Card Standard***.

1.2 History

1.2.1 History of the PC Card Standard

In 1985, the standardizing activity of PC Card Technology began with the Japan Electronic Industry Development Association (JEIDA). The organization was formed to promote memory cards, personal computers and other portable information products, and by 1990, JEIDA had released four specifications.

The Personal Computer Memory Card International Association (PCMCIA) was founded in 1989 by a small group of companies that wanted to standardize memory cards for the classic reasons behind standardization — multiple sources, lower and shared risks, and larger markets. At that time a company called Poqet Computer had designed a computer that used only memory cards as removable storage. Poqet needed software application developers to put their products on memory cards. At the same time there were ten different types of memory cards sold by different manufacturers and no real effort at standardizing them.

An initial group of about 25 companies met in San Jose, California and agreed on the need for memory card standardization. This was the birth of PCMCIA. From the beginning, there have been two primary committees within PCMCIA—the Technical and Marketing committees. These committees have worked together to develop the PC Card standards based not only on what was technologically feasible but also on what the market demanded. These two committees quickly recognized that the same slot in a host system and the same form factor card could be used for I/O capabilities such as fax/modem in addition to memory cards.

The ability to put I/O capabilities on a card soon became the main attraction for the adoption of the technology in the rapidly expanding mobile computing market. The addition of a PC Card slot would allow mobile computers to have an easily accessible bus expansion capability. PCMCIA and JEIDA also expanded their mission and purpose to embrace any technology that would work in a PC Card form factor rather than restricting it to silicon-based technology. This allowed for the development of high capacity rotating storage cards.

Today, virtually every type of card imaginable is available, including fax/modems, audio, SCSI, video, LAN adapter, and global positioning system cards. Almost all mobile computers shipped today have PC Card sockets that support 16-bit PC Cards along with 32-bit CardBus technology. JEITA and PCMCIA have ensured that PC Card technology has kept pace with industry trends—allowing for lower voltage and higher performance cards, and embracing the trend toward serial data buses such as USB. PC Card technology has fast become the preferred bus expansion interface in mobile computing and is a growing force in the mobile computing and consumer electronics markets.

PCMCIA and JEITA are both standards setting bodies and trade associations. PCMCIA's mission is "To develop standards for modular peripherals and promote their worldwide adoption."

There have been various revisions of the ***PC Card Standard*** as described in the following section.

1.2.2 PCMCIA Standard Release 1.0/JEIDA 4.0 (June 1990)

The first release of the Standard defined the 68-pin interface and both the Type I and Type II PC Card form factors. The Japan Electronic Industry Development Association (JEIDA) originally defined the Integrated Circuit card form factor utilizing 68-pin and socket connectors in 1985. The initial release of the ***PCMCIA Standard*** also specified all the electrical and physical requirements for memory cards. It defined the Metaformat or Card Information Structure (CIS) that is critical to interoperability and plug-and–play for PC Cards.

There was no concept of input/output (I/O) cards in the first release of the ***PC Card Standard***.

1.2.3 PCMCIA Standard Release 2.0/JEIDA 4.1 (September 1991)

The second release of the standard defined an I/O interface for the same 68–pin interface as was used for the PCMCIA memory cards in the first release of the Standard. The second release of the Standard also added various clarifications to the first release, support for dual–voltage memory cards, and sections dealing with card environmental requirements and test methods.

The initial version of the software Application Programming Interface (API) embodied in the BIOS–type ***Socket Services Specification*** was published in Release 2.0. Many additions were made to enhance the Card Information Structure (CIS) definitions, including the addition of geometry and interleaving tuples. Support for eXecute In Place (XIP) was also added in this release.

1.2.4 PCMCIA Standard Release 2.01 (November 1992)

The initial version of the ***PC Card ATA Specification*** defining an interface for PC Cards using the AT Attachment Standard was defined in this release. To accommodate rotating media PC Cards, the Type III PC Card was added with this release. The ***Auto-Indexing Mass Storage (AIMS) Specification,*** geared toward digital images, was also added.

The initial version of the ***Card Services Specification*** was published with this release. This part of the standard PC Card software API defined the operating system extensions required for resource management of cards, sockets and drivers. Socket Services was enhanced to accommodate the requirements of the new Card Services interface.

Additional changes were made to the Metaformat (CIS) definitions to accommodate new PC Card functionality.

1.2.5 PCMCIA Standard Release 2.1/JEIDA 4.2 (July 1993)

The Card and Socket Services software specifications were enhanced based on implementations done in compliance with the previous Standard to form a complete and robust software architecture and API necessary for compatible implementations.

The Electrical and Physical sections of the standard were updated with corrections and additions, and the CIS was again improved with additional definition information.

1.2.6 PC Card Standard February 1995 (Release 5.0)

The ***PC Card Standard February 1995 Release*** added information to improve compatibility with the Standard by requiring a Card Information Structure (CIS) on every PC Card, extending the amount of information within the CIS, adding a ***Guidelines*** volume to help developers implement the Standard, and defining common media storage formats.

The Standard was also enhanced to support the following optional features:

- Low-voltage-only operation (3.3 volt)
- Hardware Direct Memory Access (DMA)
- Multiple-function cards
- Industry standard power management interface (APM)
- A high throughput 32–bit bus mastering interface (CardBus)

1.2.6.1 PC Card Standard March 1995 Update

Included as errata to the First Printing of the February 1995 Release. Included general editorial changes.

1.2.6.2 PC Card Standard May 1995 Update

Included along with the ***March 1995 Update*** in the Second Printing. Included change to Power Waveforms at Power-on in the ***Electrical Specification***.

1.2.6.3 PC Card Standard November 1995 Update

Included along with the ***March 1995*** & ***May 1995 Updates*** in the Third Printing. Included Custom Interfaces and other updates.

1.2.6.4 PC Card Standard March 1996 Update

Released only as errata. Included Flash Translation Layer, Zoomed Video Port and other updates.

1.2.7 PC Card Standard March 1997 (Release 6.0)

The ***PC Card Standard March 1997 Release*** provided a variety of compatibility and functionality features. All of the Updates to the February 1995 release, including Custom Interfaces and the Zoomed Video (ZV) Port Custom Interface were incorporated into this release.

A Thermal Ratings system was added that allows cards and hosts to be rated for thermal output, providing an interface to warn users of a potentially damaging thermal condition.

The following features were also added:

- Power Management
- ISDN Function Extension Tuples
- Security and Instrumentation Card Function ID Tuples
- Physical Socket Naming
- Hot Dock / Undock Software Support
- Streamlined PC Card Software Configuration

1.2.8 PC Card Standard 6.1 Update (April 1998)

The ***PC Card Standard 6.1 Update*** added the following features:

- PCI / CardBus Power Management
- Small PC Card Form Factor
- Socket Services Packet Interface
- Win32 Bindings
- Editorial changes to the ***Electrical Specification***, ***Metaformat Specification, Card Services Specification***, ***Media Storage Formats Specification*** (FTL), ***PC Card ATA Specification***, and ***PCMCIA Specific Extensions*** (Modem I / O Unshielded Connector)

1.2.9 PC Card Standard Release 7.0 (February 1999)

The ***PC Card Standard Release 7.0*** added the following features:

- DVB Custom Interface
- Windows NT 4.0 Kernel Mode Bindings
- PC Card Memory Paging
- Serial Bus Adapter Function Extension Tuples
- Editorial changes to the ***Electrical Specification***, ***Metaformat Specification, Card Services Specification***, and ***Host System Specification***

1.2.10 PC Card Standard 7.1 Update (March 2000)

The ***PC Card Standard 7.1 Update*** added the following features:

- OpenCable™ POD Custom Interface
- Noted July 1, 2000 removal of references to DMA (Direct Memory Access)
- Card Services access to CardBus **Latency Timer** register
- Editorial changes to the ***Electrical Specification***, ***Physical Specification***, ***Metaformat Specification, Card Services Specification***, ***Guidelines***, and ***Host System Specification***

1.2.11 PC Card Standard 7.2 Update (November 2000)

The ***PC Card Standard 7.2 Update*** added the following features:

- Added maximum current requirements to 16-bit PC Card interface
- Removed all references to DMA (Direct Memory Access)
- Editorial corrections to bring the ***PC Card ATA Specification*** into line with current ***ANSI ATA*** Specifications
- Added Standardized Zoomed Video Port Register Model Guideline
- Added SmartCard Reader / Writer Grounding Guidance Guideline
- Added Limited Host (Lhost) Guideline

- Modified test requirements for 4/7 Position and 15 Position I/O Connectors to eliminate inconsistencies with the ***Physical Specification***

1.2.12 PC Card Standard 8.0 Release (April 2001)

The ***PC Card Standard 8.0 Release*** added the following features:

- Added CardBay high-performance serial interface
- Added support for Vcore supplemental voltage for CardBus (3.3V **VCC**/1.8V **VCORE**) and CardBay (3.3V **VCC**/1.8V **VCORE** or 5V **VCC**/3.3V **VCORE**) PC Cards
- Redefined the **VPP1** and **VPP2** pins (**VPP[2::1]**) as simply **VPP** pins since new host systems based on this release of the ***PC Card Standard*** are no longer required to provide separate programmable voltages on each pin.
- Added 3 Watt maximum thermal power recommendation for responsible card design

1.3 Uses

PC Card technology is used in a wide variety of products including notebook computers, sub-notebook computers, palmtop computers, pen computers, desktop computers, cameras, printers, telephones, medical instruments, television set-top boxes and other embedded application hosts. PC Cards supporting storage and I/O applications for the host systems mentioned above also incorporate PC Card technology as does the system and application software required to operate the cards and hosts.

The ***PC Card Standard*** is aimed at developers of the above-mentioned PC Card-based products and is designed for the technical audience. The Standard is intended for use by technical developers to create standard PC Card products such as cards, hosts, silicon, and software.

1.4 Future Trends

The future holds great promise for the PC Card technology that has been widely adopted by the mobile computer industry. We can look forward to the continuing acceptance of this technology by the computing industry in desktops, printers, and other computer peripherals as well as products that are the result of the merging of computers with other technologies such as telephones and television set-top boxes. The future will also see the PC Card interface evolve to include higher speed serial buses to support high speed networking, video and other applications. Any applications that require a small, portable and rugged industry standard interface to a system bus will find PC Card technology and the ***PC Card Standard*** suitable to their needs.

PCMCIA and JEITA will continue to maintain, enhance, and extend the ***PC Card Standard*** to accommodate the ever-changing technological and market requirements.

1.5 The PC Card Standard — A PCMCIA and JEITA Joint Release

This PC Card Standard had its early roots in technical organizations and volunteers in Japan and in the United States. The more recent activities creating the ***PC Card Standard*** have been worldwide.

The Japan Electronic Industry Development Association, JEIDA (now known as the Japan Electronics and Information Technology Industries Association, JEITA), recognized the importance of integrated circuit memory cards back in 1985 and has standardized a wide range of card interfaces and form factors since that time. This work included the publication of the JEIDA ***Version 3 IC Memory Card Specifications***; one of which, the 68-pin version, served as the starting point for the ***PC Card Standard***.

The Personal Computer Memory Card International Association, PCMCIA, was founded in Silicon Valley, California in 1989 to promote the development and standardization of memory cards for mobile computers. PCMCIA grew quickly to encompass a worldwide membership with chapters and local host offices on several continents.

Beginning in 1989, JEIDA and PCMCIA worked closely together to develop the similar documents of the JEIDA ***IC Memory Card Specification*** and the ***PCMCIA Standards***. While these documents and their later enhancements were similar, they were not identical and in some cases there were discrepancies both in language and content between the documents. Today's ***PC Card Standard*** is the unified result of a joint effort between PCMCIA and JEITA to enhance the clarity and scope of the documents as well as to resolve the differences between the specifications.

The PC Card Standard is published jointly by PCMCIA and JEITA. Thousands of hours contributed by corporations and individuals from all around the globe have supplemented the efforts of the professional staffs of JEITA and PCMCIA in creating this worldwide ***PC Card Standard***.

2. DEFINITIONS AND TERMINOLOGY

There are many terms and conventions used in the ***PC Card Standard*** and a good understanding of them will make reading and working with the Standard much easier. General terms and conventions that can be broadly applied will be described in this section. Specific terms and conventions that relate to individual sections of the Standard will be described at the beginning of each section.

The term 'PCMCIA' is an abbreviation for Personal Computer Memory Card International Association, and is used to refer to the organization itself. The term 'PC Card' is used to refer to the technology as well as being a generic term for any products based upon the ***PC Card Standard***. 'PC Card' is used as a generic term to refer to 16-bit PC Cards, 32-bit CardBus PC Cards, and high-performance serial CardBay PC Cards.

The term 'PC Card Standard' is the official name of the set of specifications produced jointly by PCMCIA and JEITA. The term 'Standard', with a capital 'S', is a proper name used as a short form replacement for the complete term: the ***PC Card Standard***.

When referring to products (both card and sockets) that support 16-bit operation, the terms '16-bit PC Card' or '16-bit PC Card socket' should be used. 'CardBus PC Card' is the correct term that can be used when referring to the 32-bit bus master specification of the ***PC Card Standard***. Likewise, 'CardBay PC Card' is the correct term to be used when referring to the high-performance serial specification of the ***PC Card Standard***. Note that both the "C" and the "B" are capitalized for both CardBus and CardBay. The terms 'PCMCIA Card' and 'PCMCIA socket' should never be used.

This page intentionally left blank.

3. COMPATIBILITY

Over time, PC Cards containing new technologies have been introduced, and significant new capabilities have been added to the Standard. At the same time, card, host and software vendors have gained considerable experience and opportunities to improve compatibility have been recognized. The goal remains to make PC Card technology as easy to use as possible with the ideal scenario being that the customer takes the PC Card out of its box, plugs it into the system and begins to use it. It is recommended that in order to support PC Card technology, developers keep the goal of compatibility in mind and use the areas of the Standard designed to support compatibility and interoperability. Also, there is opportunity within the PCMCIA organization meetings to discuss compatibility and share information.

The Standard encompasses many capabilities and optional features. Due to this complexity, manufacturers can choose different feature sets or even have different interpretations. Therefore, development planned for flexibility and adaptability will allow for the greatest compatibility. One way to be prepared for the variety of the real world is to perform exhaustive testing of designs with all of the significant components: from software functions and modules to entire platforms.

On a very general level, the following describes how a card and system interact when they are "compatible:"

For a card to operate properly, the host must first be able to provide adequate power at the correct voltage(s) to identify and operate the card. It must successfully identify the card by reading its Card Information Structure (CIS), and, in some cases, by sensing several pins on the interface. These pins are important in systems mechanically able to accept CardBus, CardBay or other low voltage cards. For 16-bit PC Cards and CardBus PC Cards, the CIS contains detailed information on a card including its allowed "configurations" which tell the host system the various ways that the card can be set up and what system resources are required. For CardBay PC Cards, the query process is used prior to applying power to the card to define the basic capabilities and configuration requirements for the card.

Once a 16-bit or CardBus card has been identified, the system must determine if the card requires a user-installed Card Services client driver (typically LAN cards, SCSI cards, audio cards or CardBus cards). If no user installed driver software is found, the system then determines whether the card can be supported by the host's built-in "Super Client" driver (typically memory cards, ATA devices or Fax/Modems). The host then links the card with the appropriate driver and configures the card and the socket. Given that the card is identified as a CardBay card, the host links the card to the appropriate electrical interface, e.g. USB, and power is then enabled to the card to allow that interface to initialize.

In the case of a data storage device such as a memory card or disk drive, the file system must be able to access the data on the card. This sometimes requires a link to be established with a specific installable file system.

A user may want to "suspend" and "resume" the operation of notebook or other system with PC Cards in the slots. To do this successfully, a card-specific routine must communicate with advanced power management software, which must then access the card through Card and Socket Services. For CardBay PC Cards, power management features are managed by the connected interface, e.g. USB.

Lastly, Card Services Client Drivers must operate consistently from one card supplier to the next, and be as flexible as possible to accommodate varying system configurations automatically. Also, "card-aware" application programs, like communications programs, need to coexist with older applications programs.

This page intentionally left blank.

4. TECHNICAL DESCRIPTIONS

4.1 Volume 2: Electrical Specification

The ***Electrical Specification*** specifies the connector pinout, interface protocol, signaling environment, interface timings, programming model, and specifics of card insertion, removal, power up, and configuration. The ***Electrical Specification*** describes three basic classes of PC Cards: 16–bit PC Cards, CardBus PC Cards, and CardBay PC Cards.

The 16-bit PC Card interface provides an ISA compatible interface for full-size and Small PC Cards. This interface supports standard ISA interrupts, and is intended to support both memory and I/O applications.

To address the class of applications that require higher performance and to take advantage of host systems that implement the PCI system bus, a 32-bit interface was developed known as CardBus. This interface provides 32-bit bandwidth, reduced latency via bus master capability, or both. CardBus hosts are required to support 16-bit PC Cards. The Small PC Card form factor does not support the CardBus interface.

CardBay brings the PC Card interface in line with the latest serial bus technology based on the Universal Serial Bus (USB). While preserving the CardBus form factor, CardBay takes advantage of existing USB plug-and-play configuration and host software class driver support. CardBay host implementations are required to implement the low-speed and full-speed modes of USB and can optionally provide high-speed USB support. Host platforms designed to support CardBay shall also provide backward compatibility with CardBus and 16-bit PC Cards.

4.2 Volume 3: Physical Specification

The ***Physical Specification*** specifies the PC Card's physical outline dimensions, basic mechanical capabilities and the environmental conditions under which the PC Cards are expected to operate. Information is provided for Type I, II, and III full-size and Small PC Cards, for 5 volt and low voltage equivalents, and 32-bit CardBus. With regard to physical characteristics, CardBay is equivalent to CardBus.

Interface dimensions for the 68-position host connectors (with pin contacts) and the mating card connectors (with female socket contacts) are provided. The specification, in consideration of EMI issues, also presents a method for grounding the PC Card along with applicable material and electrical considerations helpful to both system designers and card users. Connectors for CardBus and CardBay applications are included. A special host/header connector is required that will assure proper grounding. This host will also accept standard low voltage Type I, II and III PC Cards.

Host PCB board layout dimensions are provided for various footprint options, for both SMT (Surface Mount Technology) and through-hole mounting.

The PC Cards are intended to function in both office and harsh environments. These environments are defined. Test criteria are provided using industry MIL, ISO and JIS Standard specifications. This provides manufacturers with quantitative data to help confirm expected application performance. It is up to the individual suppliers to qualify their parts to this, and any other manufacturer's specification.

Separate criteria are defined for PC Cards involving SRAM and rotating memory components. Where applicable, the specification's requirements include considerations for PC Cards incorporating write-protect switches and batteries.

4.3 Volume 4: Metaformat Specification

The ***Metaformat Specification*** specifies the structure and contents of card description information. This card description information is stored on the card and is commonly called the Card Information Structure or CIS.

As is done with networking standards, the Metaformat is a hierarchy of layers. Each layer has a number, which increases as the level of abstraction gets higher. Below the Metaformat is the physical layer: the electrical and physical interface characteristics of PC Cards. The Metaformat layers include the Basic Compatibility Layer, the Data Recording Format Layer, the Data Organization Layer, and the System-Specific Layer.

The benefits of using Metaformat include flexibility in describing configuration options, ability to handle numerous somewhat incompatible data recording formats and data organizations.

4.4 Volume 5: Card Services Specification

The ***Card Services Specification*** specifies a software Application Programming Interface (API). The main purpose behind the Card Services (CS) API is to provide a universal software interface that is independent from the hardware that manipulates PC Cards and PC Card Sockets.

The Card Services interface has two goals. The first is to promote sharing of PC Cards, sockets and host system resources. Second, the interface provides a centralized location for common functionality required by PC Card software. The Card Services interface is structured in a client/server model. Software applications and device drivers that utilize PC Cards are the clients. Card Services is the server providing services requested by the clients.

The API is specified in a host system/operating system-independent format. However, there are bindings included that describe the detail of how to access a Card Services implementation in a particular environment. Clients register with Card Services and are notified of PC Card events synchronously via a Callback. Clients use Card Services to allocate system resources to a PC Card function and to configure the PC Card.

Card Services is very closely related to Socket Services. Card Services is the middle layer in the multiple layer software architecture. The clients make up the top layer of the architecture.

4.5 Volume 6: Socket Services Specification

The ***Socket Services Specification*** specifies a software Application Programming Interface (API). The main purpose behind the Socket Services (SS) API is to provide a universal software interface to the hardware that controls sockets for PC Cards. The interface masks the details of the hardware used to implement these sockets. This masking allows the development of higher-level software that is able to utilize PC Cards without any detailed knowledge of the actual hardware interface.

Socket Services manages the hardware by utilizing it as a number of object types. Each object type has a particular area of functionality. Sockets are the receptacles for PC Cards. Windows provide access via host system memory or I/O address space to PC Card address space. EDC Generators calculate error detection codes by monitoring data transfers. Adapters connect a host system's bus to PC Card sockets and provide the sockets, windows and EDC generators.

Individual services of Socket Services provide certain functionality. Some services allow software to inquire about the capabilities for a specified object. Other services return the current settings of a specified object. Also, the settings for a specified object are updated using other services. In addition, there are services that report on current card status and provide indirect access to PC Cards for socket controllers that cannot map PC Card address space into host system address space.

Socket Services performs all of these services when software requests them. These requests are made in a host system processor and operating environment-specific manner. For example, on x86 architecture platforms running DOS, a Socket Services implementation is invoked via a software interrupt with commands and data passed in CPU registers.

Socket Services is very closely related to the ***Card Services Specification***. Socket Services is the lowest layer in a multiple layer software architecture.

4.6 Volume 7: PC Card ATA Specification

The ***PC Card ATA Specification*** specifies the operation of mass storage PC Cards using the protocol of the ANSI AT Attachment (ATA) Interface for Disk Drives in the PC Card environment. This standard includes both the usage of the ANSI ATA-defined protocols and the differences required due to conflicts between the PC Card and ANSI ATA Standards.

The ***PC Card ATA Specification*** defines four mappings of the ANSI ATA Command/Control Registers into host memory and I/O space: memory mapped, block I/O, ANSI ATA Primary and ANSI ATA Secondary. This definition includes how the 8-bit ANSI ATA registers are accessed and the use of the **RESET**, **READY**, and **IREQ#** signals depending on whether memory mapped or I/O mode addressing is used.

Since both the ***PC Card ATA Specification*** and the ANSI ATA Standard define resets, the effects and protocols associated with the different reset methods are described. The method for implementing ANSI ATA Master/Slave devices is described as the Twin Card option in the ***PC Card ATA Specification***, detailing the operation required since inter-card communication is not provided. In addition, both Cylinder-Head-Sector as well as Logical Block addressing are supported.

Finally, mandatory and optional CIS tuples for PC Card ATA mass storage devices are defined to ensure that PC Card ATA implementations are consistent from vendor to vendor.

4.7 Volume 8: Host System Specification

The ***PC Card Host System Specification*** specifies requirements for host systems containing a PC Card socket.

The System Thermal and Power section defines a method that can be used in determining the host platform thermal rating. The purpose of determining the thermal rating is to ensure that the heat generated and dissipated within the body of the PC Card does not thermally exceed the capabilities of the host system to remove excessive heat in order to maintain the PC Card at an acceptable temperature limit.

The PCI Bus Power Management Interface Specification for PCI-to-CardBus Bridges establishes a standard set of PCI peripheral power management hardware interfaces and behavioral policies. Once established, this infrastructure enables an operating system to intelligently manage the power of PCI functions and buses.

The PCI-to-CardBus Bridge Register Description section is provided to aid in development of CardBus bridges that have some level of software interface commonality. The device described is a bridge between a PCI bus and two CardBus / 16-bit PC Card sockets.

The Socket Physical section defines the physical characteristics of the host PC Card socket necessary to ensure physical compatibility with all PC Card package types.

4.8 Volume 9: Guidelines

The ***Guidelines*** document provides implementation examples and further explanations of the ***PC Card Standard*** to:

- Enhance the interoperability of PC Card components, including card hardware and software, system hardware and software, and applications.
- Facilitate the development of PC Card technology by increasing the understanding of the Standard by PC Card Implementation community.

These guidelines are not requirements made by the PCMCIA or JEITA Standards organizations. Rather, they are implementation examples, suggestions and hints. The Guidelines included are described below.

Electrical Guidelines

- CardBus / PCI Common Silicon
- Thermal Logo Usage
- Standardized Zoomed Video (ZV) Register Model

Physical Guidelines

- Modem I / O Unshielded Connector for Open Systems
- 15 Position Shielded Latching I / O Connector
- Maximum I / O Connector Dimensions
- Extended Card Dimensions
- Extended PC Card Guidance for SmartCards

Software Guidelines

- Enabler Capabilities and Behavior
- Card-Application Interaction
- CardBus Operational Scenarios
- CIS Design for Several Common Implementations

Limited Host Guidelines

4.9 Volume 10: Media Storage Formats Specification

The ***Media Storage Formats Specification*** specifies how data are formatted on PC Card storage devices to promote the exchange of these cards among different host systems. These include memory cards using various types of volatile and non-volatile devices and ATA disk drives, for both silicon and rotating media. Each of these storage technologies have unique characteristics which may benefit from different storage techniques and handling. This has resulted in the development of different storage formats and/or partitioning for PC Cards using these devices.

The ***Media Storage Formats Specification*** is intended to provide enough information to allow software developers to use data stored on PC Cards by other host systems using potentially different operating and file systems. Unless required to understand the data structures used on the PC Card, algorithms for updating the data on the PC Card are not specified, only the storage format.

NOTE: The inclusion of partition, file format, translation layer or media type information in this document does not constitute an endorsement by PCMCIA or JEITA. PCMCIA and JEITA are only acknowledging this information has been used to record data on a PC Card and, in some cases, that PCMCIA and JEITA members have agreed that using the documented implementation may reduce problems encountered when attempting to interchange data between host systems.

Starting with Release 8.0 of the **PC Card Standard**, *the* **Media Storage Formats Specification** *is not included with the printed standard but is still available as a supplemental document. (Please contact the PCMCIA for more information.)*

4.10 Volume 11: XIP (eXecute In Place) Specification

The ***XIP (eXecute In Place) Specification*** specifies a method to directly execute applications from ROM without loading the image of the application into RAM prior to execution. The benefit of XIP is savings of both system RAM and system ROM. Usually, in the non-XIP world, a program is loaded from a disk (or ROMDISK) and essentially copied into system RAM, from where it is executed. Thus, there is an immediate waste of space since two images of the program exist: one in RAM and one on the disk. Under the XIP scheme, only the data is stored in RAM; code is left executing from the original instance in ROM. The current PC Card specification for XIP is designed primarily for low-end real mode x86 type systems, where price sensitivity is high and system RAM is a precious resource.

The ***XIP Specification*** describes the Metaformat tuples, data structures, driver architecture, and the Application Programming Interface (API) for XIP, as well as the architecture and load format of XIP-compliant applications.

Three types of XIP support are defined in order to support three real-world architectures: LXIP, SXIP and EXIP.

LXIP is for systems where demand-paging is required (i.e., pages not in memory must be explicitly paged in by software at some level). LXIP Applications are structured to operate in a 16 KB paged-execution environment.

SXIP is for those systems that have only very limited paging mechanisms. SXIP applications comprise an execution image of at most 64K of code and / or read-only data, and are monolithic in nature. These applications do no overlaying of any sort.

EXIP is for those systems with very large address spaces or with implicit paging (i.e., pages not in memory when accessed are placed into memory without intervention at a software level). EXIP applications are structured to operate in an environment where no paging is necessary, similar to an Intel 80386 extended-addressing-mode-execution environment.

Starting with Release 8.0 of the **PC Card Standard**, *the* **XIP Specification** *is not included with the printed standard but is still available as a supplemental document. (Please contact the PCMCIA for more information.)*

5. GLOSSARY

Combined Terms and Abbreviations

16-bit PC Card
PC Cards using the *PC Card Standard* 16-bit interface originally defined in PCMCIA 1.0/JEIDA 4.0 and PCMCIA 2.0/JEIDA 4.1 publications.

access latency
The time between a master requesting access to CardBus PC Card and the completion of the first data phase. Access latency consists of three parts: arbitration latency, bus acquisition latency and target latency.

Adapter
The hardware that connects a host system bus to 68-pin PC Card sockets.

Address Space
An address space is a collection of registers and storage locations contained on a PC Card that are distinguished from each other by the value of the Address Lines applied to the Card. There are three separate address spaces possible for a card. These are the Common Memory space, the Attribute Memory space and the I/O space.

Address Space(s), CardBus
A reference to the three separate physical address spaces of CardBus PC Card: memory, I/O, and configuration.
A reference to any of the CardBus PC Card card's physical address spaces, which include:

- six spaces which may map the card I/O or memory into the host system address space
- one space which may map the card expansion ROM into the host system address space
- the card's configuration spaces (one for each function)

agent
A logical entity that operates on a host system bus. The term applies collectively to functions of a bus master, a bus slave or to a combination of both.

ANSI ATA Standard
ANSI X3.221-1994.

Application Program Interface (API)
A function interface provided by one level of software to the level above it.

arbitration latency
The first component of access latency. The time that the master waits after having asserted **CREQ#** until it receives **CGNT#**.

area
See memory area.

ASCIIZ
A text string in ASCII format terminated with a byte of zero.

Asserted
A signal is asserted when it is in the state that is indicated by the name of the signal. Opposite of Negated.

asserted, deasserted
These terms refer to the state of a signal on the clock (CCLK) rising edge, not to signal transitions.

AT
Acronym for Advanced Technology. Refers to a 16-bit host system architecture using the 80x86 processor family which formed the basis for the ISA Bus definition.

ATA
Acronym for AT Attachment. Refers to the interface and protocol used to access a hard disk in AT compatible host systems. Disk drives adhering to the ATA protocol are commonly referred to as IDE interfaced drives for PC compatible host systems.

ATA Command Block
See Command Block registers.

ATA Registers
These registers are accessed by a host to implement the ATA protocol for transferring data, control and status information to and from the PC Card. They are defined in the *"ANSI ATA Standard."* These registers include the Cylinder High, Cylinder Low, Sector Number, Sector Count, Drive/Head, Drive Address, Device Control, Error, Feature, Status, and Data registers. The I/O and memory address decoding options for these registers are defined in the ***PC Card ATA Specification***

ATA Soft Reset
The condition of the PC Card ATA mass storage card when the SRST bit in the Device Control register is set. This condition directly affects only the ATA registers and protocol. Except for reflecting the state of the Busy condition and Interrupt condition, the Configuration registers are unaffected.

Attribute Memory
16-bit PC Card memory region selected by the REG pin for storage of CIS data and card configuration registers.

Attribute Memory Space
One of the three address spaces available on a PC Card. This address space is accessed by

	memory read and memory write operations which occur while the **REG#** signal is asserted. This address space is defined only for bytes located on even byte addresses. This space is the primary location for the Card Information Structure and for the Configuration registers on the card.
Audio Device	A device that normally provides both a speaker and microphone for input/output of audio. Optionally, if the application allows, the device can be limited to only output (speaker) capability.
Average Current	The highest averaged current value over any 1 second period.
backoff	A directive to terminate the current transaction and retry it at a later time, also referred to as retry.
Base Address Register Window	A memory or I/O space mapping supported by a Base Address Register in the card's configuration space.
BIOS	Acronym for Basic Input/Output System. When BIOS is in Read-Only Memory devices it may be referred to as ROM BIOS.
BIST register	An optional register in the header region of the CardBus Configuration Space. It is used for control and status of built-in self-tests.
bit field	A field containing only 1 bit.
Block	A block is the basic 512 byte region of storage into which the storage media is divided. Addressing in the ATA protocol is performed on block boundaries. Each block of data represents one sector of data using the ATA Cylinder-Head-Sector address protocol. The Logical Block Address protocol uses sequential block addresses to access the media.
Block Allocation Map (BAM)	An FTL control structure that is used to store Erase Unit block allocation information when hidden areas are not used to store this information. See the ***Media Storage Formats Specification***.
BPB	Acronym for BIOS Parameter Block. A data structure used by the Microsoft BPB/FAT File System to describe the size and format of storage media.
bridge	The logic that connects one computer bus to another, allowing an agent on one bus to access an agent on the other, such as a CardBus controller.
BSY (ATA Busy bit)	A bit in the ATA Status register that is used by the ATA protocol to indicate that the ATA registers on the card are not available for use by the host.
burst transfer	The basic data transfer mechanism of CardBus PC Cards. A burst is comprised of an address phase and one or more data phases.
bus acquisition latency	The second component of access latency. The amount of time that a requesting device waits for the bus to become free after **CGNT#** has been asserted.
bus commands	Used to indicate to a target. The type of transaction the master is requesting.
bus master	An agent that has an ability to obtain control of the interface and perform memory or I/O reads and writes to system resources. The master initiates a bus transaction.
Bus Segment Reset	Bus Segment Reset is defined as the hardware reset signal that is taken as actual physical input to a given component within a system. For example the Bus Segment Reset signal for a PCI to CardBus bridge component is **RST#** as defined in the ***PCI Local Bus Specification***. For CardBus cards, this is the **CRST#** signal.
bus slave	An agent that sends or receives data under control of a bus master, also referred to as bus target or a bus transaction target. There are two types of slaves: I/O slave – selected by its address in the I/O address space; memory slave – selected by its address in the memory address space.
Callback Handler	A Client routine to which Card Services may transfer control when events requiring Client notification occur.
Card Configuration and Status Register	This Configuration register provides the host control for the following functions: Status Changed Signal, Audio Signal, and Power Down Request. It provides status information about Status Changed state and Interrupt Request state. In addition, it can be used to advise the card that all I/O to the card will be eight bits wide. Refer to the *PC Card Standard Electrical Specification* for detailed information about this register.
Card Enumeration	The process performed by the host to provide a unique card identification number to each drive when the Twin Cards option is used. The host writes a unique number to the Copy field in the Socket and Copy register of each card sharing the same configuration.
Card Information Structure (CIS)	A data structure which is stored on a PC Card in a standard manner which contains information about the capabilities of the card as well as the formatting and organization of data on the card.

Card software — Software that configures and/or accesses the card. This may include:

- device drivers
- applications
- generic enablers

In PC Card parlance, card software is that software which could be a Card Services client.

CardBay PC Card — PC Cards which use the high-performance serial interface described in the ***PC Card Standard***.

CardBay PC Card socket — A receptacle into which a CardBay PC Card can be inserted. The term socket has similar meaning, but can apply to 16-bit PC Card, CardBus PC Card, CardBay PC Card, or all types of sockets.

CardBus Function — A set of functionality inside a CardBus card represented by one 256 byte configuration space. Each CardBus function within a device generally has a separate software driver.

CardBus PC Card — PC Cards that use the 32-bit interface defined in the *PC Card Standard*. A single CardBus PC Card may contain up to eight CardBus Functions.

CardBus PC Card adapter — The chip(s) that isolate(s) the CardBus PC Cards from the rest of the system. Depending on the definition of the system bus, this might be a set of electrical buffers or it may be a complete bus bridge. This is the same as the host CardBus PC Card adapter.

CardBus PC Card arbiter — A function that controls access to the CardBus PC Card interface.

CardBus PC Card connector — An expansion connector that conforms to the electrical and mechanical requirements of the PC Card Standard for CardBus PC Cards.

CardBus PC Card sequencer — An entity that performs the actual CardBus PC Card operations in a device, e.g., a state machine. The sequencer guarantees that the CardBus PC Card protocol is not violated.

CardBus PC Card socket — A receptacle into which a CardBus PC Card can be inserted. The term socket has similar meaning, but can apply to 16-bit PC Card, CardBus PC Card, CardBay PC Card, or all types of sockets.

central resource — The interface support functions supplied by the host system that is typically in a host CardBus PC Card adapter, or could be distributed in the system.

CHS — Acronym for Cylinder-Head-Sector addressing.

CIS — Acronym for Card Information Structure.

Clear (a bit) — A bit is Cleared when its value is set to "0."

Client — A user of Card Services, Socket Services, or XIP functions. May be a device driver, utility program or application program.

clock edge (or edge) — Refers to the rising edge of the clock (**CCLK**). The only time that the signals have any significance on the CardBus PC Card interface is at the rising edge of the clock.

Cluster — Another term for a block.

Command Block Registers — The ATA Command Block registers include the following ATA registers: Data register(s), Error register, Feature register, Sector Count register, Sector Number register, Cylinder Low register, Drive/Head register, Command register, and Status register, but not the Alternate Status register. Seven of the Command Block registers are written by the host to provide a command and its parameters. These registers are: Feature register, Sector Count register, Sector Number register, Cylinder Low register, Cylinder High register, Drive/Head register, and Command register.

Common Memory — Conventional memory area on 16-bit PC Cards when **REG#** is negated.

Common Memory Space — This 16 bit wide, memory space is one of the three address spaces available on the 16-bit PC Card. This address space is accessed by memory read and memory write operations which occur while the **REG#** signal is negated. This address space is defined both for bytes located at even and odd byte addresses. A PC Card bus multiplexing protocol is used to ensure that the odd bytes of this space can be accessed by both eight and 16 bit hosts. The ATA registers are located in this space when Memory Mapped ATA registers are supported.

Configuration — Configuration is a process by which a host initializes or alters its socket operation and the Configuration registers on a PC Card to match the PC Card's capabilities to the host's capabilities and available system resources.

configuration address space — See configuration space

configuration cycle — A CardBus PC Card cycle used for system configuration via the configuration address space.

Configuration Option Register — This register is the first of the Card Configuration registers located in the Attribute Memory Space of a PC Card. It is used by the host to control the PC Card's Configuration Index in bits 5 to 0, its Interrupt Mode in bit 6 (Pulsed = 0 or Level =1) and the PC Card Soft Reset in bit 7 (Soft Reset asserted = 1).

Configuration Registers	A set of registers, defined by the *PC Card Standard,* which are used by the host to control the operational configuration of the card.
Configuration Space	A CardBus PC Card address space, used for configuration and error handling, which consists of a 64-byte header space and a 192-byte device-dependent space.
Contiguous I/O Addresses	An I/O address decoding in which the Card decodes address lines (example A[3::0]), while the Socket is responsible for decoding all other address lines to produce the Card Enable signals for I/O cycles to the card.
Control Block Registers	The ATA Control Block registers include the following ATA registers: Alternate Status register, Device Control register and Drive Address register.
Custom Interface	Custom Interfaces support enhanced features, such as internal bus extensions, or customized signals not applicable across architectures.
Cylinder	Group of tracks accessed without moving the head used to read or write rotating media.
Cylinder-Head-Sector Address	A method for specifying the location of a block of data on a mass storage device. This is the traditional method for addressing a block of data on rotating media using the ATA protocol. This method partitions an address into a cylinder portion, one or more heads within each cylinder and one or more sectors within each cylinder-head combination.
DAA	Direct Access Attachment. A device that provides electrical protection to telecommunications medium. It may be internal or external to a Modem I/O Card. (See ***Guidelines***)
Device Dependent Space	The last 192 bytes of the CardBus PC Card Configuration Space. In this context, “device” is synonymous to “function.”
Digital Video Broadcasting Port	A PC Card Custom Interface which provides a bi-directional video and audio bus and a command control interface providing a DVB compliant Conditional Access system.
Direct Memory Access (DMA)	The process of moving data from I/O to memory or vice versa without the intervention of the processor.
Direct Memory Access, third party	When DMA is performed by a DMA controller as opposed to having an I/O device become a master on the bus and move the data to/from memory on its own.
Directory	A system file used to maintain the structure of a file system.
DMA	Acronym for Direct Memory Access
DOS	Acronym for Disk Operating System. More specifically, the term refers to MS-DOS, DR DOS, Novell DOS, Datalight ROM DOS, et al.
Double Word	A 32-bit block of data, also known as Quadlet.
Dual Drive	The Dual Drive option defines a single PC Card ATA mass storage card that contains two separate and distinct logical ATA devices. One device acts as the ATA Master, the other as the ATA Slave.
DUT	Device Under Test.
DVB	An acronym for Digital Video Broadcasting, a European television standardization body
DWORD	See Double Word.
Edge Sensitive Interrupt	An interrupt detected by the host system based upon the transition of the signal from negated to asserted. The host must see the edge to latch this type of interrupt. Commonly used in ISA Bus machines.
EISA	Acronym for Extended Industry Standard Architecture. Refers to an expansion bus promoted by manufacturers of IBM-compatible personal computers that feature 32-bit addressing and bus-mastering capabilities. Not compatible with Micro Channel. Compatible with ISA 8-bit and 16-bit adapter cards.
EISA Bus	An internal host Bus which is available in some hosts and can be used to connect PC Card sockets to the host CPU. An EISA bus can program each interrupt request line for either positive-true, edge sensitive, interrupts (IRQn) or negative-true, level sensitive, interrupts (IRQn#).
End-user	A person who uses a host system.
Erase Unit	The area of flash media that is handled as a single erasable unit by the FTL. An Erase Unit may be one (1) or more Erase Zones. All Erase Units in an FTL partition are the same size. The size of an Erase Unit is set when the FTL partition is formatted and the Erase Unit Headers written to the media. See the ***Media Storage Formats Specification***.
Erase Unit Header	An FTL data structure that describes an Erase Unit. See the ***Media Storage Formats Specification***.

Erase Zone — An area of flash media that must be erased as a single unit due to the characteristics of the media. May be determined from DGTPL_BUS and DGTPL_EBS in the Device Geometry Info field of the Device Geometry tuple, if present in the Card Information Structure. See the ***Media Storage Formats Specification***.

exclusive access — An access to a target's address range that is guaranteed to complete without being interrupted by an access to the same target by another bus master. Also known as atomic operation.

FFS — Acronym for Flash File System.

field — Depending on context, field may have different meanings.

- In the context of a tuple, a field is the smallest readable unit which has a distinct meaning.
- In the context of configuration and memory space, a field is a distinct area in a register.

File — A related unit of information stored on media.

File System — Part or extension of an operating system that manages files on a host system. May be limited or optimized to one type of media.

Flash — A type of non-volatile media that may allow byte read and write access, but requires the media to be erased before it is written. In addition, erase operations are required to be performed on a block of contiguous bytes.

FTL — Acronym for Flash Translation Layer.

Function — A PC Card capability, for example, a modem or LAN function.

function X (X is a number) — In a multifunction PC Card, each function is numbered uniquely. Numbering begins at 0, and all cards will therefore have a function 0. From the Card Services' client point of view, functions are numbered 1 to n, and all cards will therefore have a function 1.

generic enabler — A Card Services client which is capable of configuring a variety of cards. It may or may not have other capabilities such as:

- providing an alternate interface to Card Services
- providing the user information about the installed cards

This type of enabler is not custom designed for configuring specific cards; but, using the CIS and the Card Services interface, it can configure many different kinds of cards.

graceful rejection — It is made clear to the user that the PC Card is not usable in that socket, either through a message (visual or audio), or mechanical keying. In addition, no data corruption and no physical, electrical, or functional damage is caused to the system or card.

Handle — A Card Services assigned identifier associated with Card Services managed system resources.

Hardware Reset — See PC Card Hardware Reset.

Hardware Window — A 16-bit PC Card physical window (either memory or I/O). This is an area in a host system's memory or I/O address space through which a 16-bit PC Card may be addressed.

Header Space — The first 64 bytes of the CardBus PC Card Configuration Space. The Header Space consists of fields which allow a CardBus PC Card function to be generically controlled. See also Device Dependent Space.

Hidden Arbitration — Arbitration that occurs during a previous access so that no CardBus PC Card bus cycles are consumed by arbitration, except when the bus is idle.

High (Logic Level) — A signal is in the high logic state when it is above V_{IH} level. See the ***PC Card Standard Electrical Specification*** for the precise electrical definition.

Host — A computer system or other equipment which contains hardware (a Socket) and software for utilizing a PC Card.

Host System — Same as host

hot swapping — The ability to insert or remove a PC Card without cycling the system power or re-booting the system.

I/O — An abbreviation for Input / Output.

I/O Address Space — The I/O address space is one of the three address spaces available on a PC Card. The I/O address space is accessed by asserting the I/O Read signal, **IORD#**, or the I/O Write signal, **IOWR#**, while the Attribute Memory Select Signal, **REG#**, and at least one Card Enable, **CE1#** or **CE2#** are asserted.

I/O Card — ***PC Card Standard*** compliant card used for I/O (input/output) operations and connected internally to medium via a Medium Access Device. (See ***Guidelines***)

I/O Cycle — An I/O cycle is an Input operation(I/O Read) or Output operation (I/O Write) which accesses the PC Card's I/O address space.

I/O Interface	The I/O Interface is an interface supporting both memory cycles and I/O cycles. This interface is not active at power up or following a PC Card reset. This interface is permitted to be enabled when both the PC Card socket and PC Card installed in the socket support the I/O interface. The host configures a PC Card for the I/O interface using the Configuration Option register. PC Cards which support the I/O interface must indicate their support in the CIS on the card.
I/O Mapped	A storage location or register is I/O mapped when it is available to be accessed using I/O cycles. The register or storage location might also be accessible using memory cycles, in which case it would also be memory mapped.
IDE	Acronym for Integrated Drive Electronics. Disk storage devices with IDE are often referred to as ATA drives.
idle state	Any clock period that the bus is idle (**CFRAME#** and **CIRDY#** are deasserted).
IEEE	Acronym for the Institute for Electrical and Electronic Engineers
IEEE 1394	A high-speed serial bus that supports both arbitrated asynchronous communications and high-priority isochronous transmissions necessary for real-time full motion video and other high-speed data transfer.
Init. or Initialization	The state that a device must enter immediately following the Reset state. In this state, the device must allow access to its Configuration Space. It must draw a minimum current/power necessary for accessing its Configuration Space, and for the device initialization.
IREQ#	The Interrupt Request signal between a PC Card and a socket when the I/O interface is active.
IRQn	One of the Interrupt Request Signals between a socket and the host's CPU. Selection of the specific Interrupt Request Signal which is used to carry an Interrupt Request from a PC Card to the Host's CPU is controlled by hardware associated with the socket. Depending upon the host system implementation the IRQn signal may be either IRQn or IRQn#.
ISA	Acronym for Industry Standard Architecture. Refers to an IBM-compatible expansion bus of the type incorporated in IBM-AT compatible personal computers. Uses 16-bit addressing.
ISA Bus	Acronym for Industry Standard Architecture Bus. An internal host Bus that is available in some hosts and can be used to connect PC Card sockets to the host CPU. While serving the same basic purpose as a Micro Channel bus or an EISA bus, some bus protocols and signals are different. An ISA bus uses positive-true, edge sensitive, interrupt request lines (IRQn).
JEDEC	Acronym for Joint Electronic Device Engineering Council.
JEIDA	Acronym for Japan Electronic Industry Development Association.
JEITA	Acronym for Japan Electronic and Information Technology Industry Association
keepers	Another name for pull-up resistors that are only used to sustain a signal state.
latency	See access latency.
latency timer	A mechanism for ensuring that a bus master does not extend the access latency of other masters beyond a specified value.
LBA	Acronym for Logical Block Address.
legacy PCI devices	A class of devices built before the ***PCI Bus Power Management Interface Specification for PCI-to-CardBus Bridges*** was added to the ***PC Card Standard*** and are ***PC Card Standard, February 1995*** compliant. Legacy PCI to CardBus bridge and CardBus card devices are assumed to be in the ***D0*** power management state whenever power is applied to them.
Level Sensitive Interrupt	A host system interrupt based upon the logic level of the signal which causes repeated interrupts as long as the interrupt request signal is in the asserted state, and the interrupt request is not disabled. Used in Micro Channel Architecture bus hosts and available in EISA bus hosts.
LIM	Acronym for Lotus/Intel/Microsoft, commonly used to refer to an Expanded Memory Specification, for page swapping and memory management on DOS-based computers (LIM 4.0).
livelock	A condition in which two or more operations require completion of another operation before they can complete.
Logical Address	An address based on accessing the media in Logical Erase Unit order. See the ***Media Storgage Formats Specification***.
Logical Block Address	A logical block address is a sequential address for accessing the blocks on the storage media. The first block of the media is addressed as block 0 and succeeding blocks are numbered sequentially until the last block is encountered.
Logical Erase Unit Number (LogicalEUN)	A logical number assigned to an Erase Unit by the FTL. The FTL assigns logical numbers to Erase Units to remap the ordering of the physical media and simplify recovering superseded areas. See the ***Media Storage Formats Specification***.

LONGLINK	A LONGLINK is a pointer from one tuple chain to another. Such a link is described by one of the LONGLINK tuples: *CISTPL_LONGLINK_A*, *CISTPL_LONGLINK_C, CISTPL_LONGLINK_CB*. See ***Metaformat Specification***
Low (Logic Level)	A signal is in the low logic level when it is below or equal to the V_{IH} level. See the ***Electrical Specification*** for the precise electrical definition.
LSB	Acronym for Least Significant Bit and Least Significant Byte. That portion of a number, address or field that occurs rightmost when its value is written as a single number in conventional hexadecimal or binary notation. The portion of the number having the least weight in a mathematical calculation using the value.
Mandatory	A characteristic or feature that must be present in every implementation of the standard.
mapping	Associating a given card address space with a host system address space.
master	See Bus Master
master-abort	A termination mechanism that allows a master to terminate a transaction when no target responds.
Maximum Interface	A 7-position connector interface on the I/O Modem PC Card, connected to DAA. (See ***Guidelines***)
MBR	Acronym for Master Boot Record. An MBR is a specially formatted first physical sector on block storage media.
Media	Material used to store data. May be silicon, magnetic oxide or any other material that can retain information for later retrieval.
Medium Access Device	A device that provides access to a communications medium; in this instance through a Data Access Arrangement (Modem or Modem-FAX). (See ***Guidelines***)
memory area	An area of the card memory addressed by a memory handle. It may be part of a single memory region or span two or more memory regions.
Memory Cycle	A memory cycle is a memory-read operation (using Output Enable) or memory-write operation (using Write Enable) that accesses the PC Card's common memory or attribute memory address space.
memory handle	A Card Services-assigned identifier for a card memory area. Used to access memory on a card with the Card Services read, write, copy, and erase memory functions.
Memory Interface	The memory interface is the default interface after power up, PC Card Hardware Reset and PC Card Soft Reset for both PC Card cards and sockets. This interface supports memory operations only. Contrast with I/O interface.
Memory Mapped	A storage location or register is memory mapped when it is available to be accessed using memory cycles. The register or storage location might also be accessible using I/O cycles, in which case it would also be I/O mapped.
memory paging	A method of extending PC Card memory space to contain as many as 2^{42} Common Memory locations. Without memory paging, the 26 address signals at the PC Card connector allow 64Mbytes of Common Memory.
memory region	A homogeneous card memory area using one type of memory device.
Metaformat	Low level format standard of a PC Card.
Micro Channel	Micro Channel Architecture. Refers to an IBM expansion bus of the type incorporated in some of the personal computers in the PS/2 line. Features 32-bit addressing and bus-mastering capabilities. Not compatible with ISA or EISA. A Micro Channel Bus uses negative-true, level sensitive, interrupt request lines (IRQn#).
Minimum Interface	A 4-position connector interface on the I/O Modem PC Card, connected to DAA. (See ***Guidelines***)
motherboard	A circuit board containing the basic functions (e.g., CPU, memory, I/O, and expansion connectors) of a host system.
MSB	Acronym for Most Significant Bit and Most Significant Byte. That portion of a number, address or field that occurs leftmost when its value is written as a single number in conventional hexadecimal or binary notation. The portion of the number having the most weight in a mathematical calculation using the value.
MTD	Acronym for Memory Technology Driver. Embedded or installable component of Card Services that contains device-specific read, write, copy and erase algorithms.
Negated	A signal is negated when it is in the state opposed to that which is indicated by the name of the signal. See the Conventions section. Opposite of Asserted.
NMI	Acronym for Non-Maskable Interrupt (usually caused by a catastrophic error).

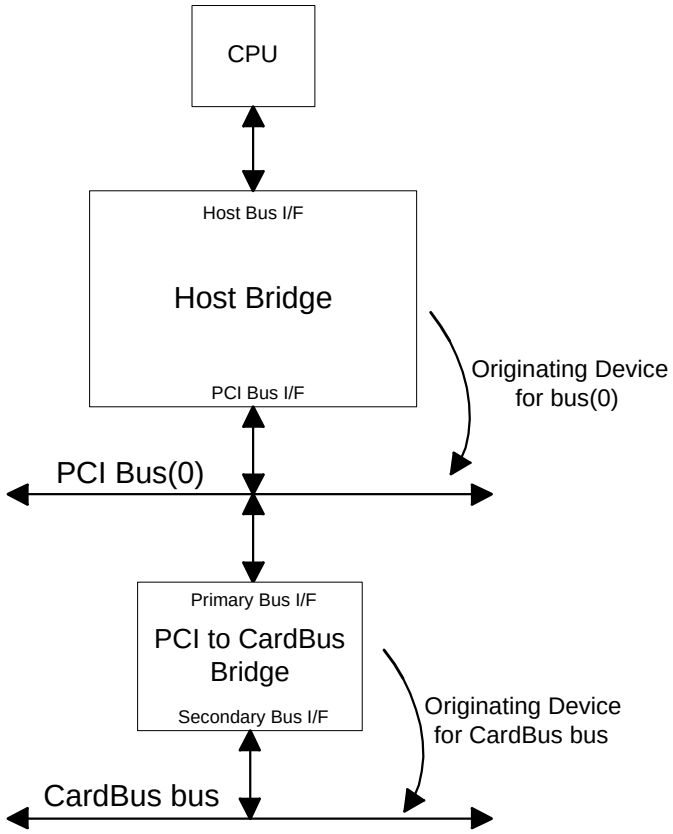
Offset The offset of a port or a memory location is the difference between the address of the specific port or memory address and the address of the first port or memory address within a contiguous group of ports or a memory window. This term is used when identifying the locations of registers located with respect to the base address of a block of contiguous I/O ports. It is also used when identifying the location of memory mapped registers with respect to the base address of the memory window.

Open System Cards Cards that contain selected I/O connectors and electrical-performance components, such that cables using connector plugs described herein can be used interchangeably with similar function cards regardless of supplier. (See ***Guidelines***)

Operating System Software on a host system that manages resources and provides services, including power management services, device drivers, user mode services, and/or kernel mode services.

optional A characteristic or feature that is not mandatory, but is specifically permitted. If an optional characteristic or feature is present, it must be implemented as described in this the ***PC Card Standard***. Optional characteristics or features are specifically identified.

originating device From the perspective of the operating system (Host CPU), the first bridge component encountered with a PCI bus downstream of it is defined as the Originating Device for that PCI bus segment. For a CardBus card, the originating device is the PCI to CardBus bridge controlling its bus (see figure below).



output driver An electrical drive element (transistor) for a single signal on a CardBus PC Card device.

page A subdivision of a 16-bit PC Card window. If there is more than one page in a window, all pages are 16 KBytes in size.

Paging See memory paging

partition A subdivision of a storage device, typically formatted for use with a single type of file system.

PC Acronym for Personal Computer. Often used to refer to an 80x86 based computer system.

PC Card A memory or I/O card compatible with the ***PC Card Standard***. When cards are referred to as PC Cards, what is being addressed are those characteristics common to both 16-bit PC Cards and CardBus PC Cards.

PC Card Hardware Reset PC Card Hardware Reset is caused when the socket asserts the RESET signal to the PC Card. During PC Card Hardware Reset, the PC Card interface is set to be the Memory Only Interface,

	and the Configuration Option register is set to 00H. Other configuration registers and the READY signal are also affected as detailed in the *PC Card Standard.*
PC Card Soft Reset	PC Card Soft Reset is caused when the host sets bit 7 of a PC Card's Configuration Option register. PC Card Soft Reset is asserted while bit 7 of Configuration Option register is set. The effect of PC Card Soft Reset is identical to the effect of PC Card Hardware Reset except that bit 7 of the Configuration Option register is not cleared by the reset condition. Because the other bits of the Configuration Option are written at the same time as the PC Card Soft Reset bit, it is recommended that the PC Card Soft Reset bit be cleared by writing a 00H to the Configuration Option register.
PC Card Standard	The ***PC Card Standard***. The applicable revision is given in the Related Documents section.
PCI	Acronym for the Peripheral Component Interface bus
PCI to CardBus bridge	PCI to CardBus bridges couple two independent buses together. They are characterized by a primary bus interface, and a secondary bus interface and are always a PCI bus and a CardBus card bus.
PCI device	A physical device consisting of one load on the PCI bus and having only one **IDSEL** input. This single PCI Device may contain up to 8 PCI Functions.
PCI or CardBus function	A set of functionality inside a PCI or CardBus Device represented by one 256-byte configuration space. Each PCI and CardBus function within a device generally has a separate software driver.
PCI Function Context	The variable data held by the PCI function, usually volatile. Function context refers to small amounts of information held internal to the function. Function Context is not limited only to the contents of the function's PCI registers, but rather refers also to the operational states of the function including state machine context, power state, execution stack (in some cases), etc. For a PCI to CardBus Bridge, the internal status and mask registers and the **Vcc** control signals would be a special case of Function Context that must be preserved.
PCMCIA	Acronym for the Personal Computer Memory Card International Association.
Peak Current	The highest averaged current value over any 10 millisecond period.
peer-to-peer	This term is used to describe data transfers between two agents that are both capable of gaining the bus mastership. It is used to specify the rules of changing the master/slave relationships between such agents.
phase	One or more clocks in which a single unit of information is transferred, consisting of: • an *address phase* (a single address transfer) • a *data phase* (one transfer state plus zero or more wait states)
Physical Address	An address based on accessing the media in Physical Erase Unit order. See the ***Media Storage Formats Specification***.
Physical Erase Unit Number (PhysicalEUN)	The number assigned to an Erase Unit based on its location on the physical media. This number never changes and is implied by the Erase Unit's position on the media. The Erase Unit at the beginning of an FTL partition is known as the First Physical Erase Unit. If the partition begins at physical address zero (0), the First Physical Erase Unit is number zero (0). See the ***Media Storage Formats Specification***.
Pin Replacement Register	The Pin Replacement register is the third Card Configuration register. It is used to retrieve status information from the PC Card about Battery, Busy and Write Protect while the card has the I/O interface active.
plug-n-play	An ability to insert and put into operation, or remove a PC Card without cycling the system power, re-booting the system, or requiring a manual user intervention for configuration.
PME Context	Power Management Event Context is defined as the functional state information and logic required to generate Power Management Events (PMEs), report PME status, and enable PMEs.
positive decoding	A method of address decoding in which a device responds to accesses only within an assigned address range. See also subtractive decoding.
POST	Acronym for Power-On Self Test. A series of diagnostic routines performed when a system is powered up.
power management	Mechanisms in software and hardware to minimize system power consumption, manage system thermal limits and maximize system battery life. Power management involves tradeoffs among system speed, noise, battery life, and AC power consumption.
Power Management Event (PME)	A power management event is the process by which a PCI or CardBus function can request a change of its power consumption state. Typically a device uses a PME to request a change from a power savings state to the fully operational (and fully powered) state. However, a device could use a PME to request a change to a lower power state. A power management event is requested via the assertion of the **PME#** signal for a PCI-to-CardBus Bridge, assertion of **CSTSCHG** for a CardBus card and **STSCHG#** for a PC Card. The power management policies of the system

	ultimately dictate what action is taken as a result of a power management event.
primary (ordinate) bus/side	The primary bus of a PCI to CardBus bridge or CardBus PC Card refers to the bus that is topologically closest to the CPU that is running the operating system.
Primary I/O Addresses	As applicable to PC Card ATA mass storage cards, it is the set of addresses 1F0H-1F7H and 3F6H-3F7H at which the first fixed disk controller is located in a PC/AT computer system. Use of these addresses allows emulation of the first ATA or IDE disk controller at its standard addresses.
Pull-ups	Resistors used to insure that signals maintain stable values when no agent is actively driving the bus.
Pulse Mode Interrupt	A method of transmitting an Interrupt Request from a PC Card to a socket using the **IREQ#** signal. In this mode, the **IREQ#** signal is asserted momentarily when the Card initiates an interrupt and is then negated regardless of whether or not the interrupt is acknowledged. The method of acknowledgment is specific to devices on the PC Card. In the case of a PC Card ATA mass storage card, acknowledgment takes place when the ATA Status register is read. The pulse mode interrupt is designed to be used with the ISA bus (and the EISA bus when ISA bus interrupt emulation is being performed). The host socket must use an "open-collector" non-inverting output to drive the ISA bus IRQn signal when it is expecting to share pulse mode interrupts from the PC Card.
Query Pins	Pins used in the CardBay PC Card interface to determine card functionality without energizing the card.
Read/Write Block	A subdivision of an Erase Unit. Used by the FTL to track media allocation. The FTL maintains the allocation state of each Read/Write Block. See the ***Media Storage Formats Specification***.
READY	When asserted, this signal Indicates that the PC Card is completely available for use. The negated state of the READY signal is used by a PC Card to indicate that it is busy with an internal operation and access to the card may be restricted. Refer to the ***Electrical Specification***, READY signal and RREADY bit for detailed information about this signal.
Region	See memory region.
Replacement Page	Values in a Replacement Page override values in the original page of the Virtual Map as follows: If an entry in an original page is zero (0), the logical address is retrieved from the corresponding entry on the Replacement Page. Replacement pages delay the need to reallocate a Page in the Virtual Map when an entry in the page is updated. See the ***Media Storage Formats Specification***.
Reset	Refers to the state of a bit within a register or variable. Reset is equivalent to off or zero(0). It is the device's default state after Power-up or reset.
restore time	Restore time is defined as the time required to fully restore a PCI or CardBus function to its fully operational state from a power saving mode of operation. It is measured as the total elapsed time between when the system software request for restoration occurs to when the function is fully configured and activated.
Retry	A directive to terminate the current transaction and retry it at a later time, also referred to as backoff.
RREADY	The Registered READY Status Bit, RREADY, is located in the Pin Replacement register if that register is present on the PC Card. The bit is provided to indicate the state of the READY function while the READY signal is unavailable because the Memory-Only Interface is not currently configured on the card.
secondary (subordinate) bus/side	The secondary bus of a PCI to CardBus bridge or CardBus PC Card refers to the bus that is topologically farthest from the CPU that is running the operating system.
Secondary I/O Addresses	As applicable to a PC Card ATA mass storage card, it is the set of addresses 170H-177H and 376H-377H at which the second fixed disk controller is located in a PC/AT computer system. Use of these addresses allows emulation of the second ATA or IDE disk controller at its standard addresses.
Sector	The smallest unit of information that may be stored on a block device. Typically 512 bytes, but may be other powers of two in size (128, 256, 1024, 2048, etc.).
Set	Refers to the state of a bit within a register or variable. Set is equivalent to on or one(1).
Shared memory	Any memory accessible by more than one agent.
Sideband signal	Any signal that is not part of the CardBus PC Card that connects two or more CardBus PC Card compliant agents, and has meaning only to those agents.
sleeping state	A computer state where the computer consumes a small amount of power, user mode threads are *not* being executed, and the system "appears" to be off (from an end user's perspective, the display is off, etc.). Latency for returning to the Working state varies on the wakeup environment selected prior to entry of this state (for example, should the system answer phone calls, etc.). Work can be resumed without rebooting the OS because large elements of system context are

	saved by the hardware with the rest saved by system software. It is not safe to disassemble the machine in this state.
Small PC Card	A PC Card form factor measuring 45.00 mm by 42.80 mm in various heights. The Small PC Card form factor does not support the CardBus interface.
Socket	The socket is the hardware, 68 pin socket, in the host which is responsible for accepting a PC Card into the host and mapping the host's internal bus signals to the PC Card interface signals.
Socket and Copy Register	The Socket and Copy register is the fourth Card Configuration register located on a PC Card. One use of this Configuration register allows the host to configure a PC Card ATA mass storage card to respond as either Drive 0 or Drive 1.
soft off state	A computer state where the computer consumes a minimal amount of power. No user mode or system mode code is run. This state requires a large latency in order to return to the ***Working*** state. The system's context will not be preserved by the hardware. The system must be restarted to return to the ***Working*** state. It is not safe to disassemble the machine.
Special Cycle	A message broadcast mechanism for communicating processor status and/or (optionally) logical sideband signaling between CardBus PC Card agents.
SRAM	Acronym for Static Random Access Memory.
SRST (Soft Reset Bit)	The ATA Soft Reset Bit, SRST, is located in the Device Control register of a PC Card ATA mass storage card. This bit provides the ATA Soft Reset Function but does not cause the PC Card interface to perform PC Card Reset processing.
Static Current	The highest averaged current value over any 1 second period while the card is in its lowest power state.
Status Changed Signal (STSCHG#)	The Status Changed Signal is present at the PC Card interface only when the I/O Interface is enabled. It is asserted when any of the four Changed Status bits in the Pin Replacement register are set while the Enable Status Changed bit is set in the Card Configuration and Status register. This signal replaces the BVD1 signal of the Memory-Only interface when the I/O Interface is configured.
stepping	The ability of an agent to spread assertion of qualified signals over several clocks.
subtractive decoding	A method of address decoding in which a device accepts all accesses not positively decoded by other agents. See also positive decoding.
system bus arbiter	A function which controls access to the system bus.
system master	An agent or a group of agents which controls system configuration and resource management. This is the same as host from the CardBus PC Card point of view.
system software	Includes Socket Services, Card Services and generic enablers.
target	An agent that responds (with a positive acknowledgment by asserting **CDEVSEL#**) to a bus transaction initiated by a master.
target abort	A termination mechanism that allows a target to terminate a transaction in which a catastrophic error has occurred, or to which the target will never be able to respond.
target latency	The third component of access latency - the amount of time that the target takes to assert **CTRDY#** for the first data transfer.
Task File Registers	In obsolete versions of the ***ATA Specification***, ATA Command Block registers were referred to as the Task File. See Command Block registers.
termination	A transaction termination brings the bus transaction to an orderly and systematic conclusion. All transactions are concluded when **CFRAME#** and **CIRDY#** are deasserted (an idle cycle). Termination may be initiated by the master or the target.
Thermal Rating	A number representing the heat generated by PC Cards (see the ***Physical Specification***) or the ability of PC Card hosts to remove heat (see the ***PC Card Host System Specification***).
Track	Group of sectors all accessed by a single head on one cylinder of a rotating media storage device.
transaction	An address phase plus one or more data phases.
transfer state	Any CardBus PC Card clock, during a data phase, in which data is transferred.
Transfer Unit	An Erase Unit reserved for storing Read/Write Blocks from an Erase Unit being emptied by the FTL prior to erasure. Transfer Units are not included in the formatted size of the FTL partition presented to the host file system. See the ***Media Storage Formats Specification***.
Tuple	A tuple is an element of a Card Information Structure. Each tuple has a tuple code which identifies the type of tuple which is present, a tuple length which specifies the amount of space occupied by the tuple, and an information area which contains the content of the tuple. Tuples located in the CIS of a PC Card are examined by host software to determine the capabilities of the card.

tuple chain	A linked set of tuples which is parsed completely before any LONGLINK is followed to another tuple chain. There is at most one LONGLINK per tuple chain.
tuple parsing	The action performed by a client whereby a CIS is interpreted into configuration requests and other useful information.
tuple traversal	Locating and reading in sequence all of the tuples on the card. This action is best performed by Card Services for a client. This is also referred to as "tuple walking" or "walking the CIS."
turnaround cycle	A CardBus PC Card cycle used to prevent contention when one agent stops driving a signal and another agent begins. A turnaround cycle must last one clock and is required on all signals that may be driven by more than one agent.
Twin Cards	An optional field in a Configuration Entry tuple that permits configurations to be described in which several cards share the same system resources such as I/O ports. The cards are uniquely labeled by the host using the Copy Number field of the Socket and Copy register. For PC Card ATA, this feature is used to permit a Drive 0 and a Drive 1 to coexist at the same Primary or Secondary I/O addresses. Support for the Twin Cards Option is optional in PC Card ATA mass storage cards.
Universal Serial Bus	A serial bus standard which allows operation at 12 Mbps with a low speed un-shielded sub-channel operating at 1.5 Mbps, and offers both asynchronous and isochronous data transfer.
USB	See Universal Serial Bus
User	Within this document, the term “user” refers to the user of Card Services, typically a higher-level software layer such as a client, and not the end-user of the host computer.
Virtual Address	The address recorded in a Read/Write Block's allocation information representing where the stored data appears in the virtual image presented to the host system. See the ***Media Storage Formats Specification***.
Virtual Block	The unit of information used by the file system layer above the FTL to read and write data to the media. The FTL uses Virtual Block sizes that are a logical power of two of 128 bytes or larger. The Virtual Block size is set when the FTL partition is formatted.
Virtual Block Map (VBM)	An array of 32-bit entries used to map a Virtual Block number to a logical address on the media. Space is always reserved on the media to store the entire VBM. The FirstVMAddress field describes how much of the VBM is maintained on the media by the FTL.
Virtual Page Map (VPM)	An array of 32-bit entries used to map Pages of the Virtual Block Map to a logical address on the media. The VPM is never stored on the media.
wait state	A CardBus PC Card clock, during a data phase, in which no transfer occurs.
Wakeup Event	An event which can be enabled to wake the system from a ***Sleeping*** or ***Soft Off*** state to a Working state to allow some task to be performed.
Window	An area in a host computer's memory or I/O port space through which a PC Card may be addressed.
working state	A computer state where the system dispatches user mode (application) threads and they execute. In this state, devices (peripherals) are dynamically having their power state changed. The user will be able to select (through some user interface) various performance/power characteristics of the system to have the software optimize for performance or battery life. The system responds to external events in real time. It is not safe to disassemble the machine in this state.
X86	Any of a number of CPU chips compatible with the Intel iAPX8086, the Intel iAPX80286, the Intel iAPX80386, the Intel iAPX80486, or the Intel Pentium.
XIP	Acronym for eXecute-In-Place. Refers to specification for directly executing code from a PC Card.
Zoomed Video Port	A PC Card Custom Interface which provides a single-source uni-directional video bus between a PC Card socket and a VGA controller.
ZV Port	See Zoomed Video Port