REALTEK GIGABIT ETHERNET MEDIA ACCESS CONTROLLER WITH POWER MANAGEMENT RTL8169

1. Features

- 208 pin QFP
- Supports descriptor-based buffer management
- Supports Microsoft* NDIS5 Checksum Offloads (IP, TCP, UDP), and Largesend Offload
- Supports IEEE 802.1Q VLAN tagging
- Supports Transmit (Tx) Priority Queue for QoS, CoS applications
- Supports major Tally Counters
- 10Mbps, 100Mbps, and 1000Mbps operation at MII/GMII, and 1000Mbps at TBI interfaces
- Supports 10Mbps, 100Mbps, and 1000Mbps N-way Auto-negotiation operation
- PCI local bus single-chip Fast Ethernet controller
  - ✧ Compliant to PCI Revision 2.2
  - ✧ Supports both Little-Endian and Big-Endian
  - ✧ Supports 16.75MHz-66MHz PCI clock
  - ✧ Supports both 32-bit and 64-bit PCI bus
  - ✧ Supports PCI target fast back-to-back transaction
  - ✧ Supports Memory Read Line, Memory Read Multiple, Memory Write and Invalidate, and Dual Address Cycle
  - ✧ Provides PCI bus master data transfers and PCI memory space or I/O space mapped data transfers of the RTL8169 operational registers
  - ✧ Supports PCI VPD (Vital Product Data)
  - ✧ Supports ACPI, PCI power management
  - ✧ Supports optional PCI multi-function with additional slave mode only functions
- Supports CardBus. The CIS can be stored in 93C56 or expansion ROM
- Supports Boot ROM interface. Up to 128K bytes Boot ROM interface for both EPROM and Flash memory can be supported
- Supports 125MHz OSC as the internal clock source or 125MHz clock provided from external PHYceiver
- Compliant to PC97, PC98, PC99 and PC2001 standards
- Supports Wake-On-LAN function and remote wake-up (Magic Packet*, LinkChg and Microsoft® wake-up frame)
- Supports 4 Wake-On-LAN (WOL) signals (active high, active low, positive pulse, and negative pulse)
- Supports auxiliary power-on internal reset, to be ready for remote wake-up when main power still remains off
- Supports auxiliary power auto-detect, and sets the related capability of power management registers in PCI configuration space
- Advanced power saving mode when LAN function or wakeup function is not used
- 3.3V and 1.8V power supplies needed
- 5V tolerant I/Os
- Includes a programmable, PCI burst size and early Tx/Rx threshold
- Supports a 32-bit general-purpose timer with the external PCI clock as clock source, to generate timer-interrupt
- Contains two large independent transmit (8KB) and receive (48KB) FIFO devices
- Uses 93C46 (64*16-bit EEPROM) or 93C56 (128*16-bit EEPROM) to store resource configuration, ID parameter, and VPD data. The 93C56 can also be used to store the CIS data structure for CardBus applications
- Supports LED pins for various network activity indications
- Supports both digital and external analog loopback
- Half/Full duplex capability (only Full duplex operation at 1000Mbps)
- Supports Full Duplex Flow Control (IEEE 802.3x)

* Third-party brands and names are the property of their respective owners.

These specifications are subject to change without notice.

2. General Description

The Realtek RTL8169 is a highly integrated, high performance PCI Gigabit Ethernet Media Access Controller for use in network adapters for servers and personal computers. The RTL8169 fully implements the 33/66MHz, 32/64-bit PCI v2.2 bus interface for host communications with power management and is compliant with the IEEE 802.3 specification for 10/100Mbps Ethernet and the IEEE 802.3z specification for 1000Mbps Ethernet. The RTL8169 supports the auxiliary power auto-detect function, and will auto-configure related bits of the PCI power management registers in PCI configuration space.

It also supports the Advanced Configuration Power management Interface (ACPI), PCI power management for modern operating systems that are capable of Operating System directed Power Management (OSPM) to achieve the most efficient power management system possible.

In addition to the ACPI feature, the RTL8169 also supports remote wake-up (including AMD Magic Packet, LinkChg, and Microsoft® wake-up frame) in both ACPI and APM environments. The RTL8169 is capable of performing an internal reset through the application of auxiliary power. When the auxiliary power is applied and the main power remains off, the RTL8169 is ready and waiting for the Magic Packet or Link Change to wake the system up. Also, the LWAKE pin provides four different output signals including active high, active low, positive pulse, and negative pulse. The versatility of the RTL8169 LWAKE pin provides motherboards with Wake-On-LAN (WOL) functionality.

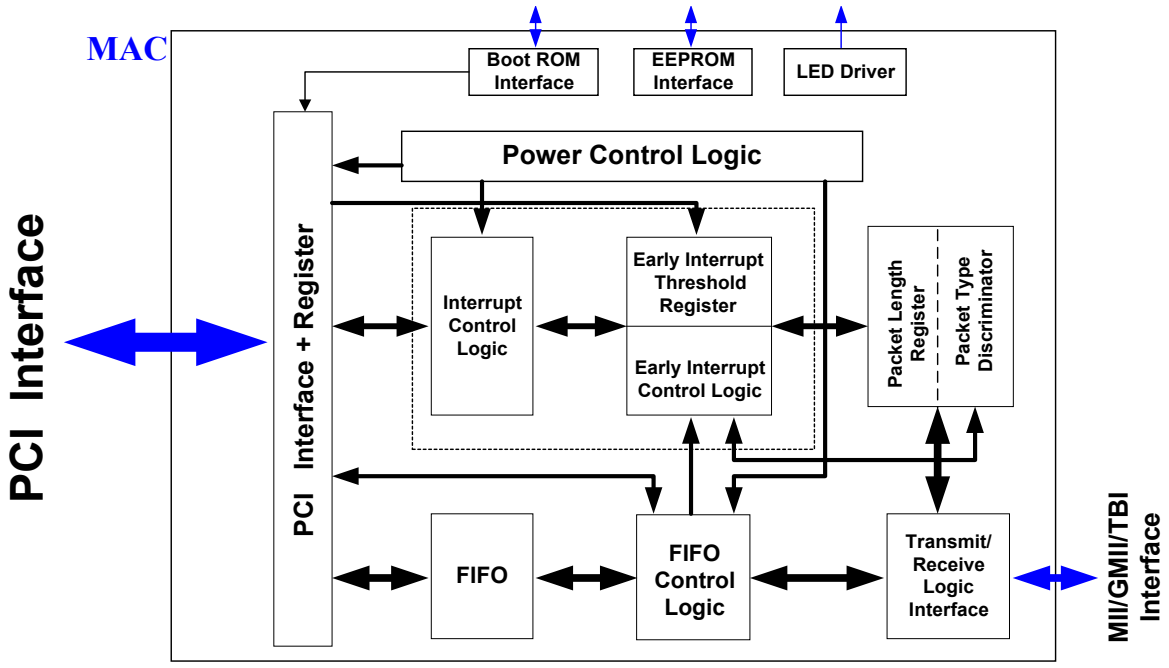
The PCI specification is inherently little-endian. The RTL8169 contains the ability to do little-endian to big-endian swaps. It is also possible that the RTL8169 can be used as a basis for a RISC CPU platform which expect the data to be in a big-endian format. This feature allows for maximum flexibility.

PCI Vital Product Data (VPD) is also supported to provide the information that uniquely identifies hardware (i.e., the RTL8169 LAN card). The information may consist of part number, serial number, and other detailed information.

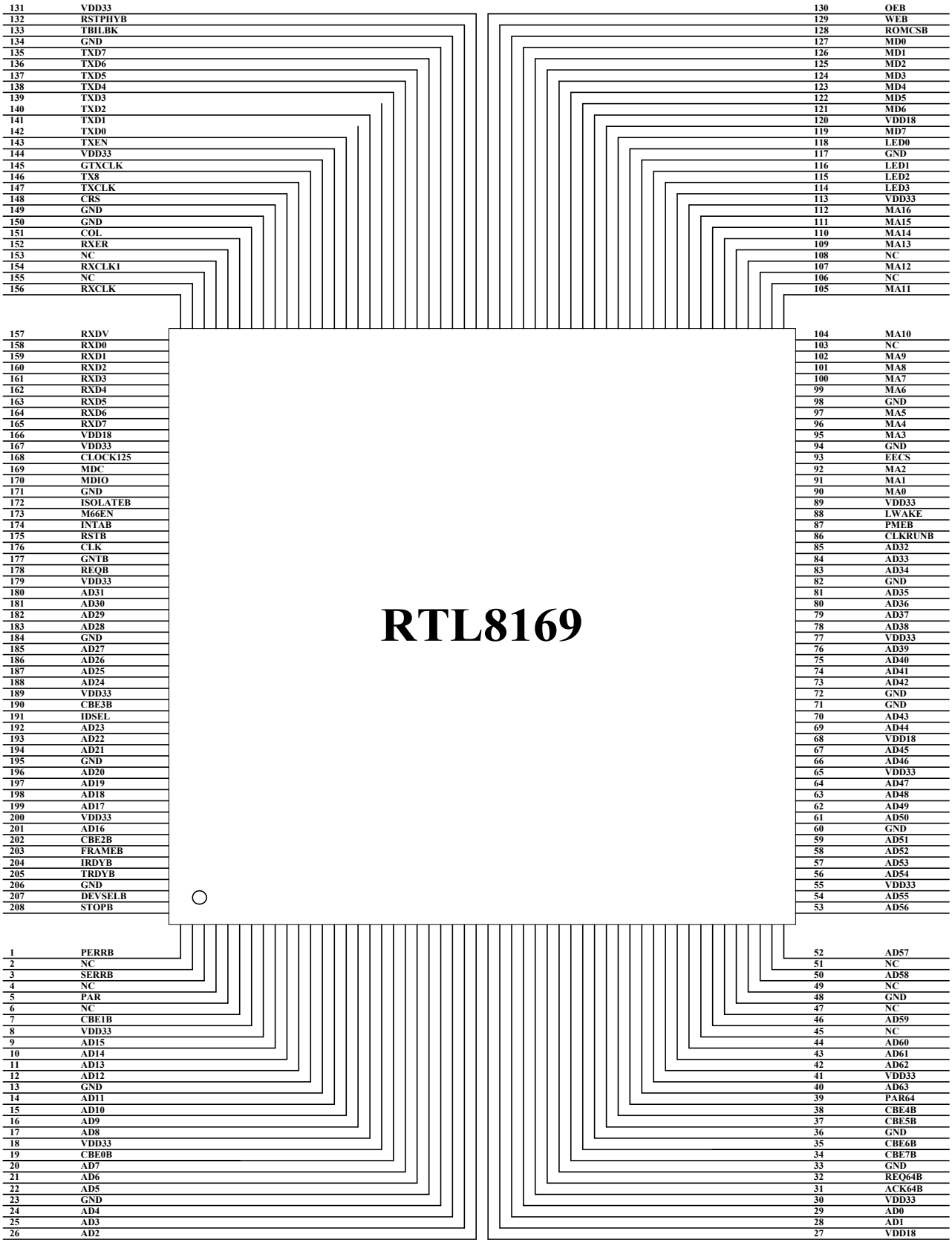
The RTL8169 is fully compliant to Microsoft® NDIS5 (IP, TCP, UDP) Checksum and Segmentation Task-offload features, and supports IEEE802.1Q Virtual bridged Local Area Network (VLAN). All the above RTL8169 features contribute to lowering CPU utilization, which is a benefit in operation as a server network card. Also, the RTL8169 boosts its PCI performance by supporting PCI Memory Read Line & Memory Read Multiple when transmitting, and Memory Write and Invalidate when receiving. To be better qualified as a server card, the RTL8169 also supports the PCI Dual Address Cycle (DAC) command, when the assigned buffers reside at a physical memory addresses higher than 4 Gigabytes. For QoS, CoS requirements, the RTL8169 supports hardware high priority queues to reduce software implementation effort and significantly improve performance.

The RTL8169 keeps network maintenance costs low and eliminates usage barriers. It is the easiest way to upgrade a network from 10/100Mbps to 1000Mbps. It also supports full-duplex operation, making possible 2000Mbps of bandwidth at no additional cost. For special applications, the RTL8169 also supports a TBI interface, which can be used to provide a connection to a Fiber channel, using a Fiber transceiver.

3. Block Diagram



4. Pin Assignments



5. Pin Description

In order to reduce pin count, and therefore size and cost, some pins have multiple functions. In those cases, the functions are separated with a "/" symbol. Refer to the Pin Assignment diagram for a graphical representation.

5.1 Power Management/Isolation Interface

Symbol	Type	Pin No	Description
PMEB (PME#)	O/D	87	**Power Management Event:** Open drain, active low. Used by the RTL8169 to request a change in its current power management state and/or to indicate that a power management event has occurred.
ISOLATEB (ISOLATE#)	I	172	**Isolate Pin:** Active low. Used to isolate the RTL8169 from the PCI bus. The RTL8169 does not drive its PCI outputs (excluding PME#) and does not sample its PCI input (including RST# and PCICLK) as long as the Isolate pin is asserted.
LWAKE/ CSTSCHG	O	88	**LAN WAKE-UP Signal** (When CardB_En=0, bit2 Config3)**:** This signal is used to inform the motherboard to execute the wake-up process. The motherboard must support Wake-On-LAN (WOL). There are 4 choices of output, including active high, active low, positive pulse, and negative pulse, that may be asserted from the LWAKE pin. Please refer to LWACT bit in CONFIG1 register and LWPTN bit in CONFIG4 register for the setting of this output signal. The default output is an active high signal. Once a PME event is received, the LWAKE and PMEB assert at the same time when the LWPME (bit4, CONFIG4) is set to 0. If the LWPME is set to 1, the LWAKE asserts only when the PMEB asserts and the ISOLATEB is low. **CSTSCHG Signal** (When CardB_En=1, bit2 Config3)**:** This signal is used in CardBus applications only and is used to inform the motherboard to execute the wake-up process whenever a PME event occurs. This is always an active high signal, and the setting of LWACT (bit 4, Config1), LWPTN (bit2, Config4), and LWPME (bit4, Config4) means nothing in this case. This pin is a 3.3V signaling output pin.

5.2 PCI Interface

Symbol	Type	Pin No	Description
AD63-0	T/S	40, 42-44, 46, 50, 52-54, 56-59, 61-64, 66-67, 69-70, 73-76, 78-81, 83-85, 180-183, 185-188, 192-194, 196-199, 201, 9-12, 14-17, 20-22, 24-26, 28-29	**AD31-0: Low 32-bit PCI address and data multiplexed pins.** The address phase is the first clock cycle in which FRAMEB is asserted. During the address phase, AD31-0 contains a physical address (32 bits). For I/O, this is a byte address, and for configuration and memory, it is a double-word address. The RTL8169 supports both big-endian and little-endian byte ordering. Write data is stable and valid when IRDYB is asserted. Read data is stable and valid when TRDYB is asserted. Data I is transferred during those clocks where both IRDYB and TRDYB are asserted. **AD63-32: High 32-bit PCI address and data multiplexed pins.** During an address phase (when using the DAC command or when REQ64B is asserted), the upper 32-bits of a 64-bit address are transferred; otherwise, these bits are reserved, and are stable and indeterminate. During a data phase, an additional 32-bits of data are transferred when a 64-bit transaction has been negotiated by the assertion of REQ64B and ACK64B.
C/BE7-0B	T/S	34-35, 37-38, 190, 202, 7, 19	**PCI bus command and byte enables multiplexed pins.** During the address phase of a transaction, C/BE3-0 define the bus command. During the data phase, C/BE3-0 are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. C/BE0 applies to byte 0, and C/BE3 applies to byte 3. During an address phase (when using DAC commands or when REQ64B is asserted), the actual bus command is transferred on C/BE7-4; otherwise, these bits are reserved and indeterminate. During a data phase, C/BE7-4 are Byte Enables indicating which byte lanes carry meaningful data when a 64-bit transaction has been negotiated by the assertion of REQ64B and ACK64B. C/BE4 applies to byte 4 and C/BE7 applies to byte 7.
CLK	I	176	**PCI clock:** This clock input provides timing for all PCI transactions and is input to the PCI device. Supports up to a 66MHz PCI clock.
CLKRUNB	I/O	86	**Clock Run:** This signal is used by the RTL8169 to request starting (or speeding up) the clock, CLK. CLKRUNB also indicates the clock status. For the RTL8169, CLKRUNB is an open drain output as well as an input. The RTL8169 requests the central resource to start, speed up, or maintain the interface clock by the assertion of CLKRUNB. For the host system, it is an S/T/S signal. The host system (central resource) is responsible for maintaining CLKRUNB asserted, and for driving it high to the negated (deasserted) state.
DEVSELB	S/T/S	207	**Device Select:** As a bus master, the RTL8169 samples this signal to insure that a PCI target recognizes the destination address for the data transfer. As a target, the RTL8169 asserts this signal low when it recognizes its target address after FRAMEB is asserted.
FRAMEB	S/T/S	203	**Cycle Frame:** As a bus master, this pin indicates the beginning and duration of an access. FRAMEB is asserted low to indicate the start of a bus transaction. While FRAMEB is asserted, data transfer continues. When FRAMEB is deasserted, the transaction is in the final data phase. As a target, the device monitors this signal before decoding the address to check if the current transaction is addressed to it.

cont...

GNTB	I	177	**Grant:** This signal is asserted low to indicate to the RTL8169 that the central arbiter has granted the ownership of the bus to the RTL8169. This input is used when the RTL8169 is acting as a bus master.
ACK64B	S/T/S	31	**Acknowledge 64-bit Transfer:** This signal is asserted low by the device that has positively decoded its address as the target of the current access, indicates the target is willing to transfer data using 64 bits. ACK64B has the same timing as DEVSELB.
REQB	T/S	178	**Request:** The RTL8169 will assert this signal low to request the ownership of the bus from the central arbiter.
REQ64B	S/T/S	32	**Request 64-bit Transfer:** The RTL8169 asserts this signal low to indicate that it wants to perform a 64-bit data transfer. If the RTL8169 sees the REQ64B asserted on the rising edge of PCI RSTB, the RTL8169 is on 64-bit slot and is capable of 64-bit transaction. Otherwise, the RTL8169 is on 32-bit slot.
IDSEL	I	191	**Initialization Device Select**: This pin allows the RTL8169 to identify when configuration read/write transactions are intended for it.
INTAB	O/D	174	**Interrupt A:** Used to request an interrupt. It is asserted low when an interrupt condition occurs, as defined by the Interrupt Status, Interrupt Mask.
IRDYB	S/T/S	204	**Initiator Ready**: This indicates the initiating agent's ability to complete the current data phase of the transaction. As a bus master, this signal will be asserted low when the RTL8169 is ready to complete the current data phase transaction. This signal is used in conjunction with the TRDYB signal. Data transaction takes place at the rising edge of CLK when both IRDYB and TRDYB are asserted low. As a target, this signal indicates that the master has put data on the bus.
TRDYB	S/T/S	205	**Target Ready:** This indicates the target agent's ability to complete the current phase of the transaction. As a bus master, this signal indicates that the target is ready for the data during write operations and with the data during read operations. As a target, this signal will be asserted low when the (slave) device is ready to complete the current data phase transaction. This signal is used in conjunction with the IRDYB signal. Data transaction takes place at the rising edge of CLK when both IRDYB and TRDYB are asserted low.
PAR	T/S	5	**Parity:** This signal indicates even parity across AD31-0 and C/BE3-0 including the PAR pin. PAR is stable and valid one clock after each address phase. For data phase, PAR is stable and valid one clock after either IRDYB is asserted on a write transaction or TRDYB is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. As a bus master, PAR is asserted during address and write data phases. As a target, PAR is asserted during read data phases.
PAR64	T/S	39	**Parity Upper Double Word:** This signal indicates even parity across AD63-32 and C/BE7-4 including the PAR64 pin. PAR64 is valid one clock after each address phase on any transaction in which REQ64B is asserted. PAR64 is stable and valid for 64-bit data phase one clock after either IRDYB is asserted on a write transaction or TRDYB is asserted on a read transaction. As a bus master, PAR64 is asserted during address and write data phases. As a target, the RTL8169 only supports 32-bit transfers, so it will not assert PAR64.

cont...

M66EN	I	173	**66MHZ_ENABLE:** This pin indicates to the RTL8169 whether the bus segment is operating at 66 or 33MHz. When this pin (active high) is asserted, the current PCI bus segment that the RTL8169 resides on operates in 66-MHz mode. If this pin is deasserted, the current PCI bus segment operates in 33-MHz mode.
PERRB	S/T/S	1	**Parity Error:** This pin is used to report data parity errors during all PCI transactions except a Special Cycle. PERRB Is driven active (low) two clocks after a data parity error is detected by the device receiving data, and the minimum duration of PERRB is one clock for each data phase with parity error detected.
SERRB	O/D	3	**System Error:** If an address parity error is detected and Configuration Space Status register bit 15 (detected parity error) is enabled, the RTL8169 asserts the SERRB pin low and bit 14 of Status register in Configuration Space.
STOPB	S/T/S	208	**Stop:** Indicates that the current target is requesting the master to stop the current transaction.
RSTB	I	175	**Reset:** When RSTB is asserted low, the RTL8169 performs an internal system hardware reset. RSTB must be held for a minimum of 120 ns periods.

5.3 FLASH/BootPROM/EEPROM/MII Interface

Symbol	Type	Pin No	Description
MA[16:9], MA7, MA[5:3]	O	112-109, 107, 105-104, 102, 100, 97-95	**Boot PROM Address Bus:** These pins are used to access up to a 128k-byte flash memory or EPROM. **MA16-3:** Output pins to the Boot PROM address bus.
MA8	O, I	101	**MA8:** Input pin as Aux. Power detect pin to detect if Aux. Power exists or not, when initial power-on. Besides connecting this pin to Boot PROM, it should be pulled high to the Aux. Power via a resistor to detect Aux. power. If this pin is not pulled high to Aux. Power, the RTL8169 assumes that no Aux. power exists. To support wakeup from ACPI D3cold or APM power-down, this pin must be pulled high to aux. power via a resistor.
MA6	O, I	99	**MA6/9356SEL:** Input pin as 9356 select pin at initial power-up. When this pin is pulled high with a 10KΩ resistor, the 93C56 EEPROM is used to store the resource data and CIS for the RTL8169. The RTL8169 latches the status of this pin at power-up to determine what EEPROM (93C46 or 93C56) is used, afterwards, this pin is used as MA6
MA2/EESK	O	92	**MA2-0:** The MA2-0 pins are switched to EESK, EEDI, EEDO in 93C46 (93C56) programming or auto-load mode.
MA1/EEDI	O	91	
MA0/EEDO	O, I	90	
EECS	O	93	**EEPROM Chip Select:** 93C46 (93C56) chip select
MD7-0	I/O	119, 121-127	Boot PROM data bus during Boot PROM mode.
ROMCSB	O	128	**ROM Chip Select:** This is the chip select signal of the Boot PROM.
OEB	O	130	**Output Enable:** This enables the output buffer of the Boot PROM or Flash memory during a read operation.
WEB	O	129	**Write Enable:** This signal strobes data into the Flash memory during a write cycle.

5.4 LED Interface

<table>
<tr><th>Symbol</th><th>Type</th><th>Pin No</th><th>Description</th></tr>
<tr><td>LED3-0</td><td>O</td><td>114-116, 118</td><td>LED pins (Active low)
1000BaseT mode:
<table>
<tr><th>LEDS1-0</th><th>00</th><th>01</th><th>10</th><th>11</th></tr>
<tr><td>LED0</td><td>Tx/Rx</td><td>ACT(Tx/Rx)</td><td>Tx</td><td>LINK10/ACT</td></tr>
<tr><td>LED1</td><td>LINK100</td><td>LINK10/100/1000</td><td>LINK10/100/1000</td><td>LINK100/ACT</td></tr>
<tr><td>LED2</td><td>LINK10</td><td>FULL</td><td>Rx</td><td>FULL</td></tr>
<tr><td>LED3</td><td>LINK1000</td><td>-</td><td>FULL</td><td>LINK1000/ACT</td></tr>
</table>
TBI mode:
<table>
<tr><th>LEDS1-0</th><th>00</th><th>01</th><th>10</th><th>11</th></tr>
<tr><td>LED0</td><td>ACT</td><td>ACT</td><td>Tx</td><td>-</td></tr>
<tr><td>LED1</td><td>-</td><td>LINK</td><td>LINK</td><td>-</td></tr>
<tr><td>LED2</td><td>-</td><td>FULL</td><td>Rx</td><td>FULL</td></tr>
<tr><td>LED3</td><td>LINK</td><td>-</td><td>FULL</td><td>LINK</td></tr>
</table>
During power down mode, the LED signals are logic high.</td></tr>
</table>

5.5 GMII, TBI, PHY CP

Gigabit Media Independent Interface, Ten Bit Interface, PHY Control Pin

Symbol	Type	Pin No	Description
GTxCLK	O	145	**Gigabit Tx clock:** In GMII mode (1000Mbps Tx clock), GTxCLK is a continuous clock used for operation at 1000Mbps. GTxCLK provides the timing reference for the transfer of the TxEN, TxER, and TxD signals. The values of TxEN, TxER, and TxDs are sampled by the PHY on the rising edge of GTxCLK. In GMII mode or TBI mode, the GTxCLK can be used as a 125MHz reference clock, and it used as the 125MHz transmit clock to an external PMD and is the reference for transmit TBI signaling.
TxCLK	I	147	**Transmit Clock (MII mode only):** TxCLK is a continuous clock that provides a timing reference for the transfer of TxD[3:0], TxEN. In MII mode, it uses the 25MHz or 2.5MHz supplied by the external PMD device.
TxEN/ Tx[9]	O	143	**Transmit Enable:** In GMII mode (or MII mode), the assertion of TxEN indicates that the RTL8169 is presenting data on the GMII (or MII) for transmission. TxEn is asserted synchronously with the first octet (or nibble) of the preamble and remains asserted while all octets (or nibbles) to be transmitted are presented to the GMII (or MII). This signal is synchronous to TxCLK and provides precise framing for data carried on TXD3-0/TXD7-0 for the external PMD. It is asserted when TXD3-0/TXD7-0 contains valid data to be transmitted. **Tx[9]:** In TBI mode, Tx[9] is the MSB of the 10-bit vector representing one transmission code-group. Tx[0] is the first bit to be transmitted, and Tx[9] is the last bit to be transmitted.
Tx[8]	O	146	**Tx[8] (TBI mode only):** In TBI mode, Tx[8] is one of the 10-bit vector representing one transmission code-group.

cont...

TxD[7:0]/ Tx[7:0]	O	135-142	**Transmit Data:** In GMII mode, TxD[7:0] is a bundle of eight data signals, representing a data byte on GMII for PHY to transmit. In MII mode, only TxD[3:0] represent a data nibble on MII for PHY to transmit. TxD[7:0] or TxD[3:0] transition synchronously with respect to GTxCLK or TxCLK. **Tx[7:0]:** In TBI mode, TxD[7:0] is part of the 10-bit vector (TxD[9:0]) representing one transmission code-group.
RxCLK/ RxCLK0	I	156	**Receive Clock(0):** RxCLK: In GMII mode or MII mode, the receive clock is a continuous clock that provides the timing reference for the transfer of the RxDV, RxER, and RxD from PHY device. RxDV, RxER, and RxD are sampled on the rising edge of RxCLK. **RxCLK0:** In TBI mode, the 62.5MHz receive clock is a continuous clock and provides timing reference for the RTL8169 to latch odd-numbered receive code-groups from PHY device.
RxCLK1	I	154	**Receive Clock1:** RxCLK1: In TBI mode, the 62.5MHz receive clock is a continuous clock and provides timing reference for the RTL8169 to latch even-numbered receive code-groups from PHY device.
RxER/ Rx[9]	I	152	**Receive Coding Error:** In GMII or MII mode, this pin is asserted synchronously with respect to RxCLK, to indicate that the PHY device detected a symbol that is not part of the valid data or delimiter set somewhere in the frame being received. The RxER may be asserted for one or more clock cycles. **Rx[9]:** In TBI mode, Rx[9] is the MSB of the 10-bit vector representing one receive code-group. Rx[0] is the first bit received, and Rx[9] is the last bit received.
RxDV/ Rx[8]	I	157	**Receive Data Valid:** In GMII or MII mode, this input pin is asserted synchronously with respect to RxCLK, to indicate that the PHY is presenting recovered, decoded, and valid data to the RTL8169. RxDV remains asserted while valid data is being presented by the PHY. **Rx[8]:** In TBI mode, Rx[8] is a bit of the 10-bit vector representing one receive code-group. Rx[0] is the first bit received, and Rx[9] is the last bit received.
RxD[7:0]/ Rx[7:0]	I	165-158	**Receive Data:** In GMII mode, RxD[7:0] is a bundle of eight data signals, representing a data byte transmitted from PHY to the RTL8169 on GMII. In MII mode, only RxD[3:0] represent a data nibble transmitted from PHY to the RTL8169 on MII. RxD[7:0] or RxD[3:0] transition synchronously with respect to RxCLK. **Rx[7:0]:** In TBI mode, RxD[7:0] is part of the 10-bit vector (RxD[9:0]) representing one receive code-group.
COL	I	151	**Collision Detected:** In GMII or MII mode, this input pin is asserted high by PHY to indicate the detection of a collision on the twisted pair medium, and remains asserted while the collision condition persists. In full duplex mode, this pin's status is ignored by the RTL8169. The COL transitions asynchronously with respect to RxCLK, GTxCLK, or TxCLK. In TBI mode, this pin's status is ignored by the RTL8169.

cont...

CRS	I	148	**Carrier Sense:** In GMII or MII mode, this pin is asserted high by the GMII/MII PHY device whenever the transmit or receive medium is not idle, and is deasserted when both transmit and receive media are idle. The CRS remains asserted throughout the duration of a collision condition. The CRS transitions asynchronously with respect to RxCLK, GTxCLK, or TxCLK. In TBI mode, this pin's status is ignored by the RTL8169.
MDC	O	169	**Management Data Clock:** In GMII or MII mode, it is a synchronous clock to the MDIO management data input/output serial interface (about 3.125MHz) which may be asynchronous to transmit and receive clocks. In TBI mode, this pin is a reserved pin.
MDIO	I/O	170	**Management Data Input/Output:** Bi-directional signal used to transfer or receive control and status information from the PHY device. MDIO is driven and sampled synchronously with respect to MDC. In TBI mode, this pin is a reserved pin.
TBILBK	O	133	**TBI LoopBack:** The RTL8169 asserts this pin high when the TBI is in loopback mode.
RSTPHYB	O	132	**PHY Reset pin:** An active low signal used by the RTL8169 to force hardware reset to external PHYceiver at initial power-on.

5.6 Clock and NC Pins

Symbol	Type	Pin No	Description
Clock125	I	168	**125MHz clock input:** The 125MHz reference clock for the RTL8169 comes from either external PHYceiver or 125MHz OSC.
NC	-	2, 4, 6, 45, 47, 49, 51, 103, 106, 108, 153, 155,	**Reserved**

5.7 Power Pins

Symbol	Type	Pin No	Description
VDD33	P	8, 18, 30, 41, 55, 65, 77, 89, 113, 131, 144, 167, 179, 189, 200	**+3.3V**
VDD18	P	27, 120, 68, 166	**+1.8V**
GND	P	13, 23, 36, 48, 60, 71, 82, 98, 117, 134, 150, 171, 184, 195, 206, 33, 94, 72, 149	**Ground**

6. Register Descriptions

The RTL8169 provides the following set of operational registers mapped into PCI memory space or I/O space.

Offset	R/W	Tag	Description
0000h	R/W	IDR0	**ID Register 0:** The ID registers 0-5 are only permitted to write by 4-byte access. Read access can be byte, word, or double word access. The initial value is autoloaded from EEPROM EthernetID field.
0001h	R/W	IDR1	**ID Register 1**
0002h	R/W	IDR2	**ID Register 2**
0003h	R/W	IDR3	**ID Register 3**
0004h	R/W	IDR4	**ID Register 4**
0005h	R/W	IDR5	**ID Register 5**
0006h-0007h	-	-	**Reserved**
0008h	R/W	MAR0	**Multicast Register 0:** The MAR registers 0-7 are only permitted to write by 4-bye access. Read access can be byte, word, or double word access. Driver is responsible for initializing these registers.
0009h	R/W	MAR1	**Multicast Register 1**
000Ah	R/W	MAR2	**Multicast Register 2**
000Bh	R/W	MAR3	**Multicast Register 3**
000Ch	R/W	MAR4	**Multicast Register 4**
000Dh	R/W	MAR5	**Multicast Register 5**
000Eh	R/W	MAR6	**Multicast Register 6**
000Fh	R/W	MAR7	**Multicast Register 7**
0010h-0017h	R/W	DTCCR	**Dump Tally Counter Command Register** (64-byte alignment)
0018h-001Fh	-	-	**Reserved**
0020h-0027h	R/W	TNPDS	**Transmit Normal Priority Descriptors**: Start address (64-bit). (256-byte alignment)
0028h-002Fh	R/W	THPDS	**Transmit High Priority Descriptors:** Start address (64-bit). (256-byte alignment)
0030h-0033h	R/W	FLASH	**Flash memory read/write register**
0034h-0035h	R	ERBCR	**Early Receive (Rx) Byte Count Register**
0036h	R	ERSR	**Early Rx Status Register**
0037h	R/W	CR	**Command Register**
0038h	W	TPPoll	**Transmit Priority Polling register**
0039h-003Bh	-	-	**Reserved**
003Ch-003Dh	R/W	IMR	**Interrupt Mask Register**
003Eh-003Fh	R/W	ISR	**Interrupt Status Register**
0040h-0043h	R/W	TCR	**Transmit (Tx) Configuration Register**
0044h-0047h	R/W	RCR	**Receive (Rx) Configuration Register**
0048h-004Bh	R/W	TCTR	**Timer CounT Register:** This register contains a 32-bit general-purpose timer. Writing any value to this 32-bit register will reset the original timer and begin the count from zero.
004Ch-004Fh	R/W	MPC	**Missed Packet Counter:** This 24-bit counter indicates the number of packets discarded due to Rx FIFO overflow. After a s/w reset, MPC is cleared. Only the lower 3 bytes are valid. When any value is written to MPC, it will be reset.
0050h	R/W	9346CR	**93C46 (93C56) Command Register**
0051h	R/W	CONFIG0	**Configuration Register 0**
0052h	R/W	CONFIG1	**Configuration Register 1**
0053h	R/W	CONFIG2	**Configuration Register 2**
0054h	R/W	CONFIG3	**Configuration Register 3**

cont...

0055h	R/W	CONFIG4	**Configuration Register 4**
0056h	R/W	CONFIG5	**Configuration Register 5**
0057h	-	-	**Reserved**
0058h-005Bh	R /W	TimerInt	**Timer Interrupt Register:** Once having written a nonzero value to this register, the Timeout bit of ISR register will be set whenever the TCTR reaches to this value. The Timeout bit will never be set as long as TimerInt register is zero.
005Ch-005Dh	R/W	MULINT	**Multiple Interrupt Select**
005Eh-005Fh	-	-	**Reserved**
0060h-0063h	R/W	PHYAR	**PHY Access Register**
0064h-0067h	R/W	TBICSR0	**TBI Control and Status Register**
0068h-0069h	R/W	TBI_ANAR	**TBI Auto-Negotiation Advertisement Register**
006Ah-006Bh	R	TBI_LPAR	**TBI Auto-Negotiation Link Partner Ability Register**
006Ch	R	PHYStatus	**PHY(GMII, MII, or TBI) Status Register**
006Dh-0081h	-	-	**Reserved**
0082-0083h	-	-	**Reserved**
0084h–008Bh	R/W	Wakeup0	**Power Management wakeup frame0 (64bit)**
008Ch–0093h	R/W	Wakeup1	**Power Management wakeup frame1 (64bit)**
0094h–009Bh	R/W	Wakeup2LD	**Power Management wakeup frame2 (128bit), low D-Word**
009Ch–00A3h	R/W	Wakeup2HD	**Power Management wakeup frame2, high D-Word**
00A4h–00ABh	R/W	Wakeup3LD	**Power Management wakeup frame3 (128bit), low D-Word**
00ACh–00B3h	R/W	Wakeup3HD	**Power Management wakeup frame3, high D-Word**
00B4h–00BBh	R/W	Wakeup4LD	**Power Management wakeup frame4 (128bit), low D-Word**
00BCh–00C3h	R/W	Wakeup4HD	**Power Management wakeup frame4, high D-Word**
00C4h-00C5h	R/W	CRC0	**16-bit CRC of wakeup frame 0**
00C6h-00C7h	R/W	CRC1	**16-bit CRC of wakeup frame 1**
00C8h-00C9h	R/W	CRC2	**16-bit CRC of wakeup frame 2**
00CAh-00CBh	R/W	CRC3	**16-bit CRC of wakeup frame 3**
00CCh-00CDh	R/W	CRC4	**16-bit CRC of wakeup frame 4**
00CEh-00D9h	-	-	**Reserved**
00DAh-00DBh	R/W	RMS	**Rx packet Maximum Size**
00DCh-00DFh	-	-	**Reserved**
00E0h-00E1h	R/W	C+CR	**C+ Command Register**
00E2h-00E3h	-	-	**Reserved**
00E4h-00EBh	R/W	RDSAR	**Receive Descriptor Start Address Register (256-byte alignment)**
00ECh	R/W	ETThR	**Early Transmit Threshold Register**
00EDh-00EFh	-	-	**Reserved**
00F0h-00F3h	R/W	FER	**Function Event Register (Cardbus only)**
00F4h-00F7h	R/W	FEMR	**Function Event Mask Register (CardBus only)**
00F8h-00FBh	R	FPSR	**Function Present State Register (CardBus only)**
00FCh-00FFh	W	FFER	**Function Force Event Register (CardBus only)**

6.1 DTCCR: Dump Tally Counter Command (Offset 0010h-0017h, R/W)

<table>
<tr><th>Bit</th><th>R/W</th><th>Symbol</th><th>Description</th></tr>
<tr><td>63:6</td><td>R/W</td><td>CntrAddr</td><td>Starting address of the 12 Tally Counters being dumped to. (64-byte alignment address, 64 bytes long)
<table>
<tr><th>Offset of starting address</th><th>Counter</th><th>Description</th></tr>
<tr><td>0</td><td>TxOk</td><td>64-bit counter of Tx Ok packets.</td></tr>
<tr><td>8</td><td>RxOk</td><td>64-bit counter of Rx Ok packets.</td></tr>
<tr><td>16</td><td>TxER</td><td>64-bit packet counter of Tx errors including Tx abort, carrier lost, Tx underrun, and out of window collision.</td></tr>
<tr><td>24</td><td>RxEr</td><td>32-bit packet counter of Rx errors including CRC error packets (should be larger than 8 bytes) and missed packets.</td></tr>
<tr><td>28</td><td>MissPkt</td><td>16-bit counter of missed packets (CRC Ok) resulted from Rx FIFO full.</td></tr>
<tr><td>30</td><td>FAE</td><td>16-bit counter of Frame Alignment Error packets (MII mode only)</td></tr>
<tr><td>32</td><td>Tx1Col</td><td>32-bit counter of those Tx Ok packets with only 1 collision happened before Tx Ok.</td></tr>
<tr><td>36</td><td>TxMCol</td><td>32-bit counter of those Tx Ok packets with more than 1, and less than 16 collisions happened before Tx Ok.</td></tr>
<tr><td>40</td><td>RxOkPhy</td><td>64-bit counter of all Rx Ok packets with physical address matched destination ID.</td></tr>
<tr><td>48</td><td>RxOkBrd</td><td>64-bit counter of all Rx Ok packets with broadcast destination ID.</td></tr>
<tr><td>56</td><td>RxOkMul</td><td>32-bit counter of all Rx Ok packets with multicast destination ID.</td></tr>
<tr><td>60</td><td>TxAbt</td><td>16-bit counter of Tx abort packets.</td></tr>
<tr><td>62</td><td>TxUndrn</td><td>16-bit counter of Tx underrun and discard packets (only possible on jumbo frames).</td></tr>
</table></td></tr>
<tr><td>5:4</td><td>-</td><td>-</td><td>Reserved</td></tr>
<tr><td>3</td><td>R/W</td><td>Cmd</td><td>Command: When set, the RTL8169 begins dumping 13 Tally counters to the address specified above.
When this bit is reset by the RTL8169, the dumping has been completed.</td></tr>
<tr><td>2:0</td><td>-</td><td>-</td><td>Reserved</td></tr>
</table>

6.2 FLASH: Flash Memory Read/Write (Offset 0030h-0033h, R)

Bit	R/W	Symbol	Description
31:24	R/W	MD7-MD0	**Flash Memory Data Bus:** These bits set and reflect the state of the MD7 - MD0 pins during the write and read process respectively.
23:21	-	-	Reserved
20	W	ROMCSB	**Chip Select:** This bit sets the state of the ROMCSB pin.
19	W	OEB	**Output Enable:** This bit sets the state of the OEB pin.
18	W	WEB	**Write Enable:** This bit sets the state of the WEB pin.
17	W	SWRWEn	**Enable software access to flash memory:** 1: Enable read/write access to flash memory via software and disable the EEPROM access during flash memory access via software. 0: Disable read/write access to flash memory via software.
16:0	W	MA16-MA0	**Flash Memory Address Bus:** These bits set the state of the MA16-0 pins.

6.3 ERSR: Early Rx Status (Offset 0036h, R)

Bit	R/W	Symbol	Description
7:4	-	-	**Reserved**
3	R	ERGood	**Early Rx Good packet:** This bit is set whenever a packet is completely received and the packet is good. Writing a '1' will clear this bit.
2	R	ERBad	**Early Rx Bad packet:** This bit is set whenever a packet is completely received and the packet is bad. Writing a '1' will clear this bit.
1	R	EROVW	**Early Rx OverWrite:** This bit is set when the RTL8169's local address pointer is equal to CAPR. In the early mode, this is different from buffer overflow. It happens when the RTL8169 detects an Rx error and wants to fill another packet data from the beginning address of that error packet. Writing a '1' will clear this bit.
0	R	EROK	**Early Rx OK:** The power-on value is 0. It is set when the Rx byte count of the arriving packet exceeds the Rx threshold. After the whole packet is received, the RTL8169 will set ROK or RER in ISR and clear this bit simultaneously. Setting this bit will invoke a ROK interrupt.

6.4 Command (Offset 0037h, R/W)

Bit	R/W	Symbol	Description
7:5	-	-	**Reserved**
4	R/W	RST	**Reset:** Setting this bit to 1 forces the RTL8169 into a software reset state which disables the transmitter and receiver, reinitializes the FIFOs, and resets the system buffer pointer to the initial value (the start address of each descriptor group set in TNPDS, THPDS and RDSAR registers). The values of IDR0-5, MAR0-7 and PCI configuration space will have no changes. This bit is 1 during the reset operation, and is cleared to 0 by the RTL8169 when the reset operation is complete.
3	R/W	RE	**Receiver Enable**
2	R/W	TE	**Transmit Enable**
1:0	-	-	**Reserved**

6.5 TPPoll: Transmit Priority Polling (Offset 0038h, R/W)

Bit	R/W	Symbol	Description
7	W	HPQ	**High Priority Queue polling:** Writing a '1' to this bit will notify the RTL8169 that there is a high priority packet(s) waiting to be transmitted. The RTL8169 will clear this bit automatically after all high priority packets have been transmitted. Writing a '0' to this bit has no effect.
6	W	NPQ	**Normal Priority Queue polling:** Writing a '1' to this bit will notify the RTL8169 that there is a normal priority packet(s) waiting to be transmitted. The RTL8169 will clear this bit automatically after all normal priority packets have been transmitted. Writing a '0' to this bit has no effect.
5:1	-	-	**Reserved**
0	W	FSWInt	**Forced Software Interrupt:** Writing a '1' to this bit will trigger an interrupt, and the SWInt bit (bit8, ISR, offset3Eh-3Fh) will set. The RTL8169 will clear this bit automatically after the SWInt bit (bit8, ISR) is cleared. Writing a '0' to this bit has no effect.

6.6 Interrupt Mask (Offset 003Ch-003Dh, R/W)

Bit	R/W	Symbol	Description
15	R/W	SERR	**System Error Interrupt:** 1: Enable; 0: Disable.
14	R/W	TimeOut	**Time Out Interrupt:** 1: Enable; 0: Disable.
13:10	-	-	**Reserved**
9	-	-	**Reserved**
8	R/W	SWInt	**Software Interrupt:** 1: Enable; 0: Disable.
7	R/W	TDU	**Tx Descriptor Unavailable Interrupt:** 1: Enable; 0: Disable.
6	R/W	FOVW	**Rx FIFO Overflow Interrupt:** 1: Enable; 0: Disable.
5	R/W	PUN/LinkChg	**Packet Underrun/Link Change Interrupt:** 1: Enable; 0: Disable.
4	R/W	RDU	**Rx Buffer Overflow/Rx Descriptor Unavailable Interrupt:** 1: Enable; 0: Disable.
3	R/W	TER	**Tx Error Interrupt:** 1: Enable; 0: Disable.
2	R/W	TOK	**Tx Ok:** Transmit (Tx) OK: Indicates that a packet transmission is completed successfully. 1: Enable; 0: Disable.
1	R/W	RER	**Rx Error Interrupt:** 1: Enable; 0: Disable.
0	R/W	ROK	**Rx OK Interrupt:** 1: Enable; 0: Disable.

6.7 Interrupt Status (Offset 003Eh-003Fh, R/W)

Bit	R/W	Symbol	Description
15	R/W	SERR	**System Error:** This bit is set to 1 when the RTL8169 signals a system error on the PCI bus.
14	R/W	TimeOut	**Time Out:** This bit is set to 1 when the TCTR register reaches the value of the TimerInt register.
13:10	-	-	**Reserved**
9	-	-	**Reserved**
8	R/W	SWInt	**Software Interrupt:** This bit is set to 1 whenever a '1' is written by software to FSWInt (bit0, offset D9h, TPPoll register).
7	R/W	TDU	**Tx Descriptor Unavailable:** When set, this bit indicates that the Tx descriptor is unavailable.
6	R/W	FOVW	**Rx FIFO Overflow:** This bit set to 1 is caused by RDU, poor PCI performance, or overloaded PCI traffic.
5	R/W	PUN/LinkChg	**Packet Underrun/Link Change:** This bit is set to 1 when CAPR is written but the Rx buffer is empty, or when link status is changed.
4	R/W	RDU	**Rx Descriptor Unavailable:** When set to 1, this bit indicates that the Rx descriptor is unavailable. The MPC (Missed Packet Counter, offset 4Ch-4Fh) indicates the number of packets discarded after Rx FIFO overflowed.
3	R/W	TER	**Transmit (Tx) Error:** This bit set to 1 indicates that a packet transmission was aborted, due to excessive collisions, according to the TXRR's setting in the TCR register.
2	R/W	TOK	**Transmit (Tx) OK:** When set to 1, this bit indicates that a packet transmission has been completed successfully.
1	R/W	RER	**Receive (Rx) Error:** When set to 1, this bit indicates that a packet has either a CRC error or a frame alignment error (FAE). A Rx error packet of CRC error is determined according to the setting of RER8, AER, AR bits in RCR register (offset 44h-47h).
0	R/W	ROK	**Receive (Rx) OK:** In normal mode, this bit set to 1 indicates the successful completion of a packet reception. In early mode, this bit set to 1 indicates that the Rx byte count of the arriving packet exceeds the early Rx threshold.

- Writing 1 to any bit in the ISR will reset that bit.

6.8 Transmit Configuration (Offset 0040h-0043h, R/W)

<table>
<tr><th>Bit</th><th>R/W</th><th>Symbol</th><th>Description</th></tr>
<tr><td>31</td><td>-</td><td>-</td><td>Reserved</td></tr>
<tr><td>30:26</td><td>R</td><td>HWVERID0</td><td>Hardware Version ID0:
<table>
<tr><th></th><th>Bit30</th><th>Bit29</th><th>Bit28</th><th>Bit27</th><th>Bit26</th><th>Bit23</th></tr>
<tr><td>RTL8139</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>RTL8139A</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>RTL8139A-G</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>RTL8139B</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>RTL8130</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>RTL8139C</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>RTL8139C+</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>RTL8100</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>RTL8169</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Reserved</td><td colspan="6">All other combination</td></tr>
</table></td></tr>
<tr><td>25:24</td><td>R/W</td><td>IFG1, 0</td><td>InterFrameGap Time: This field allows adjustment of the interframe gap time to be longer than the standards of 9.6 µs for 10Mbps, 960 ns for 100Mbps, and 96 ns for 1000Mbps. The time can be programmed from 9.6 µs to 14.4 µs (10Mbps), 960ns to 1440ns (100Mbps), and 96ns to 144ns (1000Mbps).

The setting of the inter frame gap is:
<table>
<tr><th colspan="3">IFG[2:0]</th><th>IFG@1000MHz (ns)</th><th>IFG@100MHz (ns)</th><th>IFG@10MHz (µs)</th></tr>
<tr><td>0</td><td>1</td><td>1</td><td>96</td><td>960</td><td>9.6</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>96 + 8</td><td>960 + 8 * 10</td><td>9.6 + 8 * 0.1</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>96 + 16</td><td>960 + 16 * 10</td><td>9.6 + 16 * 0.1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>96 + 24</td><td>960 + 24 * 10</td><td>9.6 + 24 * 0.1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>96 + 48</td><td>960 + 48 * 10</td><td>9.6 + 48 * 0.1</td></tr>
</table>
-Other values are reserved.</td></tr>
<tr><td>23</td><td>R</td><td>HWVERID1</td><td>Hardware Version ID1: Please see HWVERID0.</td></tr>
<tr><td>22:20</td><td></td><td>-</td><td>Reserved</td></tr>
<tr><td>19</td><td>R/W</td><td>IFG2</td><td>InterFrameGap2</td></tr>
<tr><td>18:17</td><td>R/W</td><td>LBK1, LBK0</td><td>Loopback test: There will be no packets on the (G)MII or TBI interface in Digital loopback mode, provided the external phyceiver is also set in loopback mode. The digital loopback function is independent of the current link status.

For analog loopback tests, software must force the external phyceiver into loopback mode while the RTL8169 operates normally.

00 : Normal operation
01 : Digital loopback mode
10 : Reserved
11 : Reserved</td></tr>
<tr><td>16</td><td>R/W</td><td>CRC</td><td>Append CRC: Setting this bit to 1 means that there is no CRC appended at the end of a packet. Setting to 0 means that there is a CRC appended at the end of a packet.</td></tr>
<tr><td>15:11</td><td>-</td><td>-</td><td>Reserved</td></tr>
</table>

cont...

10:8	R/W	MXDMA2, 1, 0	**Max DMA Burst Size per Tx DMA Burst:** This field sets the maximum size of transmit DMA data bursts according to the following table: 000 = 16 bytes 001 = 32 bytes 010 = 64 bytes 011 = 128 bytes 100 = 256 bytes 101 = 512 bytes 110 = 1024 bytes 111 = Unlimited
7:0	-	-	**Reserved**

★ The TCR register can only be changed after having set TE (bit2, Command register, offset 0037h).

6.9 Receive Configuration (Offset 0044h-0047h, R/W)

Bit	R/W	Symbol	Description
31:25	-	-	**Reserved**
24	R/W	MulERINT	**Multiple Early Interrupt Select:** When this bit is set to 1, any received packets invoke an early interrupt according to the MULINT<MISR[11:0]> setting in early mode.
23:17	-	-	**Reserved**
16	R/W	RER8	When this bit is set to 1, the RTL8169 will calculate the CRC of any received packed with a length larger than 8 bytes. When this bit is cleared, the RTL8169 only calculates the CRC of any received packet with a length larger than 64-bytes. The power-on default is zero. If AER or AR is set, the RTL8169 always calculates the CRC of any incoming packet with a packet length larger than 8 bytes. The RER8 is in a "Don't care" state in this situation.
15:13	R/W	RXFTH2, 1, 0	**Rx FIFO Threshold:** Specifies the Rx FIFO Threshold level. When the number of the received data bytes from a packet, which is being received into the Rx FIFO of the RTL8169, has reached this level (or the FIFO contains a complete packet), the receive PCI bus master function will begin to transfer the data from the FIFO to the host memory. This field sets the threshold level according to the following table: 000 = Reserved 001 = Reserved 010 = 64 bytes 011 = 128 bytes 100 = 256 bytes 101 = 512 bytes 110 = 1024 bytes 111 = no Rx threshold. The RTL8169 begins the transfer of data after having received a whole packet in the FIFO.
12:11	-	-	**Reserved**

cont...

10:8	R/W	MXDMA2, 1, 0	**Max DMA Burst Size per Rx DMA Burst:** This field sets the maximum size of the receive DMA data bursts according to the following table: 000 = Reserved 001 = Reserved 010 = 64 bytes 011 = 128 bytes 100 = 256 bytes 101 = 512 bytes 110 = 1024 bytes 111 = Unlimited
7	-	-	**Reserved**
6	R	9356SEL	This bit reflects what type of EEPROM is used. 1: The EEPROM used is 9356. 0: The EEPROM used is 9346.
5	R/W	AER	**Accept Error Packet:** When set to 1, all packets with CRC error, alignment error, and/or collided fragments will be accepted. When set to 0, all packets with CRC error, alignment error, and/or collided fragments will be rejected.
4	R/W	AR	**Accept Runt:** This bit set to 1 allows the receiver to accept packets that are smaller than 64 bytes. The packet must be at least 8 bytes long to be accepted as a runt.
3	R/W	AB	**Accept Broadcast Packets:** 1: Accept, 0: Reject
2	R/W	AM	**Accept Multicast Packets:** 1: Accept, 0: Reject
1	R/W	APM	**Accept Physical Match Packets:** 1: Accept, 0: Reject
0	R/W	AAP	**Accept All Packets with Destination Address:** 1: Accept, 0: Reject

6.10 9346CR: 93C46 (93C56) Command (Offset 0050h, R/W)

<table>
<tr><th>Bit</th><th>R/W</th><th>Symbol</th><th>Description</th></tr>
<tr><td>7:6</td><td>R/W</td><td>EEM1-0</td><td>Operating Mode: These 2 bits select the RTL8169 operating mode.
<table>
<tr><th>EEM1</th><th>EEM0</th><th>Operating Mode</th></tr>
<tr><td>0</td><td>0</td><td>Normal (RTL8169 network/host communication mode)</td></tr>
<tr><td>0</td><td>1</td><td>Auto-load: Entering this mode will make the RTL8169 load the contents of the 93C46 (93C56) as when the RSTB signal is asserted. This auto-load operation will take about 2 ms. Upon completion, the RTL8169 automatically returns to normal mode (EEM1 = EEM0 = 0) and all of the other registers are reset to default values.</td></tr>
<tr><td>1</td><td>0</td><td>93C46 (93C56) programming: In this mode, both network and host bus master operations are disabled. The 93C46 (93C56) can be directly accessed via bit3-0 which now reflect the states of EECS, EESK, EEDI, & EEDO pins respectively.</td></tr>
<tr><td>1</td><td>1</td><td>Config register write enable: Before writing to CONFIGx registers, the RTL8169 must be placed in this mode. This will prevent RTL8169 configurations from accidental change.</td></tr>
</table></td></tr>
<tr><td>5:4</td><td>-</td><td>-</td><td>Reserved</td></tr>
<tr><td>3</td><td>R/W</td><td>EECS</td><td rowspan="4">These bits reflect the state of the EECS, EESK, EEDI & EEDO pins in auto-load or 93C46 (93C56) programming mode and are valid only when the Flash bit is cleared.
Note: EESK, EEDI and EEDO is valid after boot ROM complete.</td></tr>
<tr><td>2</td><td>R/W</td><td>EESK</td></tr>
<tr><td>1</td><td>R/W</td><td>EEDI</td></tr>
<tr><td>0</td><td>R</td><td>EEDO</td></tr>
</table>

6.11 CONFIG 0 (Offset 0051h, R/W)

<table>
<tr><th>Bit</th><th>R/W</th><th>Symbol</th><th>Description</th></tr>
<tr><td>7:3</td><td>-</td><td>-</td><td>Reserved</td></tr>
<tr><td>2-0</td><td>R</td><td>BS2, BS1, BS0</td><td>Select Boot ROM Size
<table>
<tr><th>BS2</th><th>BS1</th><th>BS0</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>No Boot ROM</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>8K Boot ROM</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>16K Boot ROM</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>32K Boot ROM</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>64K Boot ROM</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>128K Boot ROM</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>unused</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>unused</td></tr>
</table></td></tr>
</table>

6.12 CONFIG 1 (Offset 0052h, R/W)

<table>
<tr><th>Bit</th><th>R/W</th><th>Symbol</th><th>Description</th></tr>
<tr><td>7:6</td><td>R/W</td><td>LEDS1-0</td><td>Refer to the LED PIN definition. These bits initial value com from 93C46/93C56.</td></tr>
<tr><td>5</td><td>R/W</td><td>DVRLOAD</td><td>Driver Load: Software maybe use this bit to make sure that the driver has been loaded. Writing 1 is 1. Writing 0 is 0. When the command register bits IOEN, MEMEN, BMEN of PCI configuration space are written, the RTL8169 will clear this bit automatically.</td></tr>
<tr><td>4</td><td>R/W</td><td>LWACT</td><td>LWAKE Active Mode: The LWACT bit and LWPTN bit in CONFIG4 register are used to program the LWAKE pin’s output signal. According to the combination of these two bits, there may be 4 choices of LWAKE signal, i.e., active high, active low, positive (high) pulse, and negative (low) pulse. The output pulse width is about 150 ms. In CardBus application, the LWACT and LWPTN have no meaning.

The default value of each of these two bits is 0, i.e., the default output signal of LWAKE pin is an active high signal.
<table>
<tr><th colspan="2" rowspan="2">LWAKE output</th><th colspan="2">LWACT</th></tr>
<tr><th>0</th><th>1</th></tr>
<tr><td rowspan="2">LWPTN</td><td>0</td><td>Active high*</td><td>Active low</td></tr>
<tr><td>1</td><td>Positive pulse</td><td>Negative pulse</td></tr>
</table>
* Default value.</td></tr>
<tr><td>3</td><td>R</td><td>MEMMAP</td><td>Memory Mapping: The operational registers are mapped into PCI memory space.</td></tr>
<tr><td>2</td><td>R</td><td>IOMAP</td><td>I/O Mapping: The operational registers are mapped into PCI I/O space.</td></tr>
<tr><td>1</td><td>R/W</td><td>VPD</td><td>Vital Product Data: Set to enable Vital Product Data. The VPD data is stored in 93C46 or 93C56 from within offset 40h-7Fh.</td></tr>
<tr><td>0</td><td>R/W</td><td>PMEn</td><td>Power Management Enable:
Writable only when 93C46CR register EEM1=EEM0=1

Let A denote the New_Cap bit (bit 4 of the Status Register) in the PCI Configuration space offset 06h.
Let B denote the Cap_Ptr register in the PCI Configuration space offset 34h.
Let C denote the Cap_ID (power management) register in the PCI Configuration space offset 0DCh.
Let D denote the power management registers in the PCI Configuration space offset from 0DDh to 0E1h.
Let E denote the Next_Ptr (power management) register in the PCI Configuration space offset 0DDh.

PMEn setting:
0: A=B=C=E=0, D is invalid
1: A=1, B=0DCh, C=01h, D is valid, E is valid and depends on whether VPD is enabled or not.</td></tr>
</table>

6.13 CONFIG 2 (Offset 0053h, R)

Bit	R/W	Symbol	Description
7:5	-	-	**Reserved**
4	R	Aux_Status	**Auxiliary Power Present Status:** 1: The Aux. Power is present. 0: The Aux. Power is absent. The value of this bit is fixed after each PCI reset.
3	R	PCIBusWidth	**PCI Bus Width:** 1: 64-bit slot 0: 32-bit slot
2:0	R	PCICLKF2-0	**PCI clock frequency:** PCICLKF2-0 / MHz 000 / 33 001 / 66 Other values / Reserved

6.14 CONFIG 3 (Offset 0054h, R/W)

Bit	R/W	Symbol	Description
7	R	GNTSel	**Grant Select:** Select the Frame's asserted time after the Grant signal has been asserted. The Frame and Grant are the PCI signals. 1: delay one clock from GNT assertion. 0: No delay
6	-	-	**Reserved**
5	R/W	Magic	**Magic Packet:** This bit is valid when the PWEn bit of CONFIG1 register is set. The RTL8169 will assert the PMEB signal to wakeup the operating system when the Magic Packet is received. Once the RTL8169 has been enabled for Magic Packet wakeup and has been put into an adequate state, it scans all incoming packets addressed to the node for a specific data sequence, which indicates to the controller that this is a Magic Packet frame. A Magic Packet frame must also meet the basic requirements: Destination address + Source address + data + CRC The destination address may be the node ID of the receiving station or a multicast address, which includes the broadcast address. The specific sequence consists of 16 duplications of 6 byte ID registers, with no breaks or interrupts. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream, 6 bytes of FFh. The device will also accept a multicast address, as long as the 16 duplications of the IEEE address match the address of the ID registers. If the Node ID is 11h 22h 33h 44h 55h 66h, then the format of the Magic frame looks like the following: Destination address + source address + MISC + FF FF FF FF FF FF + MISC + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + MISC + CRC

cont...

4	R/W	LinkUp	**Link Up:** This bit is valid when the PWEn bit of the CONFIG1 register is set. The RTL8169, in an adequate power state, will assert the PMEB signal to wakeup the operating system when the cable connection is reestablished.
3	R	CardB_En	**Card Bus Enable:** 1: Enable CardBus related registers and functions. 0: Disable CardBus related registers and functions.
2	R	CLKRUN_En	**CLKRUN Enable:** 1: Enable CLKRUN. 0: Disable CLKRUN.
1	R	FuncRegEn	**Functions Registers Enable (CardBus only):** 1: Enable the 4 Function Registers (Function Event Register, Function Event Mask Register, Function Present State Register, and Function Force Event Register) for CardBus application. 0: Disable the 4 Function Registers for CardBus application.
0	R	FBtBEn	**Fast Back to Back Enable:** 1: Enable; 0: Disable.

6.15 CONFIG 4 (Offset 0055h, R/W)

Bit	R/W	Symbol	Description
7:5	-	-	**Reserved**
4	R/W	LWPME	**LANWAKE vs PMEB:** 1: The LWAKE can only be asserted when the PMEB is asserted and the ISOLATEB is low. 0: The LWAKE and PMEB are asserted at the same time. In CardBus applications, this bit has no meaning.
3	-	-	**Reserved**
2	R/W	LWPTN	**LWAKE Pattern:** Please refer to the LWACT bit in CONFIG1 register.
1:0	-	-	**Reserved**

6.16 CONFIG 5
(Offset 0056h, R/W)

This register, unlike other Config registers, is not protected by 93C46 Command register. I.e. there is no need to enable the Config register write prior to writing to Config5.

Bit	R/W	Symbol	Description
7	-	-	**Reserved**
6	R/W	BWF	**Broadcast Wakeup Frame:** 1: Enable Broadcast Wakeup Frame with mask bytes of only DID field = FF FF FF FF FF FF. 0: Default value. Disable Broadcast Wakeup Frame with mask bytes of only DID field = FF FF FF FF FF FF. The power-on default value of this bit is 0.
5	R/W	MWF	**Multicast Wakeup Frame:** 1: Enable Multicast Wakeup Frame with mask bytes of only DID field, which is a multicast address. 0: Default value. Disable Multicast Wakeup Frame with mask bytes of only DID field, which is a multicast address. The power-on default value of this bit is 0.
4	R/W	UWF	**Unicast Wakeup Frame:** 1: Enable Unicast Wakeup Frame with mask bytes of only DID field, which is its own physical address. 0: Default value. Disable Unicast Wakeup Frame with mask bytes of only DID field, which is its own physical address. The power-on default value of this bit is 0.
3:2	-	-	**Reserved**
1	R/W	LANWake	**LANWake Signal Enable/Disable:** 1: Enable LANWake signal. 0: Disable LANWake signal.
0	R/W	PME_STS	**PME_Status bit:** Always sticky/can be reset by PCI RST# and software. 1: The PME_Status bit can be reset by PCI reset or by software. 0: The PME_Status bit can only be reset by software.

- Bit1 and bit0 are auto-loaded from the EEPROM Config5 byte to the RTL8169 Config5 register.

6.17 Multiple Interrupt Select (Offset 005Ch-005Dh, R/W)

Bit	R/W	Symbol	Description
15:12	-	-	**Reserved**
11:0	R/W	MISR11-0	**Multiple Interrupt Select:** Indicates that the RTL8169 will make a receive interrupt after the RTL8169 has transferred the data bytes specified in this register into the system memory. If the value of this register is zero, there will be no early receive interrupts before the whole received packet is transferred to system memory. Bit1, 0 must be zero.

- When MulERINT=1, any received packet invokes an early interrupt according to the MISR[11:0] setting in early mode.

6.18 PHYAR: PHY Access (Offset 0060h-0063h, R/W)

PHY address is fixed at 00001.

Bit	R/W	Symbol	Description
31	R/W	Flag	**Flag bit, used as PCI VPD access method:** 1: Write data to MII register, and turn to 0 automatically whenever the RTL8169 has completed writing to the specified MII register. 0: Read data from MII register, and turn to 1 automatically whenever the RTL8169 has completed retrieving data from the specified MII register.
30:21	-	-	**Reserved**
20:16	R/W	RegAddr4-0	**5-bit GMII/MII register address.**
15:0	R/W	Data15-0	**16-bit GMII/MII register data.**

6.19 TBICSR: Ten Bit Interface Control and Status (Offset 0064h-0067h, R/W)

Bit	R/W	Symbol	Description
31	R/W	ResetTBI	**Reset TBI:** This bit, when set, indicates to the TBI to reset the interfacing PHY device. This bit is cleared when the reset process is completed.
30	R/W	TBILoopBack	**TBI Loopback Enable:** This bit, when set, indicates to the TBI that the interfacing PHY device is in loopback mode.
29	R/W	TBINWEn	**TBI Auto-negotiation Enable:** This bit, when set, enables the auto-negotiation function for the TBI interface.
28	R/W	TBIReNW	**TBI Restart Auto-negotiation:** This bit, when set, restarts the auto-negotiation. This bit is cleared when the auto-negotiation completes.
27:26	-	-	**Reserved**
25	R	TBILinkOk	**TBI Link Ok:** This bit, when set, indicates that the channel connecting to the link partner is established.
24	R	TBINWComplete	**TBI Nway Complete:** This bit, when set, indicates that the auto-negotiation process has completed in TBI mode.
23:20		TXOSETST3-0	**Reserved:** For Realtek internal testing.
19	-	-	**Reserved**
18:16		ANST2-0	**Reserved:** For Realtek internal testing.
15:13	-	-	**Reserved**
12:8		RXST4-0	**Reserved:** For Realtek internal testing.
7:4		SYNCST3-0	**Reserved:** For Realtek internal testing.
3:0		TXCGST3-0	**Reserved:** For Realtek internal testing.

6.20 TBI_ANAR: TBI Auto-Negotiation Advertisement (Offset 0068h-0069h, R/W)

<table>
<tr><th>Bit</th><th>R/W</th><th>Symbol</th><th>Description</th></tr>
<tr><td>15:14</td><td>-</td><td>-</td><td>Reserved. Always 0.</td></tr>
<tr><td>13:12</td><td>R/W</td><td>RF2, RF1</td><td>Remote Fault Bits: These 2 bits indicate that a fault or error condition has occurred. The default value is 00.
<table>
<tr><th>RF1</th><th>RF2</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>No error, link Ok (default)</td></tr>
<tr><td>0</td><td>1</td><td>Offline</td></tr>
<tr><td>1</td><td>0</td><td>Link_Failure</td></tr>
<tr><td>1</td><td>1</td><td>Auto-Negotiation Error</td></tr>
</table></td></tr>
<tr><td>11:9</td><td>-</td><td>-</td><td>Reserved. Always 0.</td></tr>
<tr><td>8:7</td><td>R/W</td><td>PS2(ASM_DIR), PS1(PAUSE)</td><td>Asymmetric Pause: When this bit is set, the value of bit7 (Pause) indicates the direction PAUSE frames are supported.
<table>
<tr><th>PS1</th><th>PS2</th><th>Capability</th></tr>
<tr><td>0</td><td>0</td><td>No Pause.</td></tr>
<tr><td>0</td><td>1</td><td>Asymmetric PAUSE toward link partner.</td></tr>
<tr><td>1</td><td>0</td><td>Symmetric PAUSE.</td></tr>
<tr><td>1</td><td>1</td><td>Both symmetric PAUSE and asymmetric PAUSE toward local device.</td></tr>
</table></td></tr>
<tr><td>6</td><td>-</td><td>-</td><td>Reserved.</td></tr>
<tr><td>5</td><td>R</td><td>FullDup</td><td>Full Duplex: This bit is always set. Full duplex capability is advertised toward the link partner in NWay mode.</td></tr>
<tr><td>4:0</td><td>-</td><td>-</td><td>Reserved</td></tr>
</table>

6.21 TBI_LPAR: TBI Auto-Negotiation Link Partner Ability (Offset 006Ah-006Bh, R)

<table>
<tr><th>Bit</th><th>R/W</th><th>Symbol</th><th>Description</th></tr>
<tr><td>15</td><td>R</td><td>NextPage</td><td>Next Page Exchange Required: When set, this bit indicates that the link partner has a next page to transmit.</td></tr>
<tr><td>14</td><td>R</td><td>Ack</td><td>Acknowledge: When set, this bit indicates that the link partner has successfully received at least 3 consecutive and matching pages (ignoring the Ack bit in the received pages).</td></tr>
<tr><td>13:12</td><td>R</td><td>RF2, RF1</td><td>Remote Fault bits: These 2 bits indicate that a fault or error condition has occurred. The default value is 00.
<table>
<tr><th>RF1</th><th>RF2</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>No error, link Ok (default)</td></tr>
<tr><td>0</td><td>1</td><td>Offline</td></tr>
<tr><td>1</td><td>0</td><td>Link_Failure</td></tr>
<tr><td>1</td><td>1</td><td>Auto-Negotiation Error</td></tr>
</table></td></tr>
<tr><td>11:9</td><td>-</td><td>-</td><td>Reserved</td></tr>
</table>

cont...

8:7	R	PS2(ASM_DIR), PS1(PAUSE)	**Asymmetric Pause:** When this bit is set, the value of bit7 (Pause) indicates the direction that PAUSE frames are supported by the link partner. **PS1** / **PS2** / **Capability** 0 / 0 / No Pause. 0 / 1 / Asymmetric PAUSE toward link partner. 1 / 0 / Symmetric PAUSE. 1 / 1 / Both symmetric PAUSE and asymmetric PAUSE toward local device.
6	R	HalfDup	**Half Duplex:** When set, the link partner supports half duplex.
5	R	FullDup	**Full Duplex:** When set, the link partner supports full duplex.
4:0	-	-	**Reserved**

6.22 PHYStatus: PHY(GMII or TBI) Status (Offset 006Ch, R)

Bit	R/W	Symbol	Description
7	R	EnTBI	**TBI Enable:** This bit is autoloaded from the EEPROM. 1: TBI mode, 0: GMII(MII) mode.
6	R	TxFlow	**Transmit Flow Control:** 1: Enabled, 0: Disabled.
5	R	RxFlow	**Receive Flow Control:** 1: Enabled, 0: Disabled.
4	R	1000MF	Link speed is 1000Mbps and in full-duplex. (GMII mode only)
3	R	100M	Link speed is 100Mbps. (GMII or MII mode only)
2	R	10M	Link speed is 10Mbps. (GMII or MII mode only)
1	R	LinkSts	Link Status. 1: Link Ok, 0: No Link.
0	R	FullDup	**Full-Duplex Status:** 1: Full-duplex mode, 0: Half-duplex mode.

- MII registers polling cycle: 320ns * (32 MDC clock + 32 MDC clock) * 6 registers

6.23 RMS: Receive (Rx) Packet Maximum Size (Offset 00DAh-00DBh, R)

Bit	R/W	Symbol	Description
15:14	-	-	**Reserved**
13:0	R/W	RMS	**Rx packet Maximum Size:** i. This register should be always set to a value other than 0, in order to receive packets. ii. The maximum size supported is 2^{14}-1, i.e., 16K-1 bytes.

6.24 C+CR: C+ Command (Offset 00E0h-00E1h, R/W)

Bit	R/W	Symbol	Description
15:10	-	-	**Reserved**
9	R/W	ENDIAN	**Endian Mode:** 1: Big-endian mode. 0: Little-endian mode.
8	-	-	**Reserved** (Home LAN Enable, always 0)
7	-	-	**Reserved**
6	R/W	RxVLAN	**Receive VLAN De-tagging Enable:** 1: Enable; 0: Disable.
5	R/W	RxChkSum	**Receive Checksum Offload Enable:** 1: Enable; 0: Disable.
4	R/W	DAC	**PCI Dual Address Cycle Enable:** When set, the RTL8169 will perform Tx/Rx DMA using PCI Dual Address Cycle only when the High 32-bit buffer address is not equal to 0. 1: Enable; 0: Disable (initial value at power-up).
3	R/W	MulRW	**PCI Multiple Read/Write Enable:** If this bit is enabled, the setting of Max Tx/Rx DMA burst size is no longer valid. 1: Enable; 0: Disable.
2:0	-	-	**Reserved**

- **This register is the key before configuring other registers and descriptors.**
- **This register is word access only, byte access to this register has no effect.**

6.25 RDSAR: Receive Descriptor Start Address (Offset 00E4h-00EBh, R/W)

Bit	R/W	Symbol	Description
63:0	R/W	RDSA	**Receive Descriptor Start Address**: 64-bit address, 256-byte alignment address. Bit[31:0]: Offset E7h-E4h, low 32-bit address. Bit[63:32]: Offset EBh-E8h, high 32-bit address.

6.26 ETThR: Early Transmit Threshold (Offset 00ECh, R/W)

Bit	R/W	Symbol	Description
7:6	-	-	**Reserved**
5:0	R/W	ETTh	**Early Tx Threshold:** Specifies the threshold level in the Tx FIFO to begin the transmission. When the byte count of the data in the Tx FIFO reaches this level, (or the FIFO contains at least one complete packet) the RTL8169 will transmit the packet. - These fields count from 000001 to 111111 in units of 32 bytes. - This threshold must be avoided from exceeding 2K bytes. - 000000 is reserved. Do not set to this value.

6.27 Function Event (Offset 00F0h-00F3h, R/W)

Bit	R/W	Symbol	Description
31:16	-	-	**Reserved**
15	R/W	INTR	**Interrupt:** This bit is set to 1 when the INTR field in the Function Force Event Register is set. Writing a 1 may clear this bit. Writing a 0 has no effect. This bit is not affected by the RST# pin and software reset.
14:5	-	-	**Reserved**
4	R/W	GWAKE	**General Wakeup:** This bit is set to 1 when the GWAKE field in the Function Present State Register changes its state from 0 to 1. This bit can also be set when the GWAKE bit of the Function Force Register is set. Writing a 1 may clear this bit. Writing a 0 has no effect. This bit is not affected by the RST# pin.
3:0	-	-	**Reserved**

- This register is valid only when Card_En=1 (bit3, Config3) and FuncRegEn=1 (bit1, Config3).
- The Function Event (Offset F0h), Function Event Mask (Offset F4h), Function Present State (Offset F8h), and Function Force Event (Offset FCh) registers have some corresponding fields with the same names. The GWAKE and INTR bits of these registers reflect the wake-up event signaled on the SCTCSCHG pin. The operation of CSTCSCHG pin is similar to PME# pin except that the CSTCSCHG pin is asserted high.

6.28 Function Event Mask (Offset 00F4h-00F7h, R/W)

Bit	R/W	Symbol	Description
31:16	-	-	**Reserved**
15	R/W	INTR	**Interrupt mask:** When cleared (0), setting of the INTR bit in either the Function Present State Register or the Function Event Register will neither cause assertion of the INT# signal while the CardBus PC Card interface is powered up, nor the system Wakeup (CSTSCHG) while the interface is powered off. Setting this bit to 1, enables the INTR bit in both the Function Present State Register and the Function Event Register to generate the INT# signal (and the system Wakeup if the corresponding WKUP field in this Function Event Mask Register is also set). This bit is not affected by RST#.
14	R/W	WKUP	**Wakeup mask:** When cleared (0), the Wakeup function is disabled, i.e., the setting of this bit in the Function Event Register will not assert the CSTSCHG signal. Setting this bit to 1, enables the fields in the Function Event Register to assert the CSTSCHG signal. This bit is not affected by RST#.
13:5	-	-	**Reserved**
4	R/W	GWAKE	**General Wakeup mask:** When cleared (0), setting this bit in the Function Event Register will not cause CSTSCHG pin asserted. Setting this bit to 1, enables the GWAKE field in the Function Event Register to assert CSTSCHG pin if bit14 of this register is also set. This bit is not affected by the RST# pin.
3:0	-	-	**Reserved**

- This register is valid only when Card_En=1 (bit3, Config3) and FuncRegEn=1 (bit1, Config3).

6.29 Function Preset State (Offset 00F8h-00FBh, R)

Bit	R/W	Symbol	Description
31:16	-	-	**Reserved**
15	R	INTR	**Interrupt:** This bit is set when one of the ISR register bits has been set to 1. This bit remains set (1), until all of the ISR register bits have been cleared. This bit is not affected by the RST# pin.
14:5	-	-	**Reserved**
4	R	GWAKE	**General Wakeup:** This bit reflects the current state of the Wakeup event(s), and is just like the PME_Status bit of the PMCSR register. This bit remains set (1), until the PME_Status bit of the PMCSR register is cleared. It is not affected by the RST# pin.
3:0	-	-	**Reserved**

- This register is valid only when Card_En=1 (bit3, Config3) and FuncRegEn=1 (bit1, Config3).
- This read-only register reflects the current state of the function.

6.30 Function Force Event (Offset 00FCh-00FFh, W)

Bit	R/W	Symbol	Description
31:16	-	-	**Reserved**
15	W	INTR	**Interrupt:** Writing a 1 sets the INTR bit in the Function Event Register. However, the INTR bit in the Function Present State Register is not affected and continues to reflect the current state of the ISR register. Writing a 0 to this bit has no effect.
14:5	-	-	**Reserved**
4	W	GWAKE	**General Wakeup:** Setting this bit to 1, sets the GWAKE bit in the Function Event Register. However, the GWAKE bit in the Function Present State Register is not affected and continues to reflect the current state of the Wakeup request. Writing a 0 to this bit has no effect.
3:0	-	-	**Reserved**

- This register is valid only when Card_En=1 (bit3, Config3) and FuncRegEn=1 (bit1, Config3).

7. EEPROM (93C46 or 93C56) Contents

The RTL8169 supports the attachment of an external EEPROM. The 93C46 is a 1K-bit EEPROM, and the 93C56 is a 2K-bit EEPROM. The EEPROM interface provides the ability for the RTL8169 to read from and write data to an external serial EEPROM device. Values in the external EEPROM allow default fields in PCI configuration space and I/O space to be overridden following internal power on reset or software EEPROM autoload command. The RTL8169 will autoload values from the EEPROM to these fields in configuration space and I/O space. If the EEPROM is not present, the RTL8169 initialization uses default values for the appropriate Configuration and Operational Registers. Software can read and write to the EEPROM using "bit-bang" accesses via the 9346CR Register.

Although it is actually addressed by words, its contents are listed below by bytes for convenience. After the initial power on or autoload command in 9346CR, the RTL8169 performs a series of EEPROM read operations from the 93C46 (93C56) address 00h to 31h.

- It is suggested to obtain Realtek approval before changing the default settings of the EEPROM.

<table>
<tr><th>Bytes</th><th>Contents</th><th>Description</th></tr>
<tr><td>00h
01h</td><td>29h
81h</td><td>These 2 bytes contain ID code words for the RTL8169. The RTL8169 will load the contents of the EEPROM into the corresponding location if the ID word (8129h) is correct. Otherwise, the Vendor ID and Device ID of the PCI configuration space are "10ECh" and "8169h".</td></tr>
<tr><td>02h-03h</td><td>VID</td><td>PCI Vendor ID: PCI configuration space offset 00h-01h.</td></tr>
<tr><td>04h-05h</td><td>DID</td><td>PCI Device ID: PCI configuration space offset 02h-03h.</td></tr>
<tr><td>06h-07h</td><td>SVID</td><td>PCI Subsystem Vendor ID: PCI configuration space offset 2Ch-2Dh.</td></tr>
<tr><td>08h-09h</td><td>SMID</td><td>PCI Subsystem ID: PCI configuration space offset 2Eh-2Fh.</td></tr>
<tr><td>0Ah</td><td>MNGNT</td><td>PCI Minimum Grant Timer: PCI configuration space offset 3Eh.</td></tr>
<tr><td>0Bh</td><td>MXLAT</td><td>PCI Maximum Latency Timer: PCI configuration space offset 3Fh. Set by software to the number of PCI clocks that the RTL8169 may hold the PCI bus.</td></tr>
<tr><td>0Ch</td><td>CONFIGx</td><td>Bit3: EnTBI. When set, TBI mode is enabled. Otherwise, the RTL8169 operates in GMII/MII mode.
<table>
<tr><td>Bit</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td></td><td>-</td><td>-</td><td>-</td><td>-</td><td>EnTBI (bit7, PHYStatus)</td><td>-</td><td>-</td><td>-</td></tr>
</table></td></tr>
<tr><td>0Dh</td><td>CONFIG3</td><td>RTL8169 Configuration register 3: Operational register offset 59h.</td></tr>
<tr><td>0Eh-13h</td><td>Ethernet ID</td><td>Ethernet ID: After auto-load command or hardware reset, the RTL8169 loads Ethernet ID to IDR0-IDR5 of the RTL8169's I/O registers.</td></tr>
<tr><td>14h</td><td>CONFIG0</td><td>RTL8169 Configuration register 0: Operational registers offset 51h.</td></tr>
<tr><td>15h</td><td>CONFIG1</td><td>RTL8169 Configuration register 1: Operational registers offset 52h.</td></tr>
<tr><td>16h-17h</td><td>PMC</td><td>Reserved: Do not change this field without Realtek approval.
Power Management Capabilities. PCI configuration space address 52h and 53h.</td></tr>
<tr><td>18h</td><td>-</td><td>Reserved</td></tr>
<tr><td>19h</td><td>CONFIG4</td><td>Reserved: Do not change this field without Realtek approval.
RTL8169 Configuration register 4, operational registers offset 5Ah.</td></tr>
<tr><td>1Ah-1Eh</td><td>-</td><td>Reserved</td></tr>
<tr><td>1Fh</td><td>CONFIG_5</td><td>Do not change this field without Realtek approval.
Bit7-2: Reserved.
Bit1: LANWake signal Enable/Disable
Set to 1: Enable LANWake signal.
Set to 0: Disable LANWake signal.
Bit0: PME_Status bit property
Set to 1: The PME_Status bit can be reset by PCI reset or by software if D3cold_support_PME is 0. If D3cold_support_PME=1, the PME_Status bit is a sticky bit.
Set to 0: The PME_Status bit is always a sticky bit and can only be reset by software.</td></tr>
</table>

cont...

20h-2Fh	-	**Reserved**
30h-31h	CISPointer	**Reserved:** Do not change this field without Realtek approval. CIS Pointer.
32h-33h	CheckSum	**Reserved:** Do not change this field without Realtek approval. Checksum of the EEPROM content.
34h-3Eh	-	**Reserved:** Do not change this field without Realtek approval.
3Fh	PXE_Para	**Reserved:** Do not change this field without Realtek approval. PXE ROM code parameter.
40h-7Fh	VPD_Data	**VPD data field:** Offset 40h is the start address of the VPD data.
80h-FFh	CIS_Data	**CIS data field:** Offset 80h is the start address of the CIS data. (93C56 only).

7.1 EEPROM Registers

Offset	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h-05h	IDR0 – IDR5	R/W*								
51h	CONFIG0	R		-	-	-	-	BS2	BS1	BS0
		W*	-	-	-	-	-	-	-	-
52h	CONFIG1	R	LEDS1	LEDS0	DVRLOAD	LWACT	MEMMAP	IOMAP	VPD	PMEN
		W*	LEDS1	LEDS0	DVRLOAD	LWACT	-	-	VPD	PMEN
54h	CONFIG3	R	GNTDel	-	Magic	LinkUp	CardB_En	CLKRUN_En	FuncRegEn	FBtBEn
		W*	-	-	Magic	LinkUp	-	-	-	-
55h	CONFIG4	R/W*	RxFIFOAutoClr	-	-	LWPME	-	LWPTN	-	-
56h	CONFIG5	R/W*	-	-	-	-	-	-	LANWake	PME_STS
6Ch	PHYStatus	R	EnTBI	-	-	-	-	-	-	-
E1h	C+CR	R/W	-	-	-	-	-	-	Endian	-

* The registers marked with type = 'W*' can be written only if bits EEM1=EEM0=1.

7.2 EEPROM Power Management Registers

Configuration Space offset	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DEh	PMC	R	Aux_I_b1	Aux_I_b0	DSI	Reserved	PMECLK	Version		
DFh		R	PME_D3$_{cold}$	PME_D3$_{hot}$	PME_D2	PME_D1	PME_D0	D2	D1	Aux_I_b2

8. PCI Configuration Space Registers

8.1 PCI Bus Interface

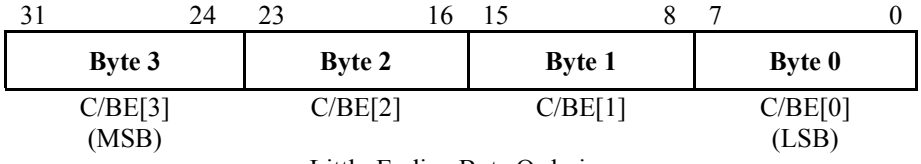
The RTL8169 implements the PCI bus interface as defined in the PCI Local Bus Specifications Rev. 2.2. When internal registers are being accessed, the RTL8169 acts as a PCI target (slave mode). When accessing host memory for descriptor or packet data transfer, the RTL8169 acts as a PCI bus master.

All of the required pins and functions are implemented in the RTL8169 as well as the optional pin, INTAB for support of interrupt requests is implemented as well. The bus interface also supports 64-bit and 66Mhz operation in addition to the more common 32-bit and 33-Mhz capabilities. For more information, refer to the PCI Local Bus Specifications Rev. 2.2, December 18, 1998.

8.1.1 Byte Ordering

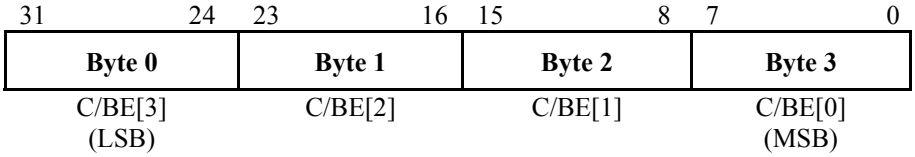
The RTL8169 can be configured to order the bytes of data on the PCI AD bus to conform to little-endian or big-endian ordering through the use of the ENDIAN bit of the C+ Command Register. When the RTL8169 is configured in big-endian mode, all the data in the data phase of either memory or I/O transaction to or from RTL8169 is in big-endian mode. All data in the data phase of any PCI configuration transaction to the RTL8169 should be in little-endian mode, regardless if the RTL8169 is set to big-endian or little-endian mode.

When configured for little-endian mode (ENDIAN bit=0), the byte orientation for receive and transmit data and descriptors in system memory is as follows:



Little-Endian Byte Ordering

When configured for big-endian mode (ENDIAN bit=1), the byte orientation for receive and transmit data and descriptors in system memory is as follows:



Big-Endian Byte Ordering

8.1.2 Interrupt Control

Interrupts are performed by asynchronously asserting the INTAB pin. This pin is an open drain output. The source of the interrupt can be determined by reading the Interrupt Status Register (ISR). One or more bits in the ISR will be set, denoting all currently pending interrupts. Writing 1 to any bit in the ISR register clears that bit. Masking of specific interrupts can be accomplished by using the Interrupt Mask Register (IMR). Assertion of INTAB can be prevented by clearing the Interrupt Enable bit in the Interrupt Mask Register. This allows the system to defer interrupt processing as needed.

8.1.3 Latency Timer

The PCI Latency Timer described in LTR defines the maximum number of bus clocks that the device will hold the bus. Once the device gains control of the bus and issues FRAMEB, the Latency Timer will begin counting down. The LTR register specifies, in units of PCI bus clocks, the value of the latency timer of the RTL8169. When the RTL8169 asserts FRAMEB, it enables its latency timer to count. If the RTL8169 deasserts FRAMEB prior to count expiration, the content of the latency timer is ignored. Otherwise, after the count expires, the RTL8169 initiates transaction termination as soon as its GNTB is deasserted. Software is able to read or write to LTR, and the default value is 00H.

8.1.4 64-Bit Data Operation

The RTL8169 samples the REQ64B pin at PCI RSTB deasserted to determine if the bus is 64-bit capable.

8.1.5 64-Bit Addressing

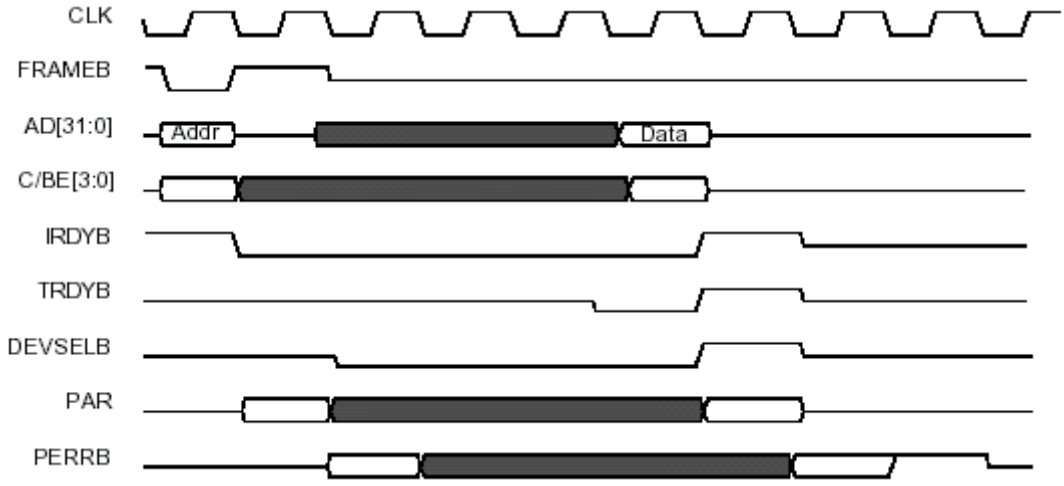
The RTL8169 supports 64-bit addressing (Dual Address Cycle, DAC) as a bus master for transferring descriptor and packet data information. The DAC mode can be enabled or disabled through software. The RTL8169 only supports 32-bit addressing as a target.

8.2 Bus Operation

8.2.1 Target Read

A Target Read operation starts with the system generating FRAMEB, Address, and either an IO read (0010b) or Memory Read (0110b) command. If the 32-bit address on the address bus matches the IO address range specified in IOAR (for I/O reads) or the memory address range specified in MEM (for memory reads), the RTL8169 will generate DEVSELB 2 clock cycles later (medium speed). The system must tri-state the Address bus, and convert the C/BE bus to byte enables, after the address cycle. On the 2nd cycle after the assertion of DEVSELB, all 32-bits of data and TRDYB will become valid. If IRDYB is asserted at that time, TRDYB will be forced HIGH on the next clock for 1 cycle, and then tri-stated.

If FRAMEB is asserted beyond the assertion of IRDYB, the RTL8169 will still make data available as described above, but will also issue a Disconnect. That is, it will assert the STOPB signal with TRDYB. STOPB will remain asserted until FRAMEB is detected as deasserted.

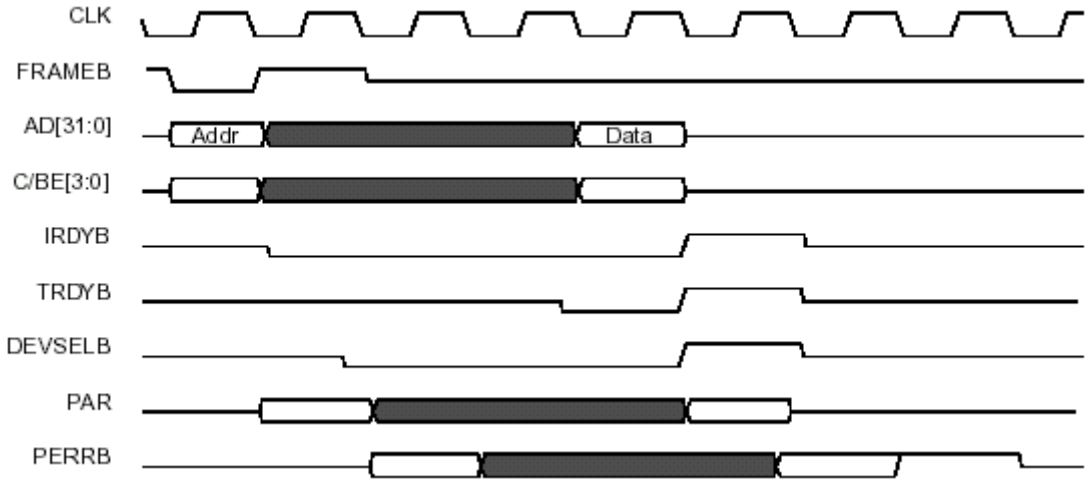


Target Read Operation

8.2.2 Target Write

A Target Write operation starts with the system generating FRAMEN, Address, and Command (0011b or 0111b). If the upper 24 bits on the address bus match IOAR (for I/O reads) or MEM (for memory reads), the RTL8169 will generate DEVSELB 2 clock cycles later. On the 2nd cycle after the assertion of DEVSELB, the device will monitor the IRDYB signal. If IRDYB is asserted at that time, the RTL8169 will assert TRDYB. On the next clock the 32-bit double word will be latched in, and TRDYB will be forced HIGH for 1 cycle and then tri-stated. Target write operations must be 32-bits wide.

If FRAMEB is asserted beyond the assertion of IRDYB, the RTL8169 will still latch the first double word as described above, but will also issue a Disconnect. That is, it will assert the STOPB signal with TRDYB. STOPB will remain asserted until FRAMEB is detected as deasserted.



Target Write Operation

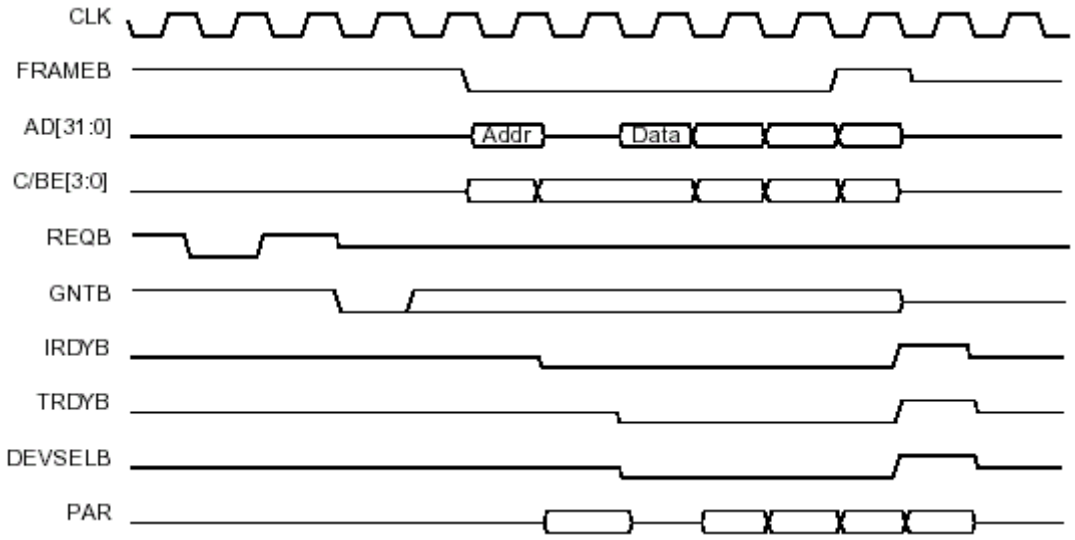
8.2.3 Master Read

A Master Read operation starts with the RTL8169 asserting REQB. If GNTB is asserted within 2 clock cycles, FRAMEB, Address, and Command will be generated 2 clocks after REQB (Address and FRAMEB for 1 cycle only). If GNTB is asserted 3 cycles or later, FRAMEB, Address, and Command will be generated on the clock following GNTB.

The device will wait for 8 cycles for the assertion of DEVSELB. If DEVSELB is not asserted within 8 clocks, the device will issue a master abort by asserting FRAMEB HIGH for 1 cycle, and IRDYB will be forced HIGH on the following cycle. Both signals will become tri-state on the cycle following their deassertion.

On the clock edge after the generation of Address and Command, the address bus will become tri-state, and the C/BE bus will contain valid byte enables. On the clock edge after FRAMEB was asserted, IRDYB will be asserted (and FRAMEB will be deasserted if this is to be a single read operation). On the clock where both TRDYB and DEVSELB are detected as asserted, data will be latched in (and the byte enables will change if necessary). This will continue until the cycle following the deassertion of FRAMEB.

On the clock where the second to last read cycle occurs, FRAMEB will be forced HIGH (it will be tri-stated 1 cycle later). On the next clock edge that the device detects TRDYB asserted, it will force IRDYB HIGH. It, too, will be tri-stated 1 cycle later. This will conclude the read operation. The RTL8169 will never force a wait state during a read operation.



Master Read Operation

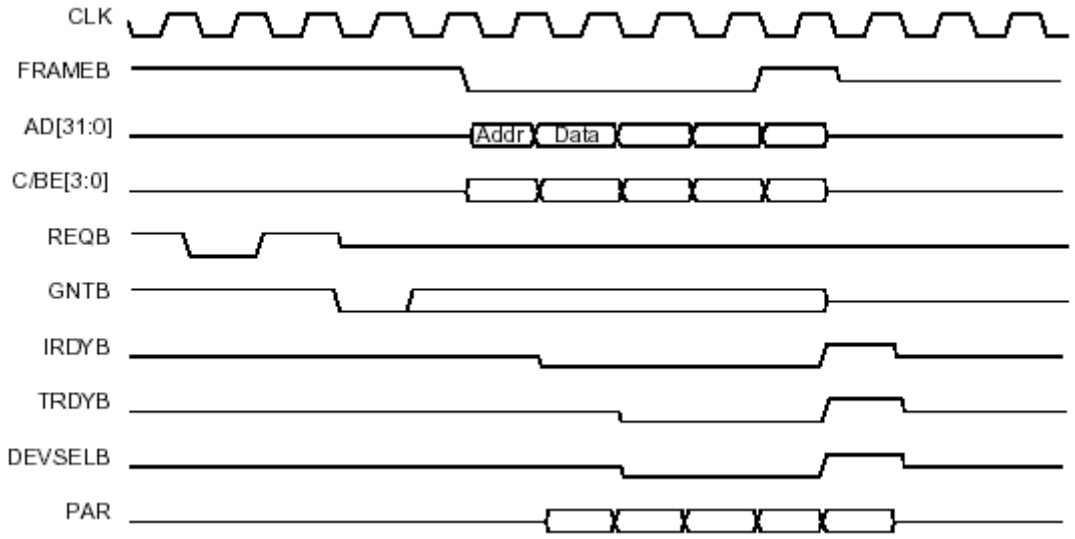
8.2.4 Master Write

A Master Write operation starts with the RTL8169 asserting REQB. If GNTB is asserted within 2 clock cycles, FRAMEB, Address, and Command will be generated 2 clocks after REQB (Address and FRAMEB for 1 cycle only). If GNTB is asserted 3 cycles or later, FRAMEB, Address, and Command will be generated on the clock following GNTB.

The device will wait for 8 cycles for the assertion of DEVSELB. If DEVSELB is not asserted within 8 clocks, the device will issue a Master Abort by asserting FRAMEB HIGH for 1 cycle. IRDYB will be forced HIGH on the following cycle. Both signals will become tri-state on the cycle following their deassertion.

On the clock edge after the generation of Address and Command, the data bus will become valid, and the C/BE bus will contain valid byte enables. On the clock edge after FRAMEB was asserted, IRDYB will be asserted (and FRAMEB will be deasserted if this is to be a single read operation). On the clock where both TRDYB and DEVSELB are detected as asserted, valid data for the next cycle will become available (and the byte enables will change if necessary). This will continue until the cycle following the deassertion of FRAMEB.

On the clock where the second to last write cycle occurs, FRAMEB will be forced HIGH (it will be tri-stated 1 cycle later). On the next clock edge that the device detects TRDYB asserted, it will force IRDYB HIGH. It, too, will be tri-stated 1 cycle later. This will conclude the write operation. The RTL8169 will never force a wait state during a write operation.



Master Write Operation

8.2.5 Configuration Access

Configuration register accesses are similar to target reads and writes in that they are single data word transfers and are initiated by the system. For the system to initiate a Configuration access, it must also generate IDSEL as well as the correct Command (1010b or 1011b) during the Address phase. The RTL8169 will respond as it does during Target operations. Configuration reads must be 32-bits wide, but writes may access individual bytes.

8.3 Packet Buffering

The RTL8169 incorporates two independent FIFOs for transferring data to/from the system interface and from/to the network. The FIFOs, providing temporary storage of data freeing the host system from the real-time demands of the network.

The way in which the FIFOs are emptied and filled is controlled by the FIFO threshold values in the Transmit Configuration and Receive Configuration registers. These values determine how full or empty the FIFOs must be before the device requests the bus. Additionally, there is a threshold value that determines how full the transmit FIFO must be before beginning transmission. Once the RTL8169 requests the bus, it will attempt to empty or fill the FIFOs as allowed by the respective MXDMA settings in the Transmit Configuration and Receive Configuration registers.

8.3.1 Transmit Buffer Manager

The buffer management scheme used on the RTL8169 allows quick, simple and efficient use of the frame buffer memory. The buffer management scheme uses separate buffers and descriptors for packet information. This allows effective transfers of data to the transmit buffer manager by simply transferring the descriptor information to the transmit queue.

The Tx Buffer Manager DMAs packet data from system memory and places it in the 8KB transmit FIFO, and pulls data from the FIFO to send to the Tx MAC. Multiple packets may be present in the FIFO, allowing packets to be transmitted with minimum interframe gap. The way in which the FIFO is emptied and filled is controlled by the ETTH (Early Transmit Threshold) and RXFTH (Rx FIFO Threshold) values. Additionally, once the RTL8169 requests the bus, it will attempt to fill the FIFO as allowed by the MXDMA setting.

The Tx Buffer Manager process also supports priority queuing of transmit packets. It handles this by drawing from two separate descriptor lists to fill the internal FIFO. If packets are available in the high priority queues, they will be loaded into the FIFO before those of low priority.

8.3.2 Receive Buffer Manager

The Rx Buffer Manager uses the same buffer management scheme as used for transmits. The Rx Buffer Manager retrieves packet data from the Rx MAC and places it in the 32KB receive data FIFO, and pulls data from the FIFO for DMA to system memory. Similar to the transmit FIFO, the receive FIFO is controlled by the FIFO threshold value in RXFTH. This value determines the number of long words written into the FIFO from the MAC unit before a DMA request for system memory occurs. Once the RTL8169 gets the bus, it will continue to transfer the long words from the FIFO until the data in the FIFO is less than one long word, or has reached the end of the packet, or the max DMA burst size is reached , as set in MXDMA.

8.3.3 Packet Recognition

The Rx packet filter and recognition logic allows software to control which packets are accepted, based on destination address and packet type. Address recognition logic includes support for broadcast, multicast hash, and unicast addresses. The packet recognition logic includes support for WOL, Pause, and programmable pattern recognition.

8.4 PCI Configuration Space Table

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	VID	R	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
01h		R	VID15	VID14	VID13	VID12	VID11	VID10	VID9	VID8
02h	DID	R	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
03h		R	DID15	DID14	DID13	DID12	DID11	DID10	DID9	DID8
04h	Command	R	0	PERRSP	0	MWIEN	0	BMEN	MEMEN	IOEN
		W	-	PERRSP	-	MWIEN	-	BMEN	MEMEN	IOEN
05h		R	0	0	0	0	0	0	FBTBEN	SERREN
		W	-	-	-	-	-	-	-	SERREN
06h	Status	R	FBBC	0	0	NewCap	0	0	0	0
07h		R	DPERR	SSERR	RMABT	RTABT	STABT	DST1	DST0	DPD
		W	DPERR	SSERR	RMABT	RTABT	STABT	-	-	DPD
08h	Revision ID	R	0	0	0	0	0	0	0	0
09h	PIFR	R	0	0	0	0	0	0	0	0
0Ah	SCR	R	0	0	0	0	0	0	0	0
0Bh	BCR	R	0	0	0	0	0	0	1	0
0Ch	CLS	R/W	0	0	0	0	0	0	0	0
0Dh	LTR	R	LTR7	LTR6	LTR5	LTR4	LTR3	LTP2	LTR1	LTR0
		W	LTR7	LTR6	LTR5	LTR4	LTR3	LTP2	LTR1	LTR0
0Eh	HTR	R	0	0	0	0	0	0	0	0
0Fh	BIST	R	0	0	0	0	0	0	0	0
10h	IOAR	R	0	0	0	0	0	0	0	IOIN
		W	-	-	-	-	-	-	-	-
11h		R/W	IOAR15	IOAR14	IOAR13	IOAR12	IOAR11	IOAR10	IOAR9	IOAR8
12h		R/W	IOAR23	IOAR22	IOAR21	IOAR20	IOAR19	IOAR18	IOAR17	IOAR16
13h		R/W	IOAR31	IOAR30	IOAR29	IOAR28	IOAR27	IOAR26	IOAR25	IOAR24
14h	MEMAR	R	0	0	0	0	0	0	0	MEMIN
		W	-	-	-	-	-	-	-	-
15h		R/W	MEM15	MEM14	MEM13	MEM12	MEM11	MEM10	MEM9	MEM8
16h		R/W	MEM23	MEM22	MEM21	MEM20	MEM19	MEM18	MEM17	MEM16
17h		R/W	MEM31	MEM30	MEM29	MEM28	MEM27	MEM26	MEM25	MEM24
18h-27h	RESERVED									
28h-2Bh	CISPtr	Cardbus CIS Pointer								
2Ch	SVID	R	SVID7	SVID6	SVID5	SVID4	SVID3	SVID2	SVID1	SVID0
2Dh		R	SVID15	SVID14	SVID13	SVID12	SVID11	SVID10	SVID9	SVID8
2Eh	SMID	R	SMID7	SMID6	SMID5	SMID4	SMID3	SMID2	SMID1	SMID0
2Fh		R	SMID15	SMID14	SMID13	SMID12	SMID11	SMID10	SMID9	SMID8
30h	BMAR	R	0	0	0	0	0	0	0	BROMEN
		W	-	-	-	-	-	-	-	BROMEN
31h		R	BMAR15	BMAR14	BMAR13	BMAR12	BMAR11	0	0	0
		W	BMAR15	BMAR14	BMAR13	BMAR12	BMAR11	-	-	-
32h		R/W	BMAR23	BMAR22	BMAR21	BMAR20	BMAR19	BMAR18	BMAR17	BMAR16
33h		R/W	BMAR31	BMAR30	BMAR29	BMAR28	BMAR27	BMAR26	BMAR25	BMAR24
34h	Cap_Ptr	R	1	1	0	1	1	1	0	0
35h-3Bh	RESERVED									
3Ch	ILR	R/W	IRL7	ILR6	ILR5	ILR4	ILR3	ILR2	ILR1	ILR0
3Dh	IPR	R	0	0	0	0	0	0	0	1

cont...

3Eh	MNGNT	R	0	0	1	0	0	0	0	0
3Fh	MXLAT	R	0	0	1	0	0	0	0	0
40h–5Fh	RESERVED									
60h	VPDID	R	0	0	0	0	0	0	1	1
61h	NextPtr	R	0	0	0	0	0	0	0	0
62h	Flag VPD Address	R/W	VPDADDR7	VPDADDR6	VPDADDR5	VPDADDR4	VPDADDR3	VPDADDR2	VPDADDR1	VPDADDR0
63h		R/W	Flag	VPDADDR14	VPDADDR13	VPDADDR12	VPDADDR11	VPDADDR10	VPDADDR9	VPDADDR8
64h	VPD Data	R/W	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0
65h		R/W	Data15	Data14	Data13	Data12	Data11	Data10	Data9	Data8
66h		R/W	Data23	Data22	Data21	Data20	Data19	Data18	Data17	Data16
67h		R/W	Data31	Data30	Data29	Data28	Data27	Data26	Data25	Data24
68h-DBh	RESERVED									
DCh	PMID	R	0	0	0	0	0	0	0	1
DDh	NextPtr	R	0	1	1	0	0	0	0	0
DEh	PMC	R	Aux_I_b1	Aux_I_b0	DSI	Reserved	PMECLK	Version		
DFh		R	PME_D3_{cold}	PME_D3_{hot}	PME_D2	PME_D1	PME_D0	D2	D1	Aux_I_b2
E0h	PMCSR	R	0	0	0	0	0	0	Power State	
		W	-	-	-	-	-	-	Power State	
E1h		R	PME_Status	-	-	-	-	-	-	PME_En
		W	PME_Status	-	-	-	-	-	-	PME_En
E2h-FFh	RESERVED									

★ The above table is based on both VPD and Power Management are enabled.

8.5 PCI Configuration Space Functions

The PCI configuration space is intended for configuration, initialization, and catastrophic error handling functions. The functions of the RTL8169's configuration space are described below.

VID: Vendor ID. This field will be set to a value corresponding to PCI Vendor ID in the external EEPROM. If there is no EEPROM, this field will default to a value of 10ECh which is Realtek Semiconductor's PCI Vendor ID.

DID: Device ID. This field will be set to a value corresponding to PCI Device ID in the external EEPROM. If there is no EEPROM, this field will default to a value of 8129h.

Command: The command register is a 16-bit register used to provide coarse control over a device's ability to generate and respond to PCI cycles.

Bit	Symbol	Description
15:10	-	**Reserved**
9	FBTBEN	**Fast Back-To-Back Enable:** Config3<FBtBEn>=0:Read as 0. Write operation has no effect. The RTL8169 will not generate Fast Back-to-back cycles. When Config3<FbtBEn>=1, This read/write bit controls whether or not a master can do fast back-to-back transactions to different devices. Initialization software will set the bit if all targets are fast back-to-back capable. A value of 1 means the master is allowed to generate fast back-to-back transaction to different agents. A value of 0 means fast back-to-back transactions are only allowed to the same agent. This bit's state after RST# is 0.
8	SERREN	**System Error Enable:** When set to 1, the RTL8169 asserts the SERRB pin when it detects a parity error on the address phase (AD<31:0> and CBEB<3:0>).
7	ADSTEP	**Address/Data Stepping:** Read as 0, and write operations have no effect. The RTL8169 never performs address/data stepping.

cont...

6	PERRSP	**Parity Error Response:** When set to 1, the RTL8169 will assert the PERRB pin on the detection of a data parity error when acting as the target, and will sample the PERRB pin as the master. When set to 0, any detected parity error is ignored and the RTL8169 continues normal operation. Parity checking is disabled after hardware reset (RSTB).
5	VGASNOOP	**VGA palette SNOOP:** Read as 0, write operations have no effect.
4	MWIEN	**Memory Write and Invalidate cycle Enable:** This is an enable bit for using the Memory Write and Invalidate command. When this bit is 1, the RTL8169 as a master may generate the command. When this bit is 0, the RTL8169 may generate Memory Write command instead. State after PCI RSTB is 0.
3	SCYCEN	**Special Cycle Enable:** Read as 0, write operations have no effect. The RTL8169 ignores all special cycle operations.
2	BMEN	**Bus Master Enable:** When set to 1, the RTL8169 is capable of acting as a PCI bus master. When set to 0, it is prohibited from acting as a bus master. For normal operations, this bit must be set by the system BIOS.
1	MEMEN	**Memory Space Access:** When set to 1, the RTL8169 responds to memory space accesses. When set to 0, the RTL8169 ignores memory space accesses.
0	IOEN	**I/O Space Access:** When set to 1, the RTL8169 responds to IO space accesses. When set to 0, the RTL8169 ignores I/O space accesses.

Status: The status register is a 16-bit register used to record status information for PCI bus related events. Reads to this register behave normally. Writes are slightly different in that bits can be reset, but not set.

Bit	Symbol	Description
15	DPERR	**Detected Parity Error:** This bit, when set, indicates that the RTL8169 has detected a parity error, even if parity error handling is disabled in command register PERRSP bit.
14	SSERR	**Signaled System Error:** This bit, when set, indicates that the RTL8169 has asserted the system error pin, SERRB. Writing a 1 clears this bit to 0.
13	RMABT	**Received Master Abort:** This bit, when set, indicates that the RTL8169 has terminated a master transaction with master abort. Writing a 1 clears this bit to 0.
12	RTABT	**Received Target Abort:** This bit, when set, indicates that an RTL8169 master transaction was terminated due to a target abort. Writing a 1 clears this bit to 0.
11	STABT	**Signaled Target Abort:** This bit is set to 1 whenever the RTL8169 terminates a transaction with a target abort. Writing a 1 clears this bit to 0.
10:9	DST1-0	**Device Select Timing:** These bits encode the timing of DEVSELB. They are set to 01b (medium), indicating the RTL8169 will assert DEVSELB two clocks after FRAMEB is asserted.
8	DPD	**Data Parity error Detected:** This bit is set when the following conditions are met: * The RTL8169 asserts parity error (PERRB pin) or it senses the assertion of PERRB pin by another device. * The RTL8169 operates as a bus master for the operation that caused the error. * The Command register PERRSP bit is set. Writing a 1 clears this bit to 0.
7	FBBC	**Fast Back-To-Back Capable:** Config3<FbtBEn>=0, Read as 0, write operations have no effect. Config3<FbtBEn>=1, Read as 1.
6	UDF	**User Definable Features Supported:** Read as 0, and write operations have no effect. The RTL8169 does not support UDF.
5	66MHz	**66MHz Capable:** Read as 1, and write operations have no effect. The RTL8169 supports 66MHz PCI clock.
4	NewCap	**New Capability:** Config3<PMEn>=0, Read as 0, and write operations have no effect. Config3<PMEn>=1, Read as 1.
0:3	-	**Reserved**

RID: Revision ID Register

The Revision ID register is an 8-bit register that specifies the RTL8169 controller revision number.

PIFR: Programming Interface Register

The programming interface register is an 8-bit register that identifies the programming interface of the RTL8169 controller. The PCI specification reversion 2.1 doesn't define any other specific value for network devices. So PIFR = 00h.

SCR: Sub-Class Register

The Sub-class register is an 8-bit register that identifies the function of the RTL8169. SCR = 00h indicates that the RTL8169 is an Ethernet controller.

BCR: Base-Class Register

The Base-class register is an 8-bit register that broadly classifies the function of the RTL8169. BCR = 02h indicates that the RTL8169 is a network controller.

CLS: Cache Line Size

Specifies, in units of 32-bit words (double-words), the system cache line size. The RTL8169 supports cache line size of 8, and 16 longwords (DWORDs). The RTL8169 uses Cache Line Size for PCI commands that are cache oriented, such as memory-read-line, memory-read-multiple, and memory-write-and-invalidate.

LTR: Latency Timer Register

Specifies, in units of PCI bus clocks, the value of the latency timer of the RTL8169.

When the RTL8169 asserts FRAMEB, it enables its latency timer to count. If the RTL8169 deasserts FRAMEB prior to count expiration, the content of the latency timer is ignored. Otherwise, after the count expires, the RTL8169 initiates transaction termination as soon as its GNTB is deasserted. Software is able to read or write, and the default value is 00h.

HTR: Header Type Register

Reads will return a 0, writes are ignored.

BIST: Built-in Self Test

Reads will return a 0, writes are ignored.

IOAR: This register specifies the BASE IO address which is required to build an address map during configuration. It also specifies the number of bytes required as well as an indication that it can be mapped into IO space. Britain

Bit	Symbol	Description
31:8	IOAR31-8	**BASE IO Address:** This is set by software to the Base IO address for the operational register map.
7:2	IOSIZE	**Size Indication:** Read back as 0. This allows the PCI bridge to determine that the RTL8169 requires 256 bytes of IO space.
1	-	**Reserved**
0	IOIN	**IO Space Indicator:** Read only. Set to 1 by the RTL8169 to indicate that it is capable of being mapped into IO space.

MEMAR: This register specifies the base memory address for memory accesses to the RTL8169 operational registers. This register must be initialized prior to accessing any RTL8169's register with memory access.

Bit	Symbol	Description
31:8	MEM31-8	**Base Memory Address:** This is set by software to the base address for the operational register map.
7:4	MEMSIZE	**Memory Size:** These bits return 0, which indicates that the RTL8169 requires 256 bytes of Memory Space.
3	MEMPF	**Memory Prefetchable:** Read only. Set to 0 by the RTL8169.
2:1	MEMLOC	**Memory Location Select:** Read only. Set to 0 by the RTL8169. This indicates that the base register is 32-bits wide and can be placed anywhere in the 32-bit memory space.
0	MEMIN	**Memory Space Indicator:** Read only. Set to 0 by the RTL8169 to indicate that it is capable of being mapped into memory space.

CISPtr: CardBus CIS Pointer. This field is valid only when CardB_En (bit3, Config3) = 1. The value of this register is auto-loaded from 93C46 or 93C56 (from offset 30h-31h).

- Bit 2-0: Address Space Indicator

Bit2:0	Meaning
7	The CIS begins in the Expansion ROM space.
6:1	The CIS begins in the memory address governed by one of the six Base Address Registers. Ex., if the value is 2, then the CIS begins in the memory address space governed by Base Address Register 2.
0	Not supported. (CIS begins in device-dependent configuration space.)

- Bit27-3: Address Space Offset
- Bit31-28: ROM Image number

Bit2-0	Space Type	Address Space Offset Values
0	Configuration space	Not supported.
X; 1≤X≤6	Memory space	0h≤value≤FFFF FFF8h. This is the offset into the memory address space governed by Base Address Register X. Adding this value to the value in the Base Address Register gives the location of the start of the CIS. For the RTL8169, the value is 100h.
7	Expansion ROM	0≤image number≤Fh, 0h≤value≤0FFF FFF8h. This is the offset into the expansion ROM address space governed by the Expansion ROM Base Register. The image number is in the uppermost nibble of the CISPtr register. The value consists of the remaining bytes. For the RTL8169, the image number is 0h.

This read-only register points to where the CIS begins, in one of the following spaces:

i. Memory Space – The CIS may be in any of the memory spaces from offset 100h and up after being auto-loaded from 93C56. The CIS is stored in 93C56 EEPROM physically from offset 80h-FFh.
ii. Expansion ROM space – The CIS is stored in expansion ROM physically within the 128KB max.

SVID: Subsystem Vendor ID. This field will be set to a value corresponding to PCI Subsystem Vendor ID in the external EEPROM. If there is no EEPROM, this field will default to a value of 10ECh which is Realtek Semiconductor's PCI Subsystem Vendor ID.

SMID: Subsystem ID. This field will be set to value corresponding to PCI Subsystem ID in the external EEPROM. If there is no EEPROM, this field will default to a value of 8129h.

BMAR: This register specifies the base memory address for memory accesses to the RTL8169 operational registers. This register must be initialized prior to accessing any of the RTL8169's register with memory access.

Bit	Symbol	Description
31:18	BMAR31-18	**Boot ROM Base Address**
17:11	ROMSIZE	**Boot ROM Size:** These bits indicate how many Boot ROM spaces to be supported. The Relationship between Config 0 <BS2:0> and BMAR17-11 is as follows: **BS2 BS1 BS0 Description** 0 0 0 No Boot ROM, BROMEN=0 (R) 0 0 1 8K Boot ROM, BROMEN (R/W), BMAR12-11 = 0 (R), BMAR17-13 (R/W) 0 1 0 16K Boot ROM, BROMEN (R/W), BMAR13-11 = 0 (R), BMAR17-14 (R/W) 0 1 1 32K Boot ROM, BROMEN (R/W), BMAR14-11 = 0 (R), BMAR17-15 (R/W) 1 0 0 64K Boot ROM, BROMEN (R/W), BMAR15-11 = 0 (R), BMAR17-16 (R/W) 1 0 1 128K Boot ROM, BROMEN(R/W), BMAR16-11=0 (R), BMAR17 (R/W) 1 1 0 unused 1 1 1 unused
10:1	-	**Reserved** (read back 0)
0	BROMEN	**Boot ROM Enable:** This is used by the PCI BIOS to enable accesses to Boot ROM.

ILR: Interrupt Line Register

The Interrupt Line Register is an 8-bit register used to communicate with the routing of the interrupt. It is written by the POST software to set interrupt line for the RTL8169.

IPR: Interrupt Pin Register

The Interrupt Pin register is an 8-bit register indicating the interrupt pin used by the RTL8169. The RTL8169 uses INTA interrupt pin. Read only. IPR = 01h.

MNGNT: Minimum Grant Timer: Read only

Specifies how long a burst period the RTL8169 needs at 33MHz clock rate in units of 1/4 microsecond. This field will be set to a value from the external EEPROM. If there is no EEPROM, this field will default to a value of 20h.

MXLAT: Maximum Latency Timer: Read only

Specifies how often the RTL8169 needs to gain access to the PCI bus in unit of 1/4 microsecond. This field will be set to a value from the external EEPROM. If there is no EEPROM, this field will default to a value of 20h.

8.6 Default Value After Power-on (RSTB Asserted)

PCI Configuration Space Table

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	VID	R	1	1	1	0	1	1	0	0
01h		R	0	0	0	1	0	0	0	0
02h	DID	R	0	0	1	0	1	0	0	1
03h		R	1	0	0	0	0	0	0	1
04h	Command	R	0	0	0	0	0	0	0	0
		W	-	PERRSP	-	MWIEN	-	BMEN	MEMEN	IOEN
05h		R	0	0	0	0	0	0	0	0
		W	-	-	-	-	-	-	-	SERREN
06h	Status	R	0	0	0	NewCap	0	0	0	0
07h		R	0	0	0	0	0	0	1	0
		W	DPERR	SSERR	RMABT	RTABT	STABT	-	-	DPD
08h	Revision ID	R	0	0	0	1	0	0	0	0
09h	PIFR	R	0	0	0	0	0	0	0	0
0Ah	SCR	R	0	0	0	0	0	0	0	0
0Bh	BCR	R	0	0	0	0	0	0	1	0
0Ch	CLS	R/W	0	0	0	0	0	0	0	0
0Dh	LTR	R	0	0	0	0	0	0	0	0
		W	LTR7	LTR6	LTR5	LTR4	LTR3	LTP2	LTR1	LTR0
0Eh	HTR	R	0	0	0	0	0	0	0	0
0Fh	BIST	R	0	0	0	0	0	0	0	0
10h	IOAR	R	0	0	0	0	0	0	0	1
11h		R/W	0	0	0	0	0	0	0	0
12h		R/W	0	0	0	0	0	0	0	0
13h		R/W	0	0	0	0	0	0	0	0
14h	MEMAR	R	0	0	0	0	0	0	0	0
15h		R/W	0	0	0	0	0	0	0	0
16h		R/W	0	0	0	0	0	0	0	0
17h		R/W	0	0	0	0	0	0	0	0
18h | 27h	-	RESERVED(ALL 0)								
28h	CISPtr	R	0	0	0	0	0	0	0	0
29h		R	0	0	0	0	0	0	0	0
2Ah		R	0	0	0	0	0	0	0	0
2Bh		R	0	0	0	0	0	0	0	0
2Ch	SVID	R	1	1	1	0	1	1	0	0
2Dh		R	0	0	0	1	0	0	0	0
2Eh	SMID	R	0	0	1	0	1	0	0	1
2Fh		R	1	0	0	0	0	0	0	1
30h	BMAR	R	0	0	0	0	0	0	0	0
		W	-	-	-	-	-	-	-	BROMEN
31h		R	0	0	0	0	0	0	0	0
		W	BMAR15	BMAR14	BMAR13	BMAR12	BMAR11	-	-	-
32h		R/W	0	0	0	0	0	0	0	0
33h		R/W	0	0	0	0	0	0	0	0
34h	Cap-Ptr	R	Ptr7	Ptr6	Ptr5	Ptr4	Ptr3	Ptr2	Ptr1	Ptr0

cont...

35h | 3Bh	-	RESERVED(ALL 0)								
3Ch	ILR	R/W	0	0	0	0	0	0	0	0
3Dh	IPR	R	0	0	0	0	0	0	0	1
3Eh	MNGNT	R	0	0	1	0	0	0	0	0
3Fh	MXLAT	R	0	0	1	0	0	0	0	0
40h | FFh	-	RESERVED(ALL 0)								

8.7 Power Management functions

The RTL8169 is compliant to ACPI (Rev 1.0, 1.0b, 2.0), PCI Power Management (Rev 1.1), and Network Device Class Power Management Reference Specification (V1.0a), such as to support OS Directed Power Management (OSPM) environment. To support this, the RTL8169 provides the following capabilities:

- The RTL8169 can monitor the network for a Wakeup Frame, a Magic Packet, or a Re-LinkOk, and notify the system via PME# when such a packet or event occurs. Then, the whole system can be restore to a working state to process the incoming jobs.

When the RTL8169 is in power down mode (D1 ~ D3):

- The Rx state machine is stopped, and the RTL8169 keeps monitoring the network for wakeup events such as Magic Packet, Wakeup Frame, and/or Re-LinkOk, in order to wake up the system. When in power down mode, the RTL8169 will not reflect the status of any incoming packets in the ISR register and will not receive any packets into the Rx FIFO.
- The FIFO status and the packets which are already received into Rx FIFO before entering into power down mode, are kept by the RTL8169 during power down mode
- Transmission is stopped. The action of the PCI bus master mode is stopped, too. The Tx FIFO is kept.
- After restoration to a D0 state, the PCI bus master mode continues to transfer the data, which is not yet moved into the Tx FIFO from the last break. The packet that was not transmitted completely last time is transmitted again.

D3cold_support_PME bit(bit15, PMC register) & Aux_I_b2:0 (bit8:6, PMC register) in PCI configuration space.
If EEPROM D3cold_support_PME bit(bit15, PMC) = 1, the above 4 bits depend on the existence of Aux power.
If EEPROM D3cold_support_PME bit(bit15, PMC) = 0, the above 4 bits are all 0's.
Ex.:

1. If EEPROM D3c_support_PME = 1,
   - If Aux. power exists, then PMC in PCI config space is the same as EEPROM PMC, i.e. if EEPROM PMC = C2 F7, then PCI PMC = C2 F7.
   - If Aux. power is absent, then PMC in PCI config space is the same as EEPROM PMC except the above 4 bits are all 0's. I.e. if EEPROM PMC = C2 F7, the PCI PMC = 02 76.
     - In this case, if wakeup support is desired when the main power is off, it is suggested that the EEPROM PMC be set to: C2 F7 (RT EEPROM default value).
2. If EEPROM D3c_support_PME = 0,
   - If Aux. power exists, then PMC in PCI config space is the same as EEPROM PMC. I.e. if EEPROM PMC = C2 77, then PCI PMC = C2 77.
   - If Aux. power is absent, then PMC in PCI config space is the same as EEPROM PMC except the above 4 bits are all 0's. I.e. if EEPROM PMC = C2 77, the PCI PMC = 02 76.
     - In this case, if wakeup support is not desired when the main power is off, it is suggested that the EEPROM PMC be set to be 02 76.

Link Wakeup occurs only when the following conditions are met:

- The LinkUp bit (CONFIG3#4) is set to 1, the PMEn bit (CONFIG1#0) is set to 1, and the PME# can be asserted in current power state.
- The Link status is re-established.

Magic Packet Wakeup occurs only when the following conditions are met:

- The destination address of the received Magic Packet is acceptable to the RTL8169, such as broadcast, multicast, or unicast address to the current RTL8169 adapter.
- The received Magic Packet does not contain a CRC error.
- The Magic bit (CONFIG3#5) is set to 1, the PMEn bit (CONFIG1#0) is set to 1, and the PME# can be asserted in current power state.
- The Magic Packet pattern matches, i.e. 6 * FFh + MISC(can be none)+ 16 * DID(Destination ID) in any part of a valid (Fast) Ethernet packet.

Wakeup Frame event occurs only when the following conditions are met:

- The destination address of the received Wakeup Frame is acceptable to the RTL8169, such as broadcast, multicast, or unicast address to the current RTL8169 adapter.
- The received Wakeup Frame does not contain a CRC error.
- The PMEn bit (CONFIG1#0) is set to 1.
- The **16-bit CRC*** (or **16-bit CRC**) of the received Wakeup Frame matches with the **16-bit CRC*** of the sample Wakeup Frame pattern given by the local machine's OS. Or, the RTL8169 is configured to allow direct packet wakeup, such as broadcast, multicast, or unicast network packet.

  - **16-bit CRC:**

    The RTL8169 supports 5 wakeup frames that includes 2 normal wakeup frames (covering 64 mask bytes from offset 0 to 63 of any incoming network packet) and 3 long wakeup frames (covering 128 mask bytes from offset 0 to 127 of any incoming network packet).

The PME# signal is asserted only when the following conditions are met:

- The PMEn bit (bit0, CONFIG1) is set to 1.
- The PME_En bit (bit8, PMCSR) in PCI Configuration Space is set to 1.
- The RTL8169 may assert PME# in current power state, or the RTL8169 is in isolation state, referring to PME_Support(bit15-11) of the PMC register in PCI Configuration Space.
- Magic Packet, LinkUp, or Wakeup Frame has occurred.

  * Writing a 1 to the PME_Status (bit15) of PMCSR register in the PCI Configuration Space will clear this bit and cause the RTL8169 to stop asserting a PME# (if enabled).

When the RTL8169 is in power down mode, ex. D1-D3, the IO, MEM, and Boot ROM spaces are all disabled, after a RST# assertion, the RTL8169's power state is restored to D0 automatically, if the original power state is $D3_{cold}$. There is no hardware delay at the RTL8169's power state transition. When in ACPI mode, the RTL8169 does not support PME from D0 (This is Realtek default setting of PMC register autoloaded from EEPROM. The setting may be changed from the EEPROM, if required.).

The RTL8169 also supports the legacy LAN WAKE-UP function. The LWAKE pin is used to notify legacy motherboards to execute the wake-up process whenever the RTL8169 receives a wakeup event, such as Magic Packet.

The LWAKE signal is asserted according the following setting.

- LWPME bit (bit4, CONFIG4):
  1: The LWAKE can only be asserted when the PMEB is asserted and the ISOLATEB is low.
  0: The LWAKE is asserted whenever there is wakeup event occurs.
- Bit1 of DELAY byte(offset 1Fh, EEPROM):
  1: LWAKE signal is enabled
  0: LWAKE signal is disabled.

8.8 Vital Product Data (VPD)

Bit 31 of the VPD is used to issue VPD read/write command and is also a flag used to indicate whether the transfer of data between the VPD data register and the 93C46/93C56 is completed or not.

1. Write VPD register: (write data to 93C46/93C56)
   Set the flag bit to 1 at the same time the VPD address is written to write VPD data to EEPROM. When the flag bit is reset to 0 by the RTL8169, the VPD data (4 bytes per VPD access) has been transferred from the VPD data register to EEPROM.
2. Read VPD register: (read data from 93C46/93C56)
   Reset the flag bit to 0 at the same time the VPD address is written to retrieve VPD data from EEPROM. When the flag bit is set to 1 by the RTL8169, the VPD data (4 bytes per VPD access) has been transferred from EEPROM to the VPD data register.

- Please refer to PCI Configuration Space Table in Section 8.1 and PCI 2.2 Specifications for further information.
- The VPD address does not have to be a DWORD-aligned address as defined in the PCI 2.2 Specifications, but the VPD data is always consecutive 4-byte data starting from the VPD address specified.
- Realtek reserves offset 40h to 7Fh in EEPROM mainly for VPD data to be stored.
- The VPD function of the RTL8169 is designed to be able to access the full range of the EEPROM (either 93C46 or 93C56).

9. Functional Description

9.1 Transmit & Receive Operations

The RTL8169 supports a new descriptor-based buffer management that will significantly reduce host CPU utilization and is more suitable for a server application. The new buffer management algorithm provides capabilities of Microsoft Large-Send offload, IP checksum offload, TCP checksum offload, UDP checksum offload, and IEEE802.1P, 802.1Q VLAN tagging. The RTL8169 supports up to 1024 consecutive descriptors in memory for transmit and receive separately, which means there might be 3 descriptor rings, one is a high priority transmit descriptor ring, another is a normal priority transmit descriptor ring, and the other is a receive descriptor ring, each descriptor ring may consist of up to 1024 4-double-word consecutive descriptors. Each descriptor consists of 4 consecutive double words. The start address of each descriptor group should be 256-byte alignment. Software must pre-allocate enough buffers and configure all descriptor rings before transmitting and/or receiving packets. Descriptors can be chained to form a packet in both Tx and Rx. Please refer to the Realtek RTL8169 programming guide for detailed information. Any Tx buffers pointed to by one of Tx descriptors should be at least 4 bytes.

Padding: The RTL8169 will automatically pad any packets less than 64 bytes (including 4 bytes CRC) to 64-byte long (including 4-byte CRC) before transmitting that packet onto network medium.

If a packet consists of 2 or more descriptors, then the descriptors in command mode should have the same configuration, except EOR, FS, LS bits.

9.1.1 Transmit

This portion implements the transmit portion of 802.3 Media Access Control. The Tx MAC retrieves packet data from the Tx Buffer Manager and sends it out through the transmit physical layer interface. Additionally, the Tx MAC provides MIB control information for transmit packets. The Tx MAC supports 4-bit MII, 8-bit GMII, and 10-bit TBI interfaces to physical layer devices.

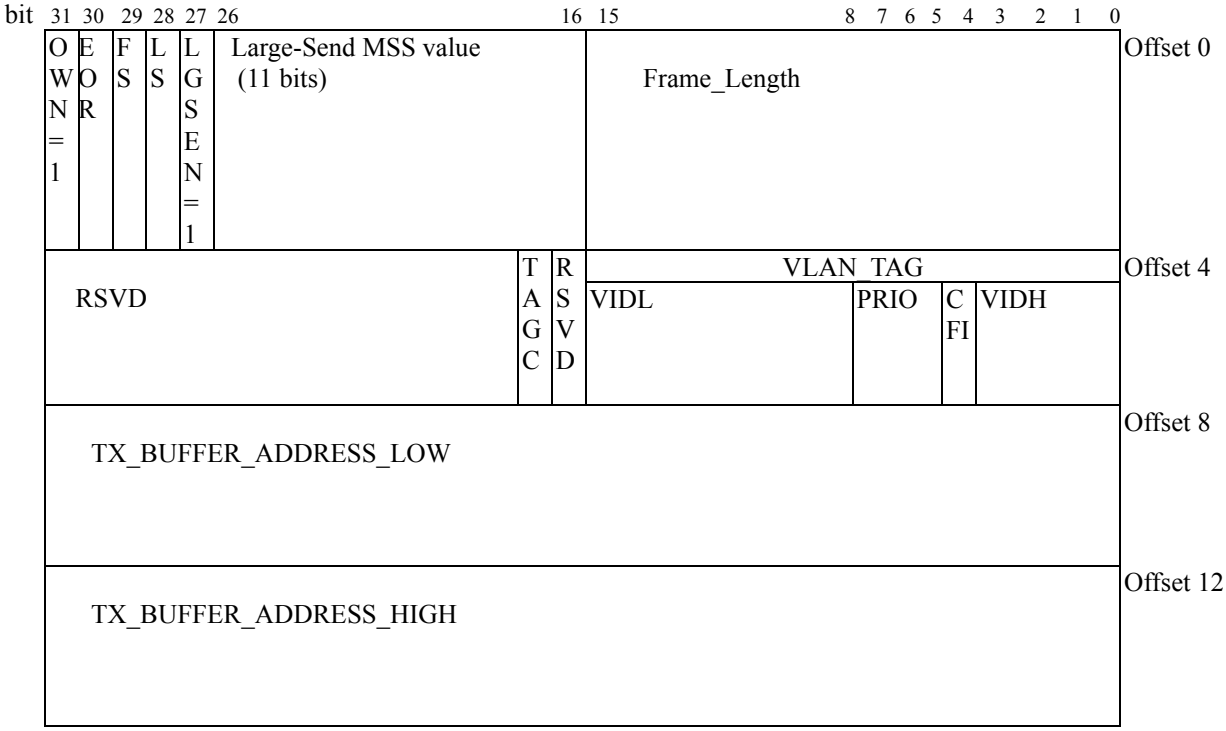
The Tx MAC has the capability to insert a 4-byte VLAN tag in the transmit packet. If Tx VLAN Tag insertion is enabled, the MAC will insert the 4 bytes, as specified in the VTAG register, following the source and destination addresses of the packet. The VLAN tag insertion can be enabled on a global or per-packet basis.

When operating in 1G mode, the RTL8169 operates in full duplex mode only.

The Tx MAC supports task offloading of IP, TCP, and UDP checksum generation. It can generate the checksums and insert them into the packet. The checksum generation can be enabled on a global or per-packet basis.

The following information describes what the Tx descriptor may look like, depending on different states in each Tx descriptor. The minimum Tx buffer should be at least 4 bytes.

Large-Send Task Offload Tx Descriptor Format (before transmitting, OWN=1, LGSEN=1, Tx command mode 0)

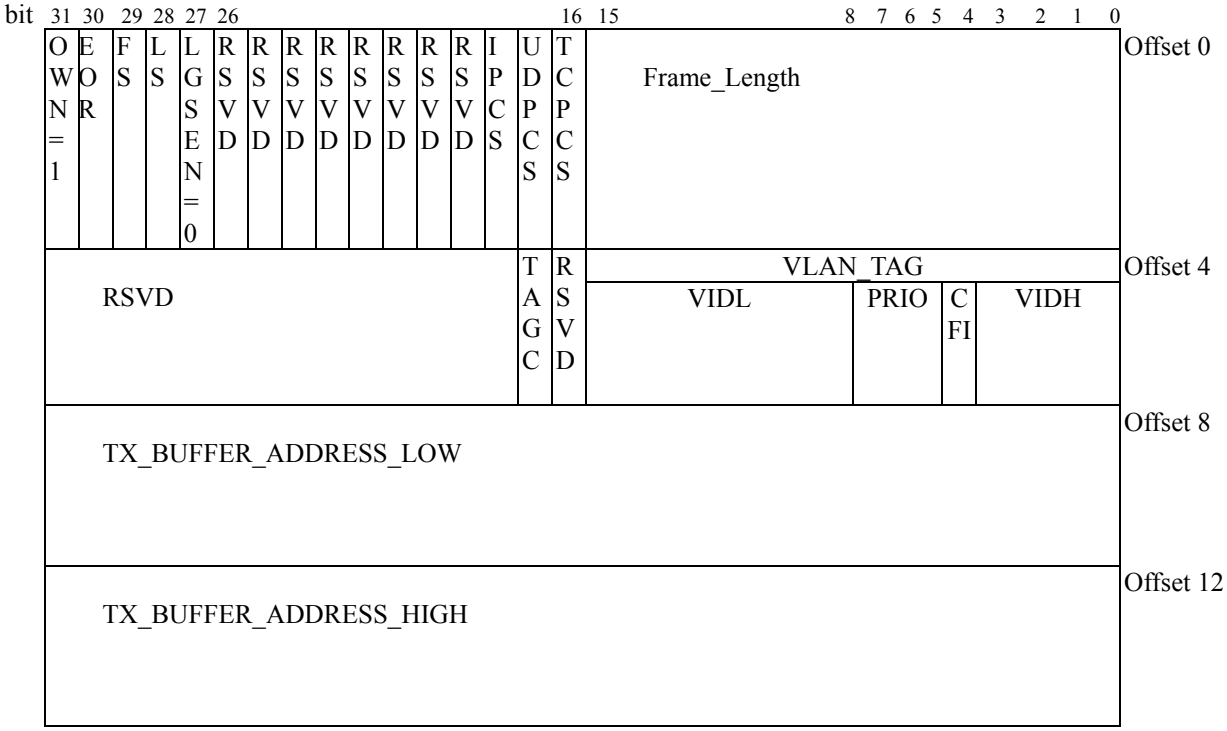


Offset#	Bit#	Symbol	Description
0	31	OWN	**Ownership:** This bit, when set, indicates that the descriptor is owned by THE NIC, and the data relative to this descriptor is ready to be transmitted. When cleared, it indicates that the descriptor is owned by host system. The NIC clears this bit when the relative buffer data is transmitted. In this case, OWN=1.
0	30	EOR	**End of Descriptor Ring:** This bit, when set, indicates that this is the last descriptor in descriptor ring. When the NIC's internal transmit pointer reaches here, the pointer will return to the first descriptor of the descriptor ring after transmitting the data relative to this descriptor.
0	29	FS	**First Segment Descriptor:** This bit, when set, indicates that this is the first descriptor of a Tx packet, and that this descriptor is pointing to the first segment of the packet.
0	28	LS	**Last Segment Descriptor:** This bit, when set, indicates that this is the last descriptor of a Tx packet, and that this descriptor is pointing to the last segment of the packet.
0	27	LGSEN	**Large Send:** A command bit; TCP/IP Large send operation enable. The driver sets this bit to ask the NIC to offload the Large send operation. In this case, LGSEN=1.
0	26:16	MSS	**Maximum Segmentation Size:** An 11-bit long command field, the driver passes large send MSS to the NIC through this field.
0	15:0	Frame_Length	**Transmit Drame Length:** This field indicates the length in TX buffer, in byte, to be transmitted
4	31:18	RSVD	**Reserved**

cont...

4	17	TAGC	**VLAN tag control bit:** 1: Enable; 0: Disable. 1: Add TAG. 0x8100 (Ethernet encoded tag protocol ID, indicating that this is a IEEE 802.1Q VLAN packet) is inserted after source address, and 2 bytes are inserted after tag protocol ID from VLAN_TAG field in transmit descriptor. 0: Packet remains unchanged when transmitting. I.e., the packet transmitted is the same as it was passed down by upper layer.
4	16	RSVD	**Reserved**
4	15:0	VLAN_TAG	The 2-byte VLAN_TAG contains information, from the upper layer, of user priority, canonical format indication, and VLAN ID. Please refer to IEEE 802.1Q for more VLAN tag information. VIDH: The high 4 bits of a 12-bit VLAN ID. VIDL: The low 8 bits of a 12-bit VLAN ID. PRIO: 3-bit 8-level priority. CFI: Canonical Format Indicator.
8	31:0	TxBuffL	**Low 32-bit address of transmit buffer**
12	31:0	TxBuffH	**High 32-bit address of transmit buffer**

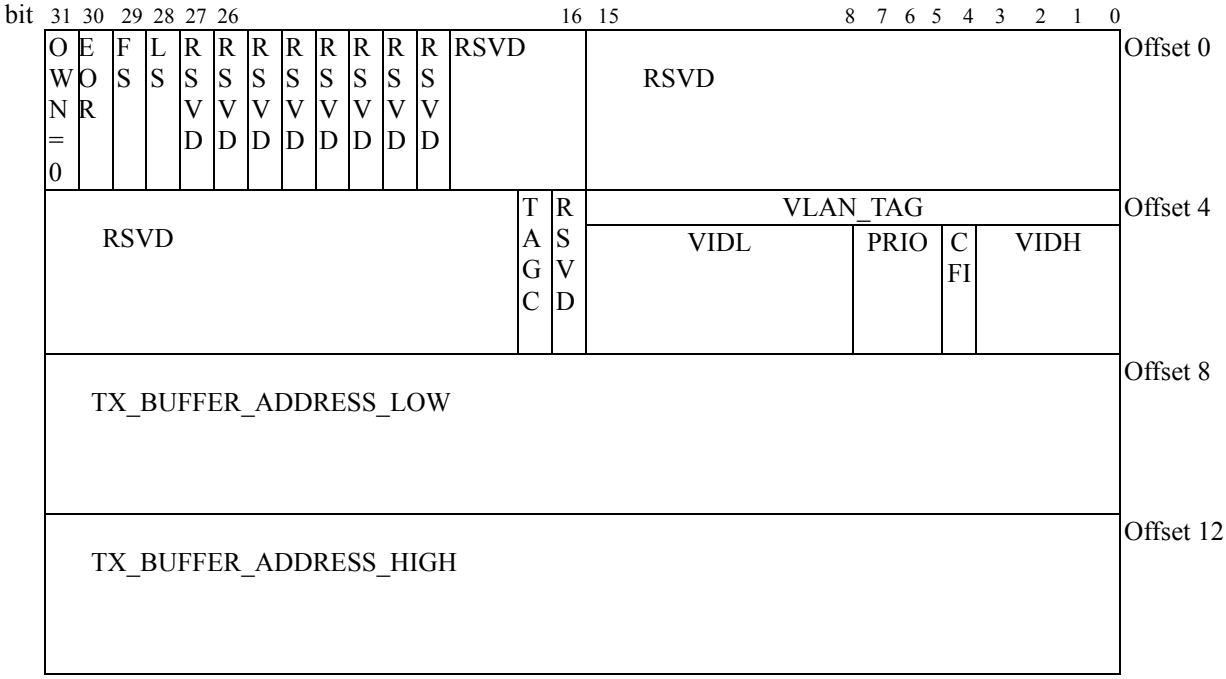
Normal (including IP, TCP, UDP Checksum Task Offloads) Tx Descriptor Format (before transmitting, OWN=1, LGSEN=0, Tx command mode 1)



Offset#	Bit#	Symbol	Description
0	31	OWN	**Ownership:** This bit, when set, indicates that the descriptor is owned by the NIC, and that the data relative to this descriptor is ready to be transmitted. When cleared, it indicates that the descriptor is owned by the host system. The NIC clears this bit when the relative buffer data is transmitted. In this case, OWN=1.
0	30	EOR	**End of descriptor Ring:** This bit, when set, indicates that this is the last descriptor in the descriptor ring. When the NIC's internal transmit pointer reaches here, the pointer will return to the first descriptor of the descriptor ring after transmitting the data relative to this descriptor.
0	29	FS	**First segment descriptor:** This bit, when set, indicates that this is the first descriptor of a Tx packet, and that this descriptor is pointing to the first segment of the packet.
0	28	LS	**Last segment descriptor:** This bit, when set, indicates that this is the last descriptor of a Tx packet, and that this descriptor is pointing to the last segment of the packet.
0	27	LGSEN	**Large Send:** A command bit; TCP/IP Large send operation enable. Driver sets this bit to ask NIC to offload Large send operation. In this case, LGSEN=0.
0	26:19	RSVD	**Reserved**
0	18	IPCS	**IP checksum offload:** A command bit. The driver sets this bit to ask the NIC to offload the IP checksum.
0	17	UDPCS	**UDP checksum offload:** A command bit. The driver sets this bit to ask the NIC to offload the UDP checksum.
0	16	TCPCS	**TCP checksum offload enable:** A command bit; The driver sets this bit to ask the NIC to offload the TCP checksum.
0	15:0	Frame_Length	**Transmit frame length:** This field indicates the length of the TX buffer, in bytes, to be transmitted
4	31:18	RSVD	**Reserved**
4	17	TAGC	**VLAN tag control bit:** 1: Enable; 0: Disable. 1: Add TAG. 0x8100 (Ethernet encoded tag protocol ID, indicating that this is an IEEE 802.1Q VLAN packet) is inserted after the source address, and 2 bytes are inserted after tag protocol ID from the VLAN_TAG field in transmit descriptor. 0: Packet remains unchanged when transmitting. I.e., the packet transmitted is the same as it was passed down by upper layer.
4	16	RSVD	**Reserved**
4	15:0	VLAN_TAG	**VLAN Tag:** The 2-byte VLAN_TAG contains information, from upper layer, of user priority, canonical format indicator, and VLAN ID. Please refer to IEEE 802.1Q for more VLAN tag information. VIDH: The high 4 bits of a 12-bit VLAN ID. VIDL: The low 8 bits of a 12-bit VLAN ID. PRIO: 3-bit 8-level priority. CFI: Canonical Format Indicator.
8	31:0	TxBuffL	**Low 32-bit address of transmit buffer**
12	31:0	TxBuffH	**High 32-bit address of transmit buffer**

Tx Status Descriptor (after transmitting, OWN=0, Tx status mode)

After having transmitted, the Tx descriptor turns into a Tx status descriptor.



Offset#	Bit#	Symbol	Description
0	31	OWN	**Ownership:** This bit, when set, indicates that the descriptor is owned by the NIC. When cleared, it indicates that the descriptor is owned by the host system. NIC clears this bit when the relative buffer data is already transmitted. In this case, OWN=0.
0	30	EOR	**End of Descriptor Ring:** When set, indicates that this is the last descriptor in descriptor ring. When NIC's internal transmit pointer reaches here, the pointer will return to the first descriptor of the descriptor ring after transmitting the data relative to this descriptor.
0	29	FS	**First Segment Descriptor:** This bit, when set, indicates that this is the first descriptor of a Tx packet, and that this descriptor is pointing to the first segment of the packet.
0	28	LS	**Last Segment Descriptor:** This bit, when set, indicates that this is the last descriptor of a Tx packet, and that this descriptor is pointing to the last segment of the packet.
0	27:0	RSVD	**Reserved**
4	31:18	RSVD	**Reserved**
4	17	TAGC	**VLAN Tag Control Bit:** 1: Enable; 0: Disable. 1: Add TAG. 0x8100 (Ethernet encoded tag protocol ID, indicating that this is an IEEE 802.1Q VLAN packet) is inserted after source address, and 2 bytes are inserted after tag protocol ID from VLAN_TAG field in transmit descriptor. 0: Packet remains unchanged when transmitting. I.e., the packet transmitted is the same as it was passed down by the upper layer.
4	16	RSVD	**Reserved**

cont...

4	15:0	VLAN_TAG	**VLAN Tag:** The 2-byte VLAN_TAG contains information, from the upper layer, of user priority, canonical format indicator, and VLAN ID. Please refer to IEEE 802.1Q for more VLAN tag information. VIDH: The high 4 bits of a 12-bit VLAN ID. VIDL: The low 8 bits of a 12-bit VLAN ID. PRIO: 3-bit 8-level priority. CFI: Canonical Format Indicator.
8	31:0	TxBuffL	**Low 32-bit address of transmit buffer**
12	31:0	TxBuffH	**High 32-bit address of transmit buffer**

9.1.2 Receive

The receive portion implements the receive portion of 802.3 Media Access Control. The Rx MAC retrieves packet data from the receive portion and sends it to the Rx Buffer Manager. Additionally, the Rx MAC provides MIB control information and packet address data for the Rx Filter. The Rx MAC supports 4-bit MII, 8-bit GMII, and 10-bit TBI interfaces to physical layer devices.

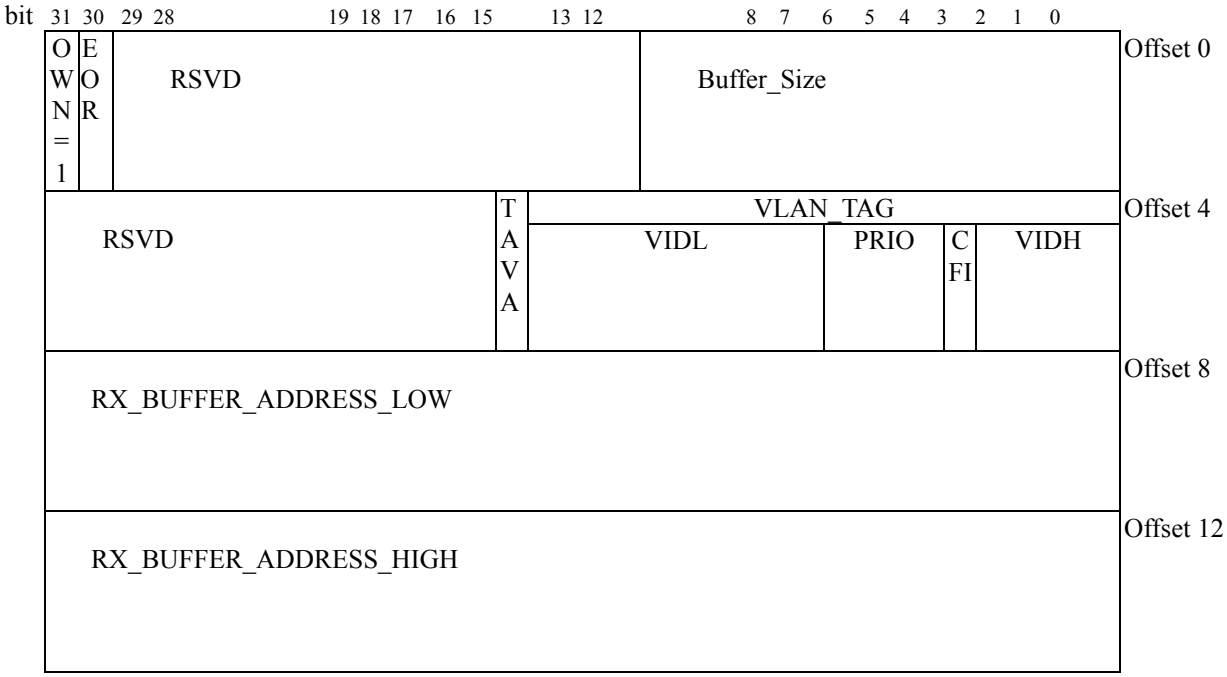
The Rx MAC can detect packets containing a 4-byte VLAN tag, and remove the VLAN tag from the received packet. If Rx VLAN Tag Removal is enabled, then the 4 bytes following the source and destination addresses will be stripped out. The VLAN status can be returned in the VLAN Tag field.

The Rx MAC supports IP checksum verification. It can validate IP checksums as well as TCP and UDP checksums. Packets can be discarded based on detecting checksum errors.

The following information describes what the Rx descriptor may look like, depending on different states in each Rx descriptor. Any Rx buffers pointed to by one of the Rx descriptors should be to at least 8 bytes in length and to 8-byte alignment in memory.

Rx Command Descriptor (OWN=1)

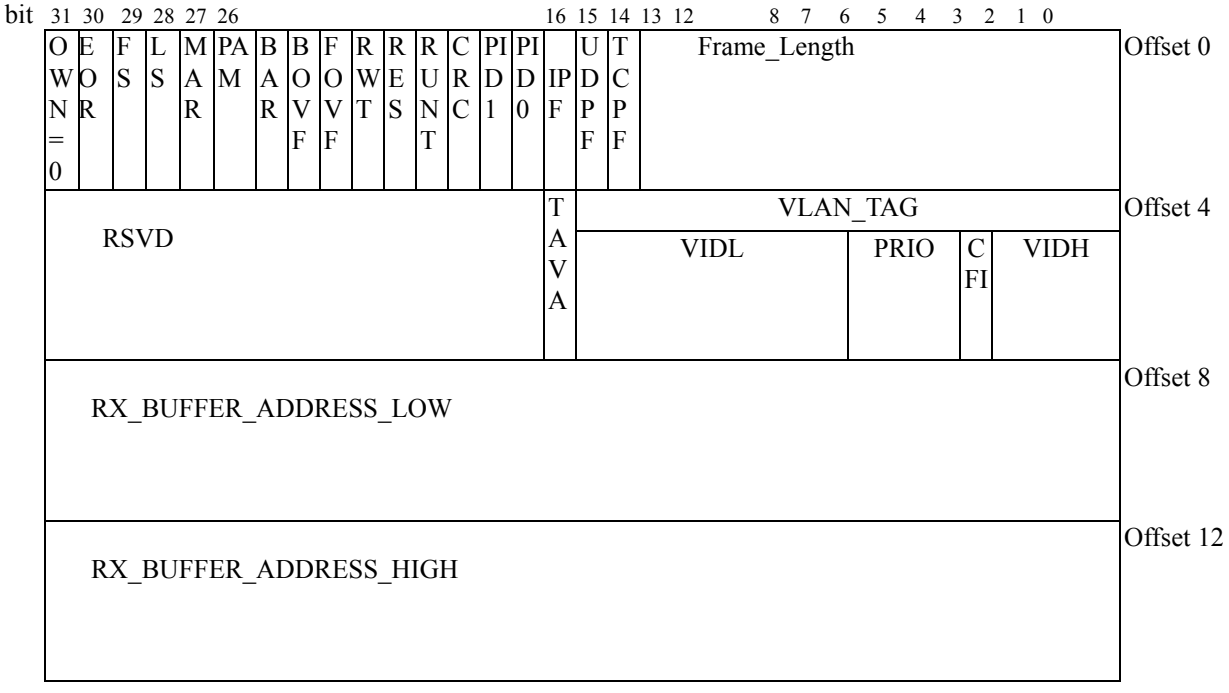
The driver should pre-allocate Rx buffers and configure Rx descriptors before packet reception. The following describes what Rx descriptors may look like before packet reception.



Offset#	Bit#	Symbol	Description
0	31	OWN	**Ownership:** This bit, when set, indicates that the descriptor is owned by the NIC, and is ready to receive a packet. The OWN bit is set by the driver after having pre-allocated the buffer at initialization, or the host has released the buffer to the driver. In this case, OWN=1.
0	30	EOR	**End of Rx descriptor Ring:** This bit, set to 1 indicates that this descriptor is the last descriptor of the Rx descriptor ring. Once the NIC's internal receive descriptor pointer reaches here, it will return to the first descriptor of the Rx descriptor ring after this descriptor is used by packet reception.
0	29:14	RSVD	**Reserved**
0	13:0	Buffer_Size	**Buffer Size:** This field indicate the receive buffer size in bytes.
4	31:17	RSVD	**Reserved**
4	16	TAVA	**Tag Available:** This bit, when set, indicates that the received packet is an IEEE802.1Q VLAN TAG (0x8100) available packet.
4	15:0	VLAN_TAG	**VLAN Tag:** If the TAG of the packet is 0x8100, The RTL8169 MAC extracts four bytes from after source ID, sets the TAVA bit to 1, and moves the TAG value of this field in Rx descriptor. VIDH: The high 4 bits of a 12-bit VLAN ID. VIDL: The low 8 bits of a 12-bit VLAN ID. PRIO: 3-bit 8-level priority. CFI: Canonical Format Indicator.
8	31:0	RxBuffL	**Low 32-bit Address of Receive Buffer**
12	31:0	RxBuffH	**High 32-bit Address of Receive Buffer**

Rx Status Descriptor (OWN=0)

When packet is received, the Rx command descriptor turns to be a Rx status descriptor.



<table>
<tr><th>Offset#</th><th>Bit#</th><th>Symbol</th><th>Description</th></tr>
<tr><td>0</td><td>31</td><td>OWN</td><td>Ownership: This bit, when set, indicates that the descriptor is owned by the NIC. When cleared, it indicates that the descriptor is owned by the host system. The NIC clears this bit when the NIC has filled up this Rx buffer with a packet or part of a packet. In this case, OWN=0.</td></tr>
<tr><td>0</td><td>30</td><td>EOR</td><td>End of Rx Descriptor Ring: This bit, set to 1, indicates that this descriptor is the last descriptor of the Rx descriptor ring. Once the NIC's internal receive descriptor pointer reaches here, it will return to the first descriptor of the Rx descriptor ring after this descriptor is used by packet reception.</td></tr>
<tr><td>0</td><td>29</td><td>FS</td><td>First Segment descriptor: This bit, when set, indicates that this is the first descriptor of a received packet, and this descriptor is pointing to the first segment of the packet.</td></tr>
<tr><td>0</td><td>28</td><td>LS</td><td>Last Segment Descriptor: This bit, when set, indicates that this is the last descriptor of a received packet, and this descriptor is pointing to the last segment of the packet.</td></tr>
<tr><td>0</td><td>27</td><td>MAR</td><td>Multicast Address Packet Received: This bit, when set, indicates that a multicast packet has been received.</td></tr>
<tr><td>0</td><td>26</td><td>PAM</td><td>Physical Address Matched: This bit, when set, indicates that the destination address of this Rx packet matches the value in the RTL8169's ID registers.</td></tr>
<tr><td>0</td><td>25</td><td>BAR</td><td>Broadcast Address Received: This bit, when set, indicates that a broadcast packet has been received. BAR and MAR will not be set simultaneously.</td></tr>
<tr><td>0</td><td>24</td><td>BOVF</td><td>Buffer Overflow: This bit, when set, indicates that the receive buffer has been exhausted before this packet was received.</td></tr>
<tr><td>0</td><td>23</td><td>FOVF</td><td>FIFO Overflow: This bit, when set, indicates that a FIFO overflow has occurred before this packet was received.</td></tr>
<tr><td>0</td><td>22</td><td>RWT</td><td>Receive Watchdog Timer Expired: This bit, when set, indicates that the received packet length exceeded 4096 bytes.</td></tr>
<tr><td>0</td><td>21</td><td>RES</td><td>Receive Error Summary: This bit, when set, indicates that at least one of the following errors has occurred: CRC, RUNT, RWT, FAE. This bit is valid only when LS (Last segment bit) is set</td></tr>
<tr><td>0</td><td>20</td><td>RUNT</td><td>Runt Packet: This bit, when set, indicates that the received packet length is smaller than 64 bytes. RUNT packets are able to be received only when RCR_AR is set.</td></tr>
<tr><td>0</td><td>19</td><td>CRC</td><td>CRC Error: This bit, when set, indicates that a CRC error has occurred on the received packet. A CRC packet is able to be received only when RCR_AER is set.</td></tr>
<tr><td>0</td><td>18:17</td><td>PID1, PID0</td><td>Protocol ID1, Protocol ID0: These 2 bits indicate the protocol type of the packet received.
<table>
<tr><th></th><th>PID1</th><th>PID0</th></tr>
<tr><td>Non-IP</td><td>0</td><td>0</td></tr>
<tr><td>TCP/IP</td><td>0</td><td>1</td></tr>
<tr><td>UDP/IP</td><td>1</td><td>0</td></tr>
<tr><td>IP</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>0</td><td>16</td><td>IPF</td><td>IP Checksum Failure: 1: Failure, 0: No failure.</td></tr>
<tr><td>0</td><td>15</td><td>UDPF</td><td>UDP Checksum Failure: 1: Failure, 0: No failure.</td></tr>
<tr><td>0</td><td>14</td><td>TCPF</td><td>TCP Checksum Failure: 1: Failure, 0: No failure.</td></tr>
<tr><td>0</td><td>13:0</td><td>Frame_Length</td><td>When OWN=0 and LS =1, these bits indicate the received packet length including CRC, in bytes.</td></tr>
<tr><td>4</td><td>31:17</td><td>RSVD</td><td>Reserved</td></tr>
</table>

cont...

4	16	TAVA	**Tag Available:** When set, the received packet is an IEEE802.1Q VLAN TAG (0x8100) available packet.
4	15:0	VLAN_TAG	**VLAN Tag:** If the TAG of the packet is 0x8100, The RTL8169 MAC extracts four bytes from the after source ID, sets TAVA bit to 1, and moves the TAG value to this field in the Rx descriptor. VIDH: The high 4 bits of a 12-bit VLAN ID. VIDL: The low 8 bits of a 12-bit VLAN ID. PRIO: 3-bit 8-level priority. CFI: Canonical Format Indicator.
8	31:0	RxBuffL	**Low 32-bit Address of Receive Buffer**
12	31:0	RxBuffH	**High 32-bit Address of Receive Buffer**

9.2 Loopback Operation

Loopback mode is normally used to verify that the logic operations up to the Ethernet cable/fiber channel function correctly. The RTL8169 supports both internal and external loopback capabilities. The RTL8169 internal loopback is actually a digital loopback inside the RTL8169. To test an external loopback, the RTL8169 must operate in normal mode and the external PHYceiver should be configured in loopback mode.

9.3 Collision

If the RTL8169 is not in full-duplex mode, a collision event occurs when the receive input is not idle while the RTL8169 transmits. If the collision was detected during the preamble transmission, a jam pattern is transmitted after completing the preamble (including the JK symbol pair when network speed is 100Mbps). The RTL8169 does not support half-duplex mode in 1000Mbps mode. Therefore, there is no collision when the RTL8169 operates in 1000Mbps mode.

9.4 Flow Control

The RTL8169 supports IEEE802.3X flow control to improve performance in full-duplex mode. It detects and sends PAUSE packets to achieve the flow control task. Results from the N-Way process with the link partner determine if flow control is supported for the current connection.

9.4.1. Control Frame Transmission

When the RTL8169 is running out of receive descriptors in full duplex mode, it sends a PAUSE packet (with pause_time=FFFFh) to inform the source station to stop transmission for the specified period of time. Once the receive descriptors are available again, the RTL8169 sends another PAUSE packet (with pause_time=0000h) to wake up the source station to restart transmission.

9.4.2. Control Frame Reception

The RTL8169 enters backoff state for the specified period of time when it receives a valid PAUSE packet (with pause_time=n) in full duplex mode. If the PAUSE packet is received while the RTL8169 is transmitting, the RTL8169 starts to backoff after the current transmission is completed. The RTL8169 is free to transmit packets when it receives a valid PAUSE packet (with pause_time=0000h) or the backoff timer(=n*512 bit time) elapses.

The PAUSE operation cannot be used to inhibit transmission of MAC Control frames (e.g. a PAUSE packet). The N-way flow control capability can be disabled. Please refer to Section 7, EEPROM (93C46 or 93C56) Contents for further information.

9.5 Memory Functions

9.5.1 Memory Read Line (MRL)

The Memory Read Line command reads more than a longword (DWORD) up to the cache line boundary in a prefetchable address space. The Memory Read Line command is semantically identical to the Memory Read command except that it additionally indicates that the master intends to fetch a complete cache line. This command is intended to be used with bulk sequential data transfers where the memory system and the requesting master might gain some performance advantages by reading up to a cache line boundary in response to the request rather than a single memory cycle. As with the Memory Read command, pre-fetched buffers must be invalidated before any synchronization events are passed through this access path.

The RTL8169 performs MRL according to the following rules:

i. Read accesses that reach the cache line boundary use the Memory Read Line command (MRL) instead of the Memory Read command.
ii. Read accesses that do not reach the cache line boundary use the Memory Read (MR) command.
iii. The Memory Read Line (MRL) command operates in conjunction with the Memory Read Multiple command (MRM).
iv. The RTL8169 will terminate the read transaction on the cache line boundary when it is out of resources on the transmit DMA. For example, when the transmit FIFO is almost full.

9.5.2 Memory Read Multiple (MRM)

The Memory Read Multiple command is semantically identical to the Memory Read command except that it additionally indicates that the master may intend to fetch more than one cache line before disconnecting. The memory controller should continue pipelining memory requests as long as FRAMEB is asserted. This command is intended to be used with bulk sequential data transfers where the memory system and the requesting master might gain some performance advantage by sequentially reading ahead one or more additional cache line(s) when a software transparent buffer is available for temporary storage.

The RTL8169 performs MRM according to the following rules,

i. When the RTL8169 reads full cache lines, it will use the Memory Read Multiple command.
ii. If the memory buffer is not cache-aligned, the RTL8169 will use the Memory Read Line command to reach the cache line boundary first.

Example:

Assume the packet length = 1514 byte, cache line size = 16 longwords (DWORDs), and Tx buffer start address = 64m+4 (m > 0).

;Step1: Memory Read Line (MRL)
;Data: (0-3) => (4-7) => (8-11) =>……... => (56-59) (byte offset of the Tx packet)
;From Address: <64m+4>, <64m+8>, ……., <64m+60> (reach cache line boundary)
;Step2. Memory Read Multiple (MRM)
;Data: (60-63) => (64-67) => (68-71) => …….. => (1454-1467)
;From Address: <64m+64>, <64m+68>, ……., <64m+64+(16*4)*21+(16-1)*4>
;Step3. Memory Read(MR)
;Data: (1468-1471) => (1472-1475) => ……, => (1510-1513)
;From Address:<64m+64+(16*4)*22>,<64m+64+(16*4)*22+4>,..,<64m+64+(16*4)*22+42>
Step1: Memory Read Multiple (MRM)
Data: (0-3) => (4-7) => (8-11) =>…….. => (1454-1467)
From Address: <64m+4>, <64m+8>, ……., <64m+64+(16*4)*21+(16-1)*4>
Step2. Memory Read(MRL)
Data: (1468-1471) => (1472-1475) => ……, => (1510-1513)
From Address:<64m+64+(16*4)*22>,<64m+64+(16*4)*22+4>,..,<64m+64+(16*4)*22+42>

9.5.3 Memory Write and Invalidate (MWI)

The Memory Write and Invalidate command is semantically identical to the Memory Write command except that it additionally guarantees a minimum transfer of one complete cache line; i.e., the master intends to write all bytes within the addressed cache line in a single PCI transaction unless interrupted by the target. Note: All byte enables must be asserted during each data phase for this command. The master may allow the transaction to cross a cache line boundary only if it intends to transfer the entire next line also. This command requires implementation of a configuration register in the master indicating the cache line size and may only be used with Linear Burst Ordering. It allows a memory performance optimization by invalidating a "dirty" line in a write-back cache without requiring the actual write-back cycle, thus shortening access time. The RTL8169 uses the MWI command while writing full cache lines, and the Memory Write command while writing partial cache lines.

The RTL8169 issues MWI command, instead of MW command on Rx DMA when the following requirements are met:

i. The Cache Line Size written in offset 0Ch of the PCI configuration space is 8 or 16 longwords (DWORDs).
ii. The accessed address is cache line aligned.
iii. The RTL8169 has at least 8/16 longwords (DWORDs) of data in its Rx FIFO.
iv. The MWI (bit 4) in the PCI Configuration Command register should be set to 1.

The RTL8169 uses the Memory Write (MW) command instead of the MWI whenever there any one of the above listed requirements has failed. The RTL8169 terminates the WMI cycle at the end of the cache line when a WMI cycle has started and at least one of the requirements are no longer held.

Example:

Assume Rx packet length = 1514 byte, cache line size = 16 DWORDs (longwords), and Rx buffer start address = 64m+4 (m > 0).

Step1: Memory Write (MW)
Data: (0-3) => (4-7) => (8-11) => ……... => (56-59) (byte offset of the Rx packet)
To Address: <64m+4>, <64m+8>, ……., <64m+60> (reach cache line boundary)
Step2. Memory Write and Invalidate (MWI)
Data: (60-63) => (64-67) => (68-71) => ……..…..... => (1454-1457)
To Address: <64m+64>, <64m+68>, ……..…..., <64m+64+(16*4)*21+(16-1)*4>
Step3. Memory Write(MW)
Data: (1458-1461) => (1462-1465) => ……..…….... => (1512-1513)
To Address: <64m+64+(16*4)*22>, <64m+64+(16*4)*22+4>, , <64m+64+(16*4)*22+42>

9.5.4 Dual Address Cycle (DAC)

The Dual Address Cycle (DAC) command is used to transfer a 64-bit address to devices that support 64-bit addressing when the address is not in the low 4 GB address space. The RTL8169 is capable of performing DAC, such that it is very competent as a network server card in a heavy-duty server with the possibility of allocating a memory buffer above a 4GB memory address space.

9.6 LED Functions

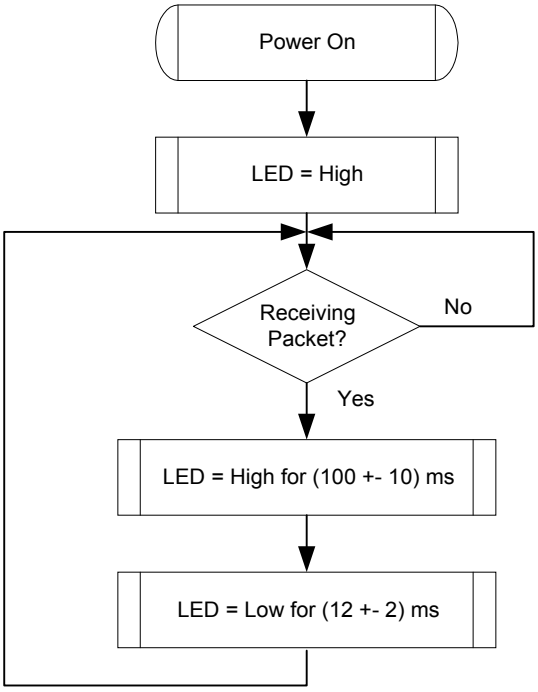
The RTL8169 supports 4 LED signals in 4 different configurable operation modes. The following sections describe the different LED actions.

9.6.1 Link Monitor

The Link Monitor senses the link integrity or if a station is down, such as LINK10, LINK100, LINK1000, LINK10/100/1000, LINK10/ACT, LINK100/ACT, or LINK1000/ACT. Whenever link status is established, the specific link LED pin is driven low. Once a cable is disconnected, the link LED pin is driven high indicating that no network connection exists.

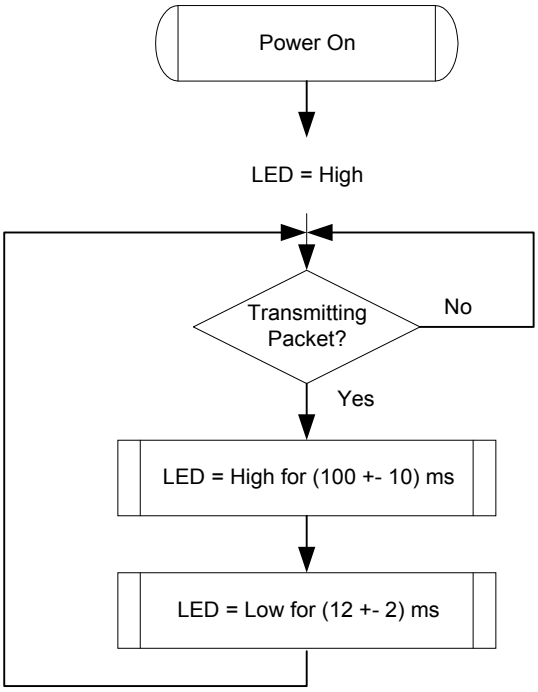
9.6.2 Rx LED

In 10/100/1000Mbps mode, blinking of the Rx LED indicates that receive activity is occurring.



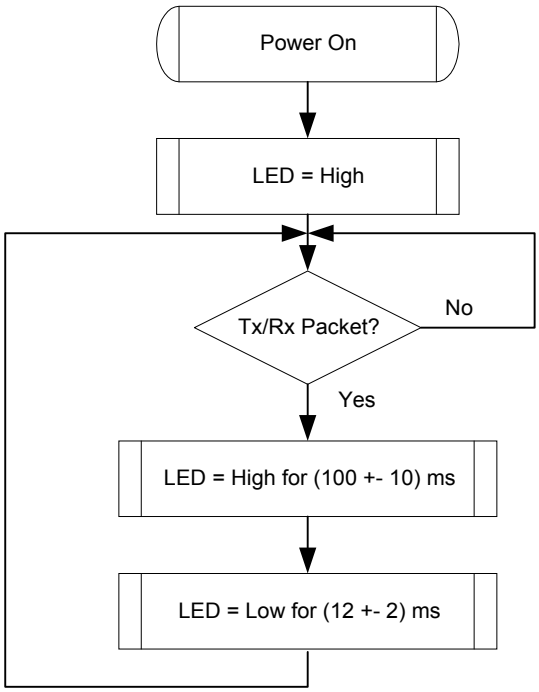
9.6.3 Tx LED

In 10/100/1000Mbps mode, blinking of the Tx LED indicates that transmit activity is occurring.



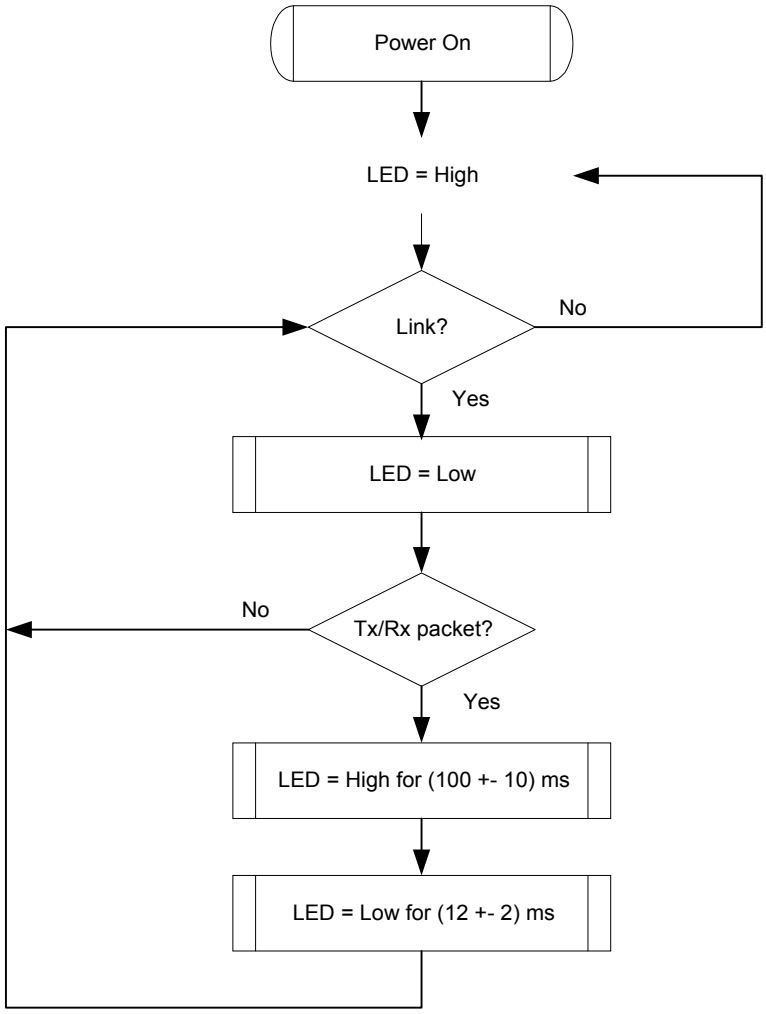
9.6.4 Tx/Rx LED

In 10/100/1000Mbps mode, blinking of the Tx/Rx LED indicates that both transmit and receive activity is occurring.



9.6.5 LINK/ACT LED

In 10/100/1000Mbps mode, blinking of the LINK/ACT LED indicates that the RTL8169 is linked and operating properly. This LED high for extended periods, indicates that a link problem exists.



9.7 Physical Layer Interfaces

The RTL8169 supports standard media independent MII and GMII for 10Mbps, 100Mbps, and 1000Mbps applications. The RTL8169 also supports TBI (Ten-Bit Interface) for 1000Base-X applications by connecting to industry standard external SERDES devices for fiber applications. The RTL8169 only operates in full-duplex mode in 1000Mbps for both GMII and TBI applications. In addition, a management interface is defined for MII and GMII.

9.7.1 Media Independent Interface (MII)

The RTL81689 supports 10Mbps and 100Mbps physical layer devices through the MII as defined in the IEEE 802.3 (clause 22) specifications. The MII consists of a transmit data interface (TxEN, TxER, TXD[3:0], and TxCLK), a receive data interface (RxDV, RxER, RXD[3:0], and RxCLK), 2 status signals (CRS and COL) and a management interface (MDC and MDIO). In this mode of operation, both Transmit and Receive clocks are supplied by the PHY.

9.7.2 Gigabit Media Independent Interface (GMII)

The RTL81689 can support 1000Mbps physical layer devices through the GMII as defined in the IEEE 802.3 (clause 35) specifications. The GMII extends from the MII to use 8-bit data interfaces and to operate at a higher frequency. The GMII consists of a transmit data interface (TxEN, TxER, TXD[7:0], and GTxCLK), a receive data interface (RxDV, RxER, RXD[7:0], and RxCLK), 2 status signals (CRS and COL) and a management interface (MDC and MDIO). Many of the signals are shared with the MII interface. One significant difference is the Transmit clock (GTxCLK) is supplied by the RTL81689 instead of the PHY. The management interface (described later) is the same in both MII and GMII modes

9.7.3 Ten Bit Interface (TBI)

The TBI provides a port for transmit and receive data for interfacing to devices that support the 1000Base-X portion of the 802.3 specifications. This includes 1000Base-FX fiber devices. The port consists of data paths that are 10 bits wide in each direction as well as control signals. This interface shares pins with the MII and GMII interfaces.

9.7.4 MII/GMII Management Interface

The MII/GMII management interface utilizes a communication protocol similar to a serial EEPROM. Signaling occurs on two signals: clock (MDC) and data (MDIO). This protocol provides capability for addressing up to 32 individual Physical Media Dependent (PMD) devices which share the same serial interface, and for addressing up to 32 16-bit read/write registers within each PMD. The MII management protocol utilizes the following frame format: start bits (SB), opcode (OP), PMD address (PA), register address (RA), line turnaround (LT) and data, as shown below.

SB	OP	PA	RA	LT	Data
2 bits	2 bits	5 bits	5 bits	2 bits	16 bits

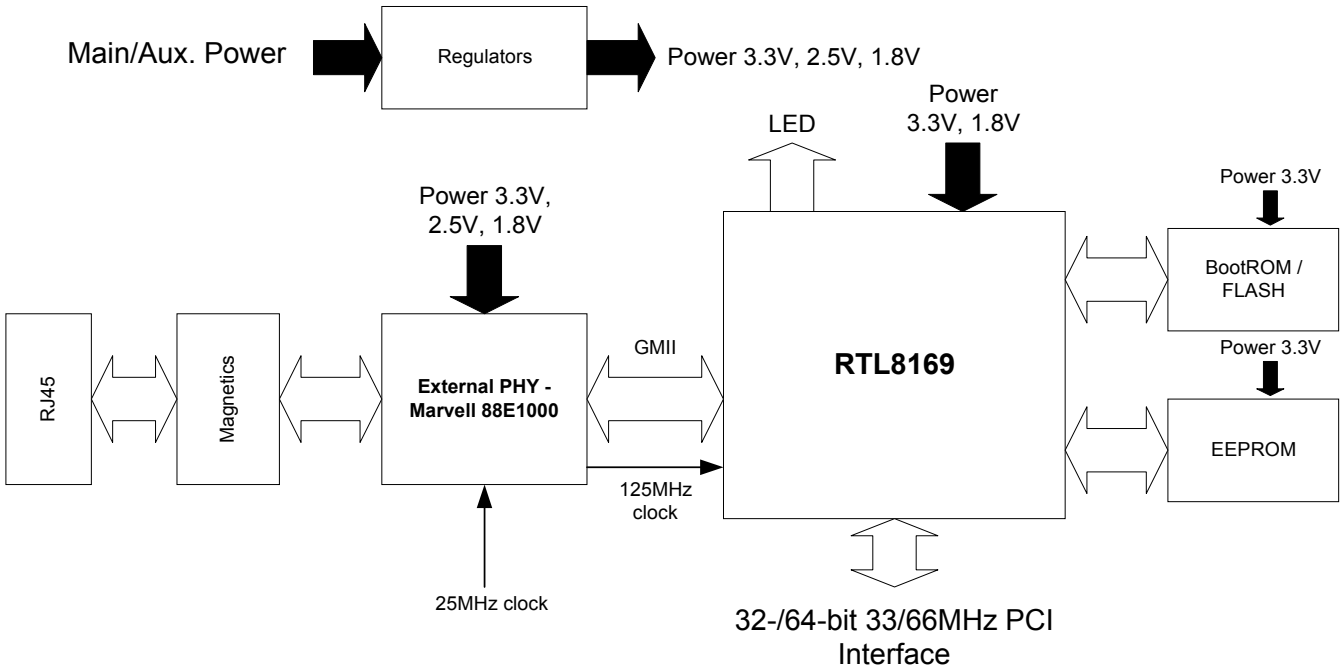
MII Management Frame Format

i. Start bits are defined as <01>.
ii. Opcode bits are defined as <01> for a Write access and <10> for a Read access.
iii. PMD address is the device address.
iv. Register address is address of the register within that device.
v. Line turnaround bits will be <10> for Write accesses and will be <xx> for Read accesses. This allows time for the MII lines to “turn around”.
vi. Data is the 16 bits of data that will be written to or read from the PMD device.

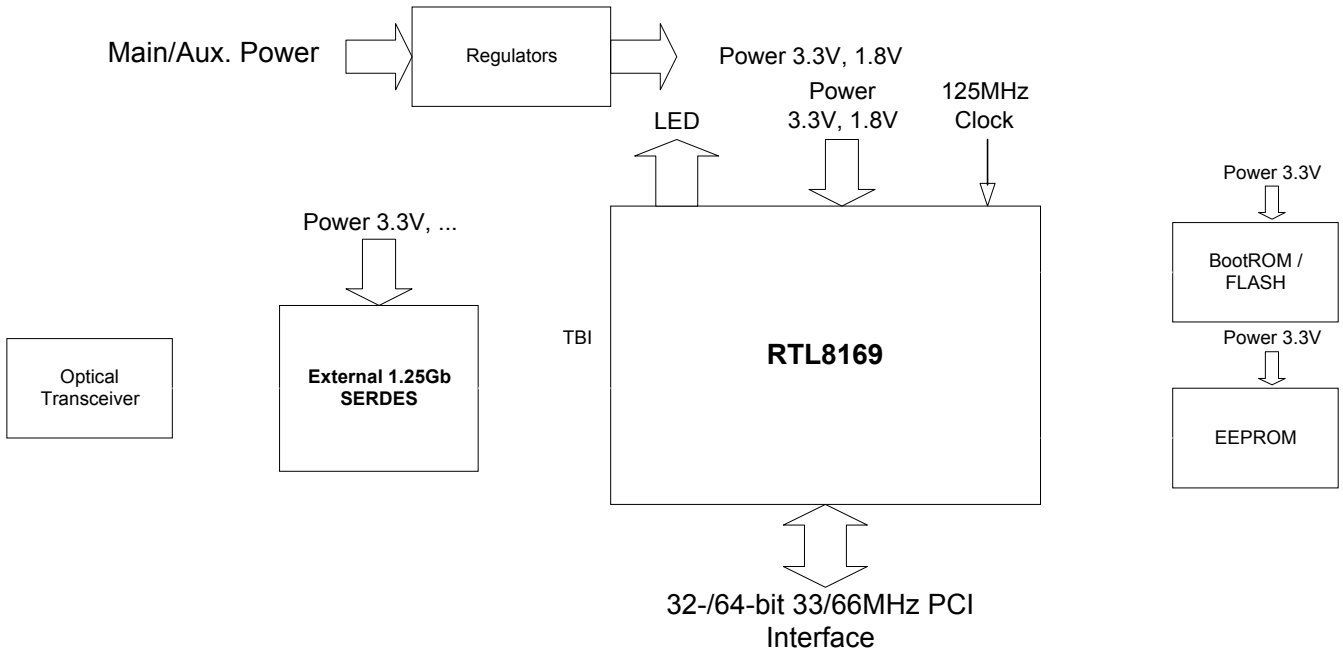
A reset frame, defined as 32 consecutive 1s (FFFF FFFFh), is also provided. After power up, all MII PMD devices must wait for a reset frame to be received prior to participating in MII management communication. Additionally, a reset frame may be issued at any time to allow all connected PMDs to re-synchronize to the data traffic.

10. Application Diagrams

10.1 10/100/1000Base-T Application



10.2 1000Base-X Application



11. Electrical Characteristics

11.1 Temperature Limit Ratings

Parameter	Minimum	Maximum	Units
Storage temperature	-55	+125	°C
Operating temperature	0	70	°C

11.2 DC Characteristics

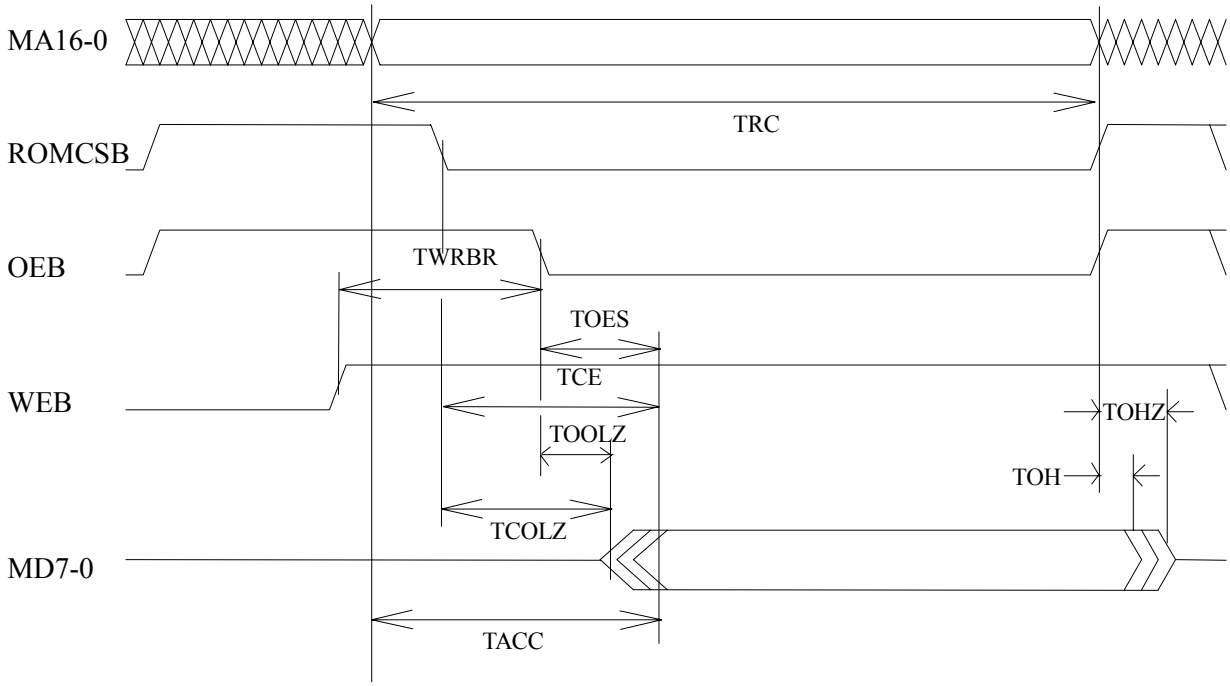
Below is a description of the general DC specifications for the RTL8169.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
VDD33	3.3V Supply Voltage		3.0	3.3	3.6	V
VDD18	1.8V Supply Voltage		1.71	1.8	1.89	V
V_{oh}	Minimum High Level Output Voltage	I_{oh} = -8mA	0.9 * Vcc		Vcc	V
V_{ol}	Maximum Low Level Output Voltage	I_{ol} = 8mA			0.1 * Vcc	V
V_{ih}	Minimum High Level Input Voltage		0.5 * Vcc		Vcc+0.5	V
V_{il}	Maximum Low Level Input Voltage		-0.5		0.3 * Vcc	V
I_{in}	Input Current	V_{in} =V_{cc} or GND	-1.0		1.0	uA
I_{oz}	Tri-State Output Leakage Current	V_{out} =V_{cc} or GND	-10		10	uA
Icc33	Average Operating Supply Current from 3.3V				100	mA
I_{cc18}	Average Operating Supply Current from 1.8V				70	mA

11.3 AC Characteristics

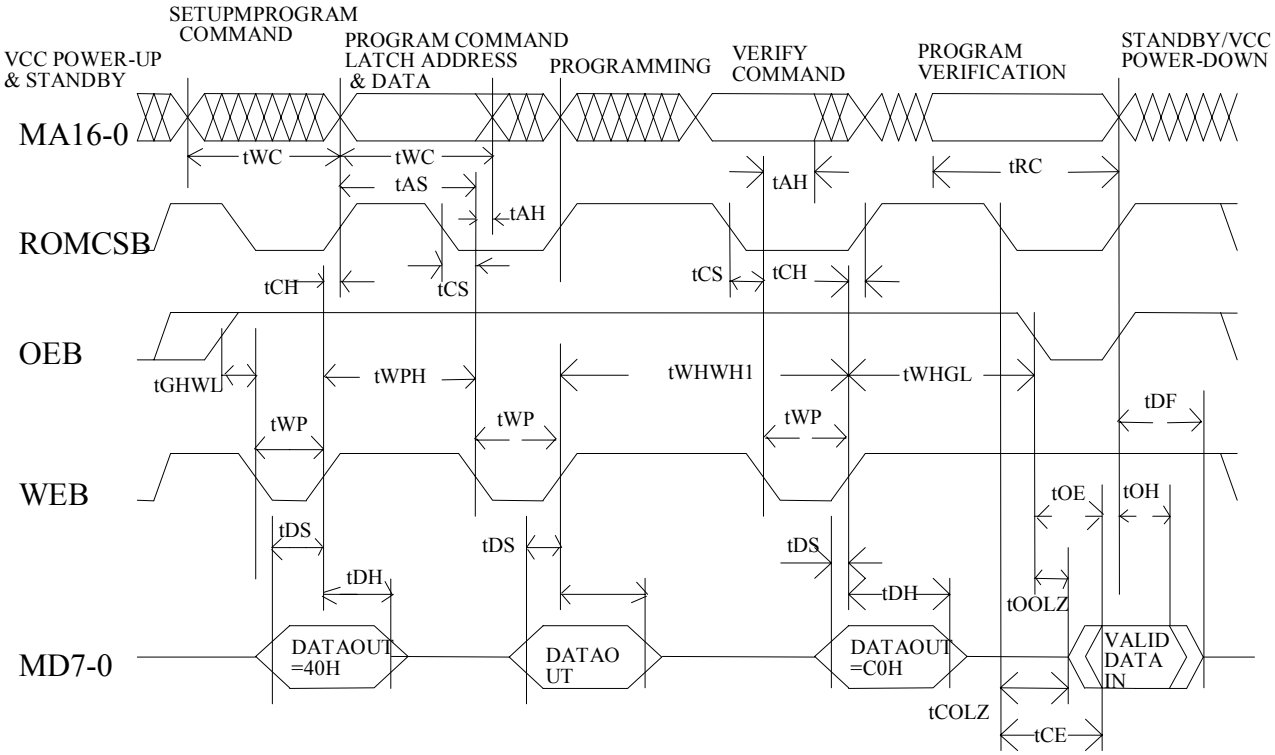
11.3.1 FLASH/BOOT ROM Timing

FLASH/BOOT ROM - Read



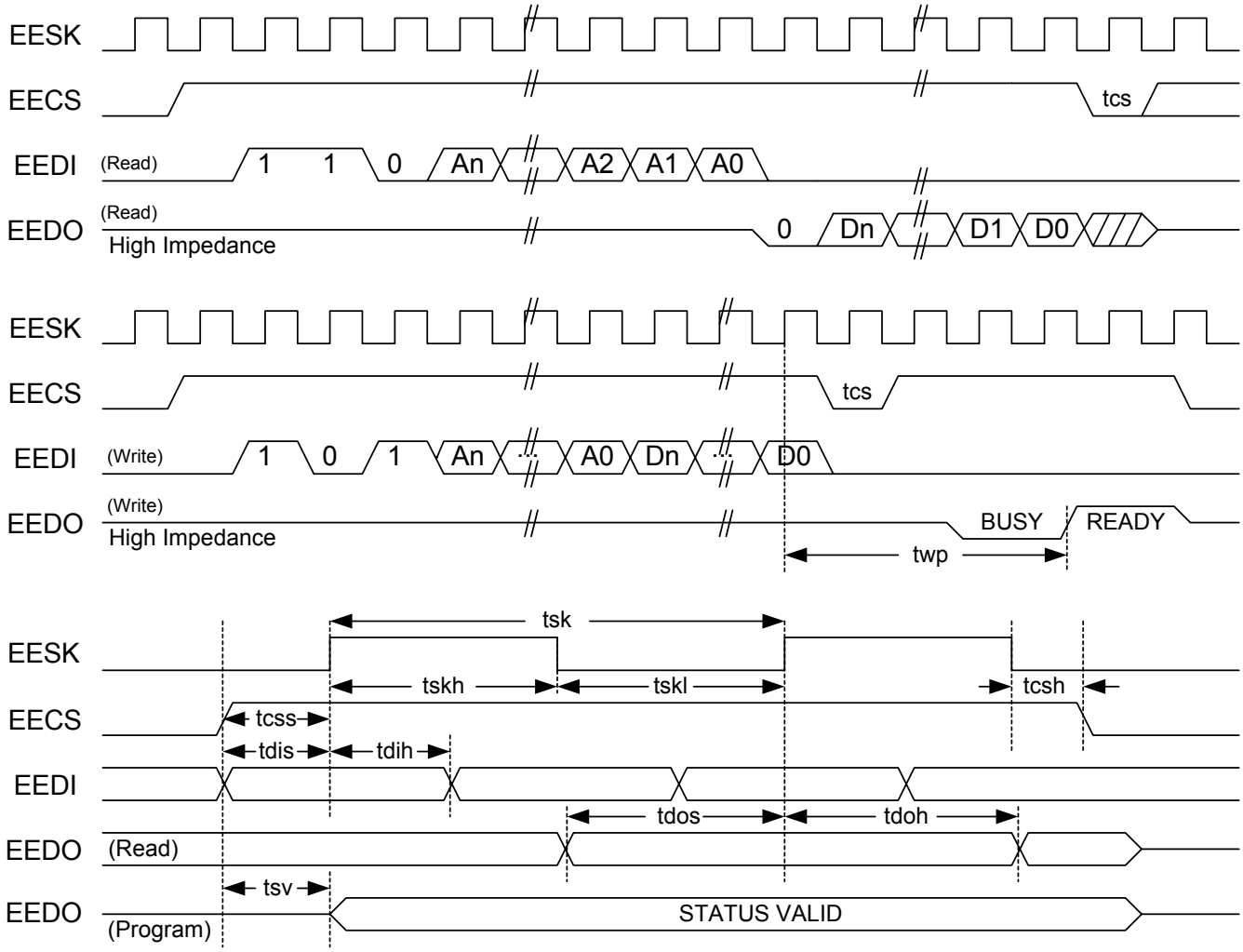
Symbol	Description	Minimum	Typical	Maximum	Units
TRC	Read Cycle	135	-	-	ns
TCE	Chip Enable Access Time	-	-	200	ns
TACC	Address Access Time	-	-	200	ns
TOES	Output Enable Access Time	-	-	60	ns
TCOLZ	Chip Enable to Output in Low Z	0	-	-	ns
TOOLZ	Output Enable to Output in Low Z	0	-	-	ns
TOHZ	Output Disable to Output in High Z	-	-	40	ns
TOH	Output Hold from Address, ROMCSB, or OEB	0	-	0	ns
TWRBR	Write Recovery time Before Read	6	-	-	us

FLASH MEMORY - Write



Symbol	Description	Minimum	Typical	Maximum	Units
TWC	Write Cycle Time	135	-	-	ns
TAS	Address Set-up Time	0	-	-	ns
TAH	Address Hold Time	60	-	-	ns
TDS	Data Set-up Time	50	-	-	ns
TDH	Data Hold Time	10	-	-	ns
TWHGL	Write Recovery Time before Read	6	-	-	us
TGHWL	Read Recovery Time before Write	0	-	-	us
TCS	Chip Enable Set-up Time before Write	20	-	-	ns
TCH	Chip Enable Hold Time	0	-	-	us
TWP	Write Pulse Width	50	-	-	ns
TWPH	Write Pulse Width High	20	-	-	ns
TWHWH1	Duration of Programming Operation	10	-	25	us

11.3.2 Serial EEPROM Interface Timing (93C46(64*16)/93C56(128*16))



Symbol	Parameter		Min.	Typical	Max.	Unit
tcs	Minimum CS Low Time	9346/9356	1000/250			ns
twp	Write Cycle Time	9346/9356			10/10	ms
tsk	SK Clock Cycle Time	9346/9356	4/1			us
tskh	SK High Time	9346/9356	1000/500			ns
tskl	SK Low Time	9346/9356	1000/250			ns
tcss	CS Setup Time	9346/9356	200/50			ns
tcsh	CS Hold Time	9346/9356	0/0			ns
tdis	DI Setup Time	9346/9356	400/50			ns
tdih	DI Hold Time	9346/9356	400/100			ns
tdos	DO Setup Time	9346/9356	2000/500			ns
tdoh	DO Hold Time	9346/9356			2000/500	ns
tsv	CS to Status Valid	9346/9356			1000/500	ns

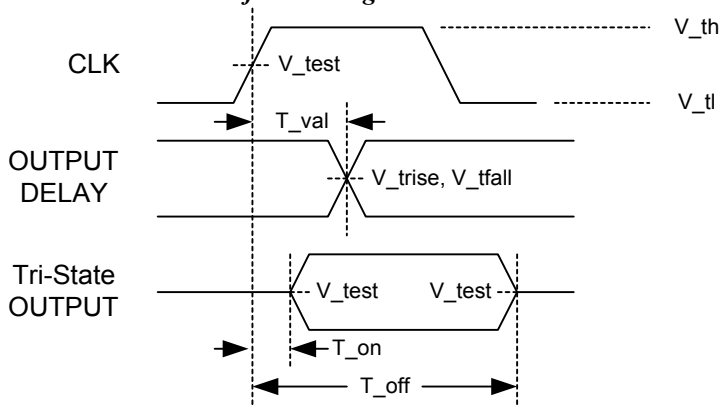
EEPROM Access Timing Parameters

11.3.3 PCI Bus Operation Timing

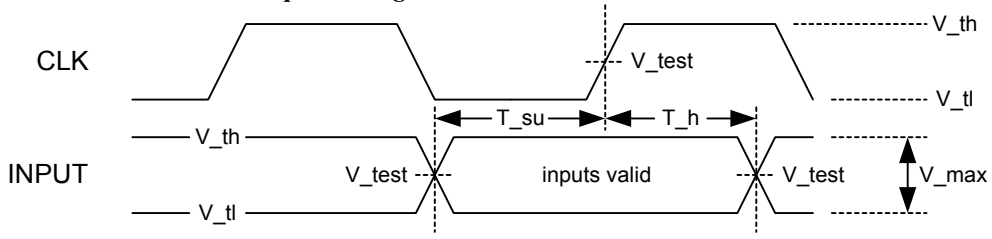
PCI Bus Timing Parameters

		66MHz		33MHz		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
T val	CLK to Signal Valid Delay-bused signals	2	6	2	11	ns
T val(ptp)	CLK to Signal Valid Delay-point to point	2	6	2	12	ns
T on	Float to Active Delay	2		2		ns
T off	Active to Float Delay		14		28	ns
T su	Input Setup Time to CLK-bused signals	3		7		ns
T su(ptp)	Input Setup Time to CLK-point to point	5		10		ns
T h	Input Hold Time from CLK	0		0		ns
T rst	Reset active time after power stable	1		1		ms
T rst-clk	Reset active time after CLK STABLE	100		100		us
T rst-off	Reset Active to Output Float delay		40		40	ns
Trrsu	REQB to REQ64B Setup Time	10*Tcyc		10*Tcyc		ns
Trrh	RSTB to REQ64B Hold Time	0	50	0	50	ns
T rhfa	RSTB High to First configuration Access	2^25		2^25		clocks
T rhff	RSTB High to First FRAMEB assertion	5		5		clocks

PCI Interface Timing Parameters



Output Timing Measurement Condition

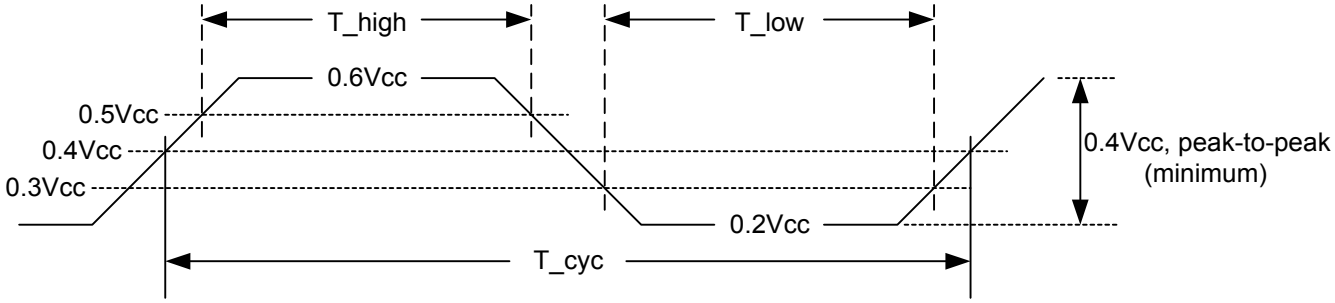


Input Timing Measurement Conditions

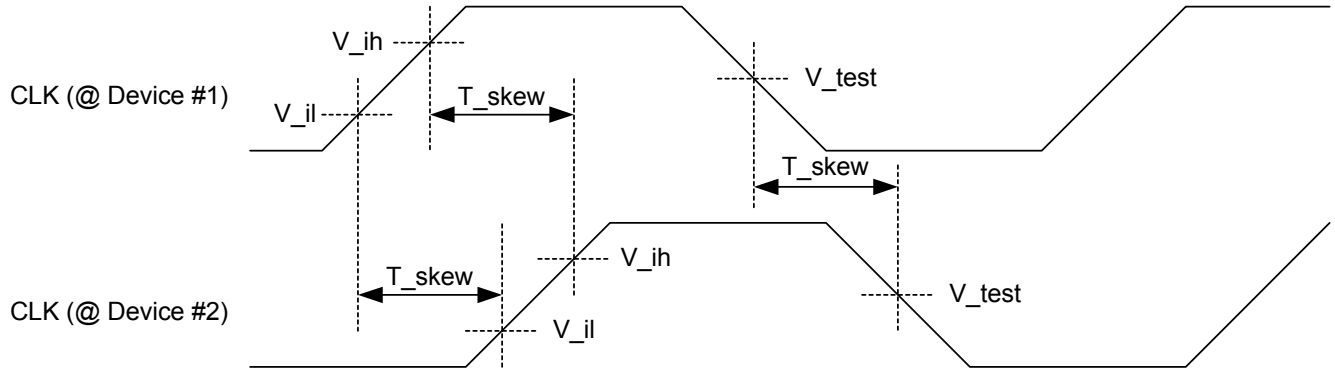
Symbol	Level	Units
Vth	0.6Vcc	V
Vtf	0.2Vcc	V
Vtest	0.4Vcc	V
Vtrise	0.285Vcc	V
Vtfall	0.615Vcc	V
Vmax	0.4Vcc	V
Input Signal Edge Rate	1	V/ns

Measurement Condition Parameters

PCI Clock Specification



3.3V Clock Waveform

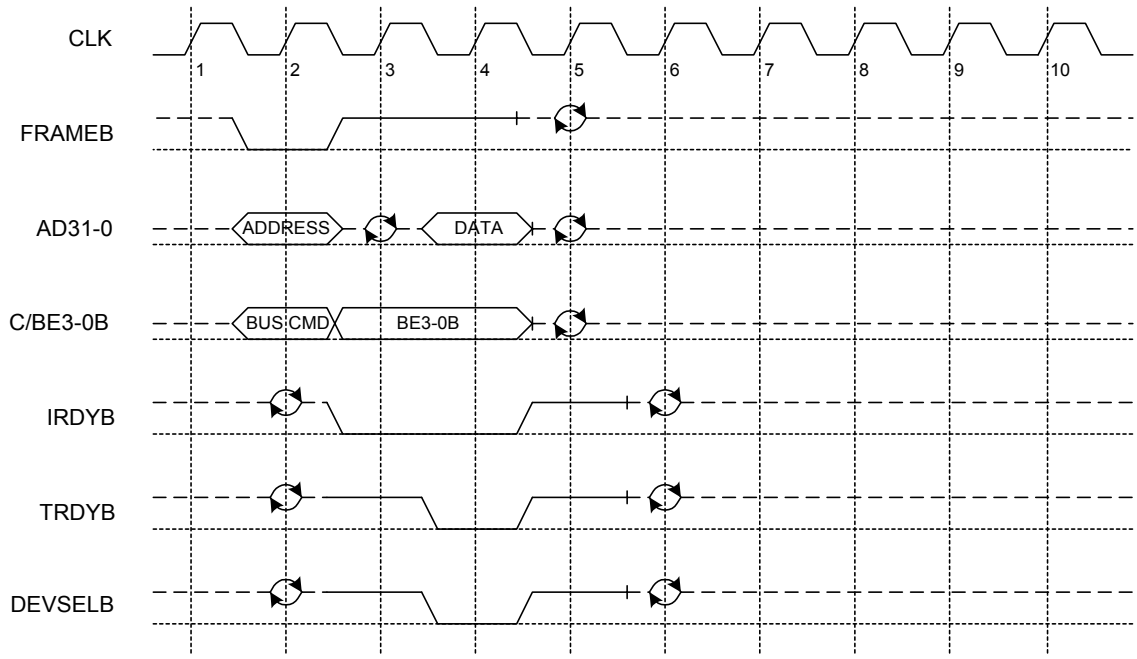


Clock Skew Diagram

		66MHz		33MHz		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
Tcyc	**CLK** Cycle Time	15	30	30	∞	ns
Thigh	**CLK** High Time	6		11		ns
Tlow	**CLK** Low Time	6		11		ns
--	**CLK** Slew Rate	1.5	4	1	4	V/ns
--	**RST#** Slew Rate	50	-	50	-	mV/ns
Tskew	**CLK** Skew		1		2	ns

Clock and Reset Specifications

PCI Transactions



I/O Read

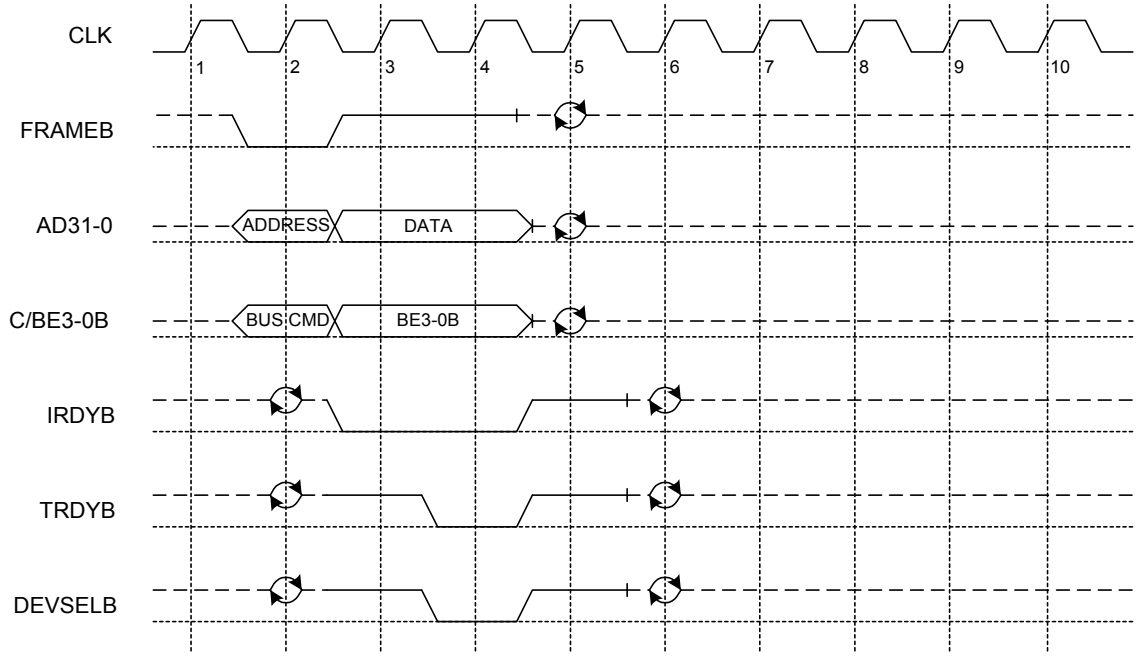
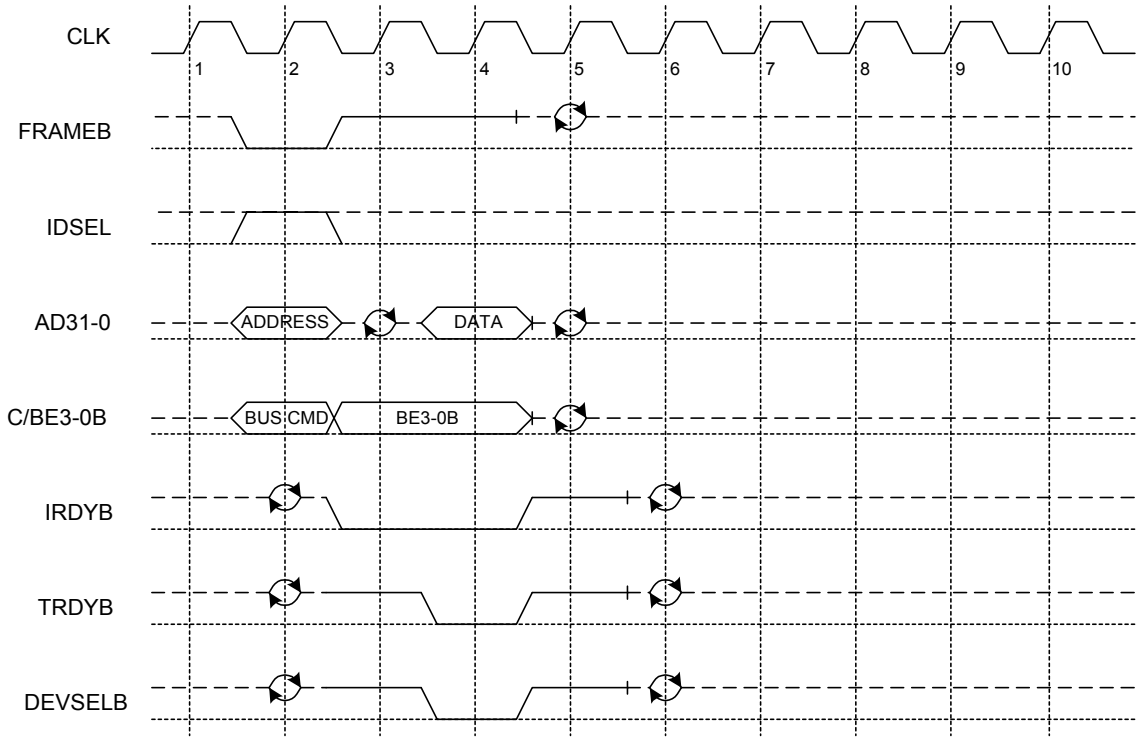
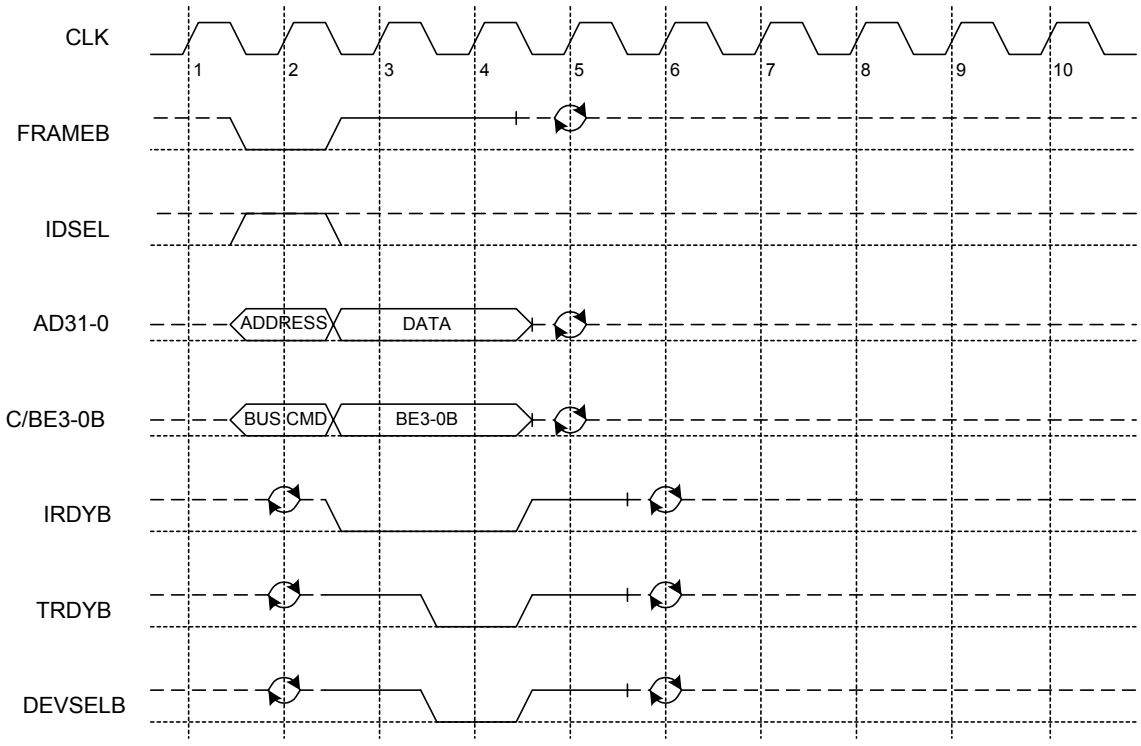


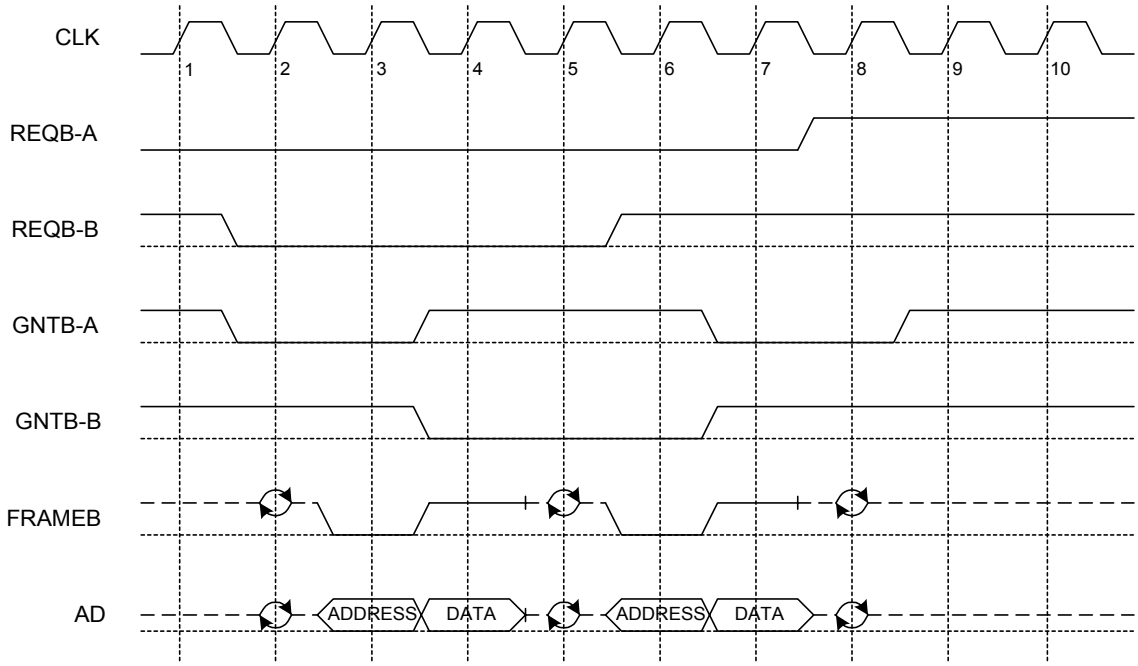
Fig. 11.3.3.3.2 I/O Write



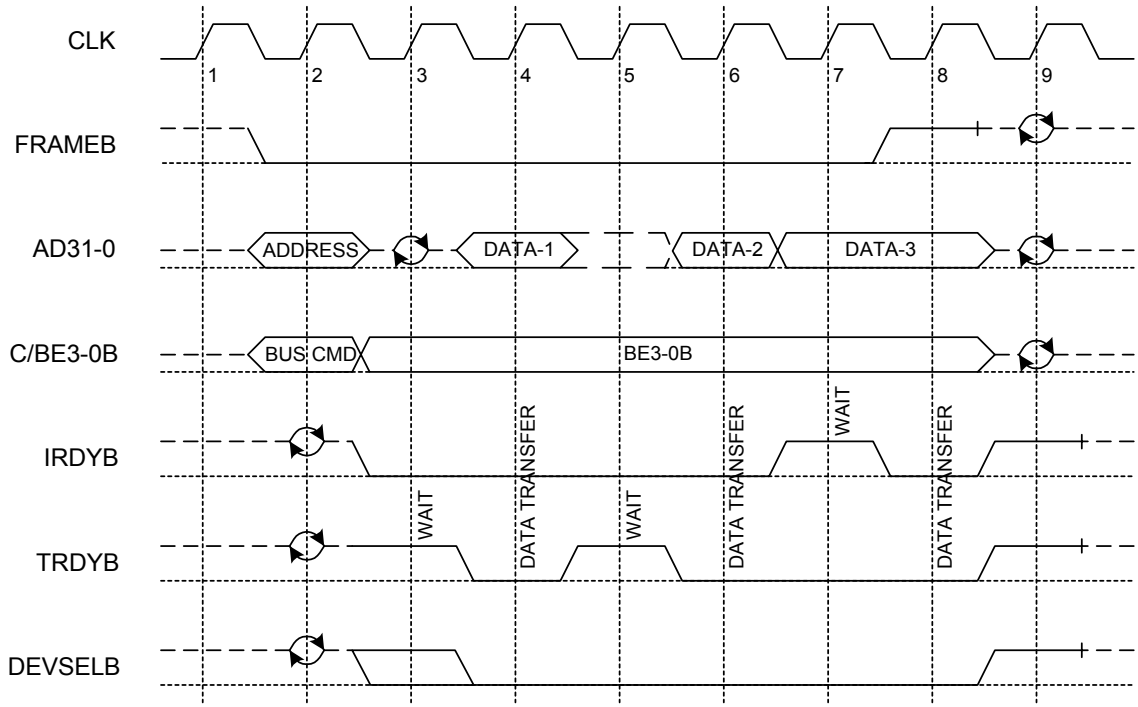
Configuration Read



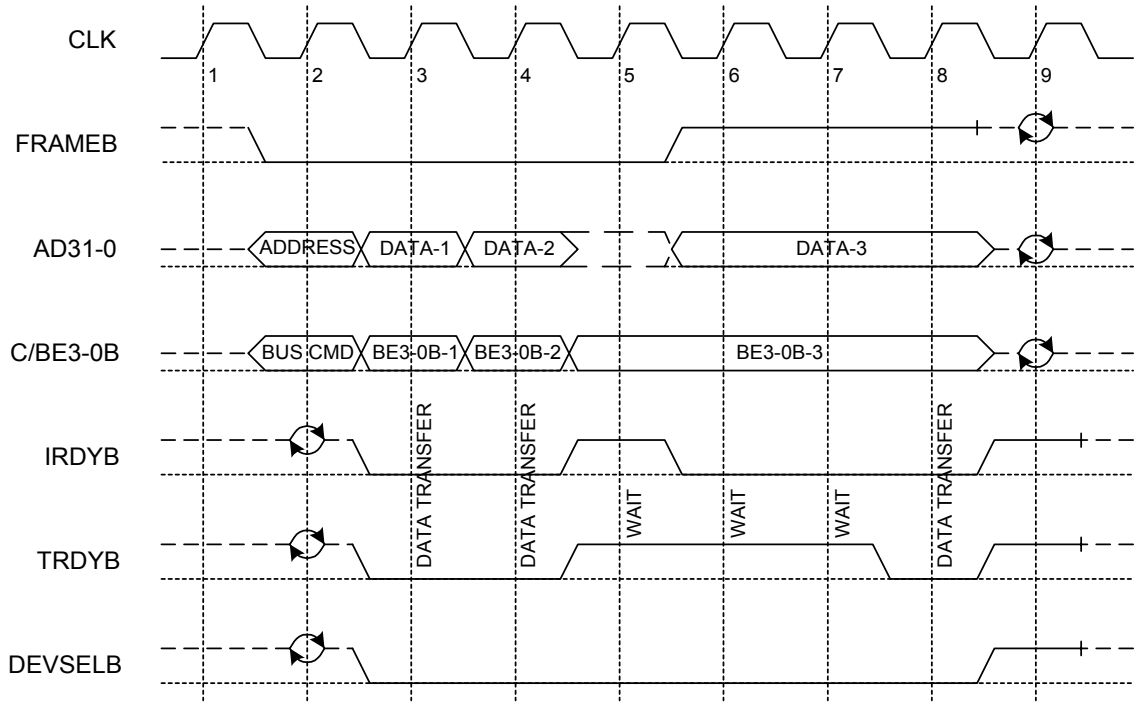
Configuration Write



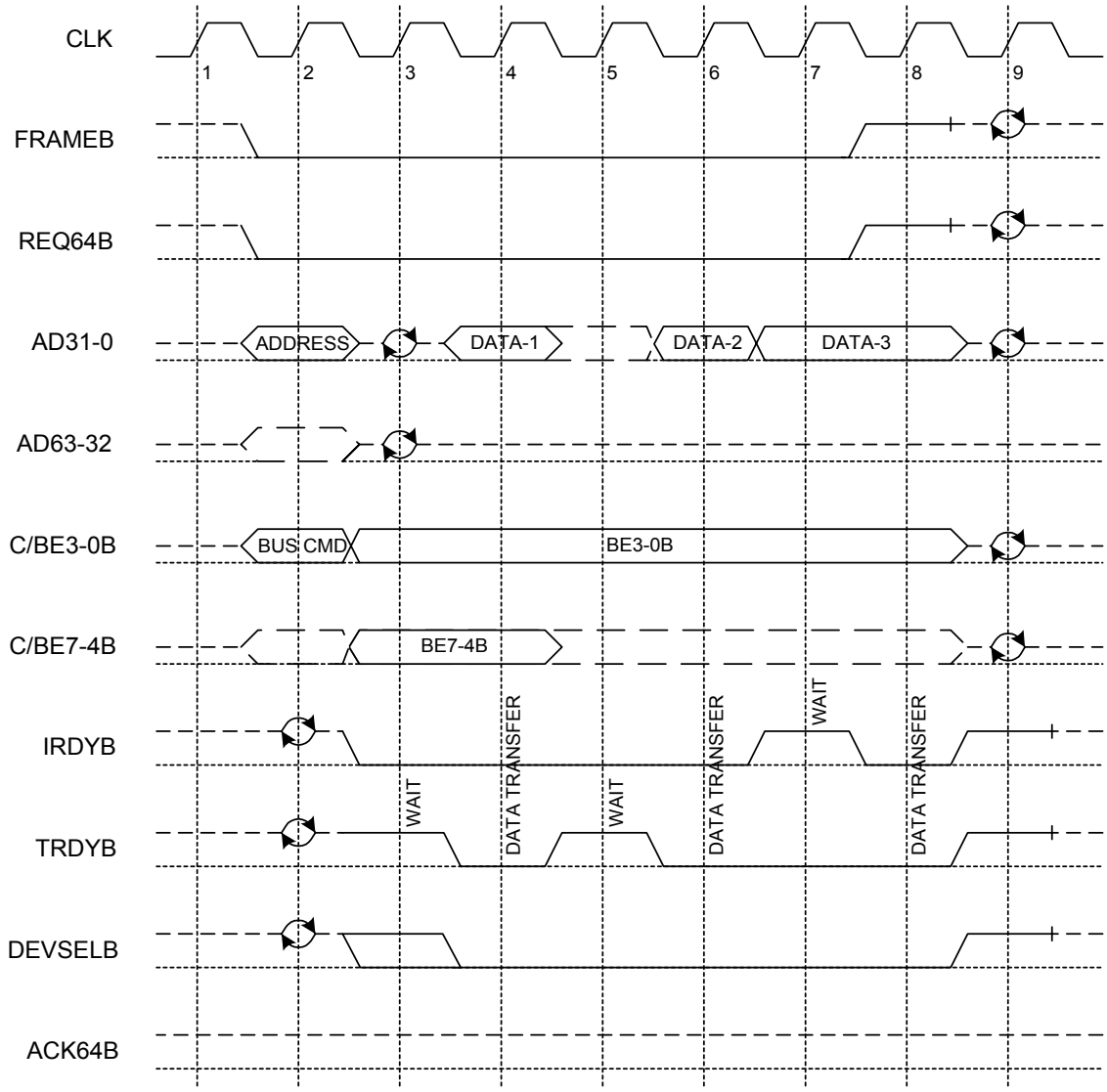
BUS Arbitration



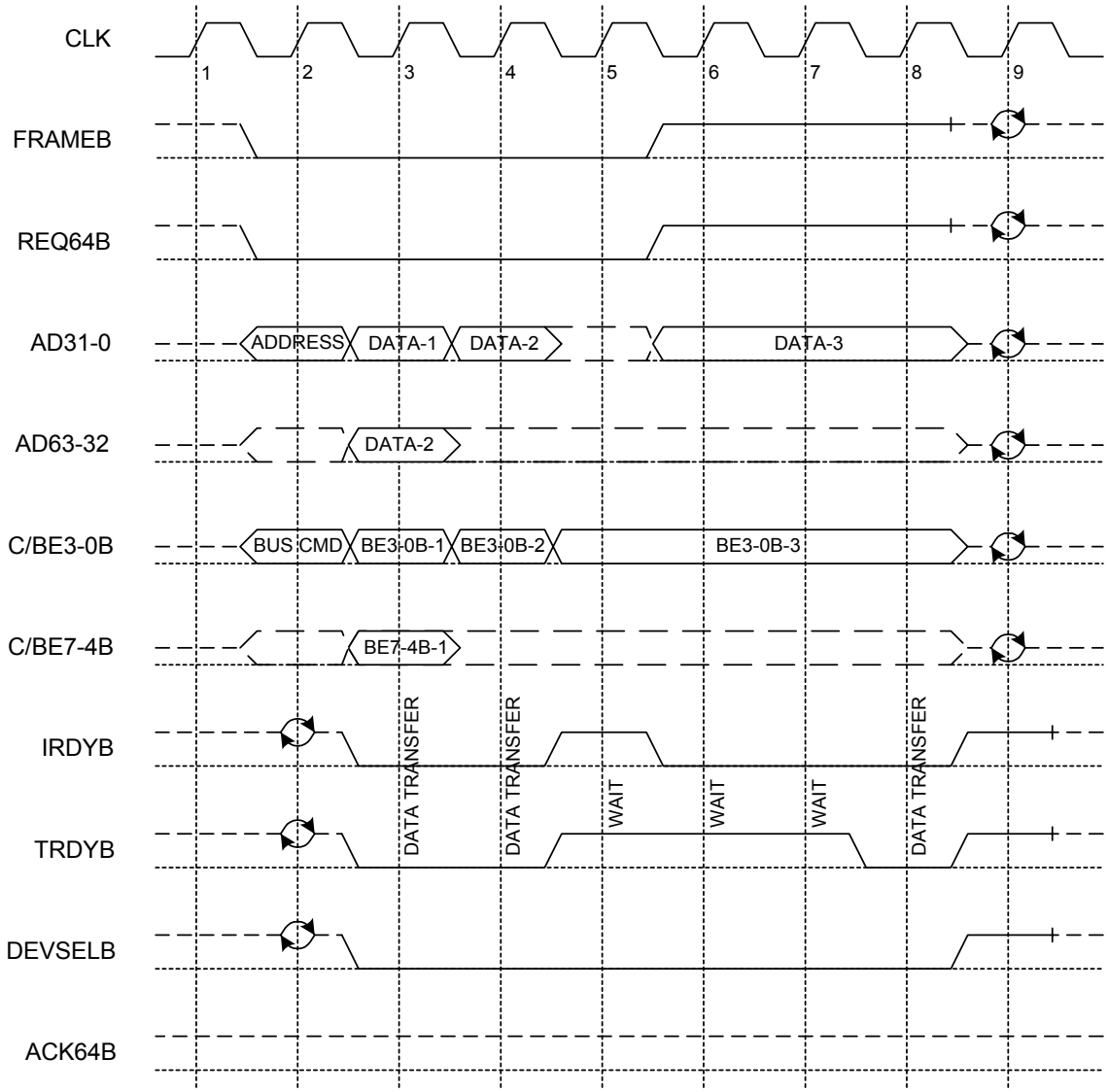
Memory Read below 4GB (32-bit address, 32-bit data; 32-bit slot)



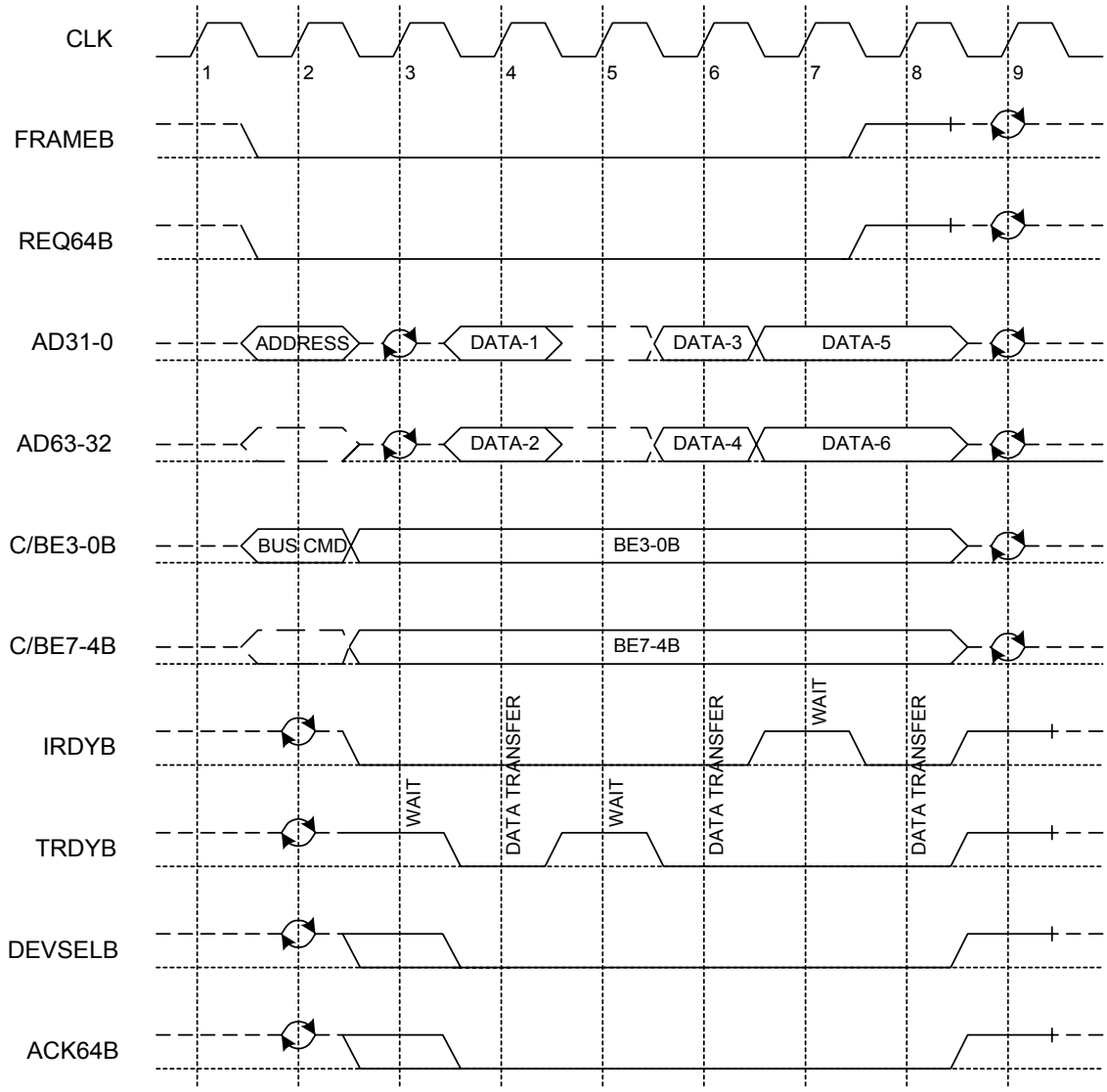
Memory Write below 4GB (32-bit address, 32-bit data; 32-bit slot)



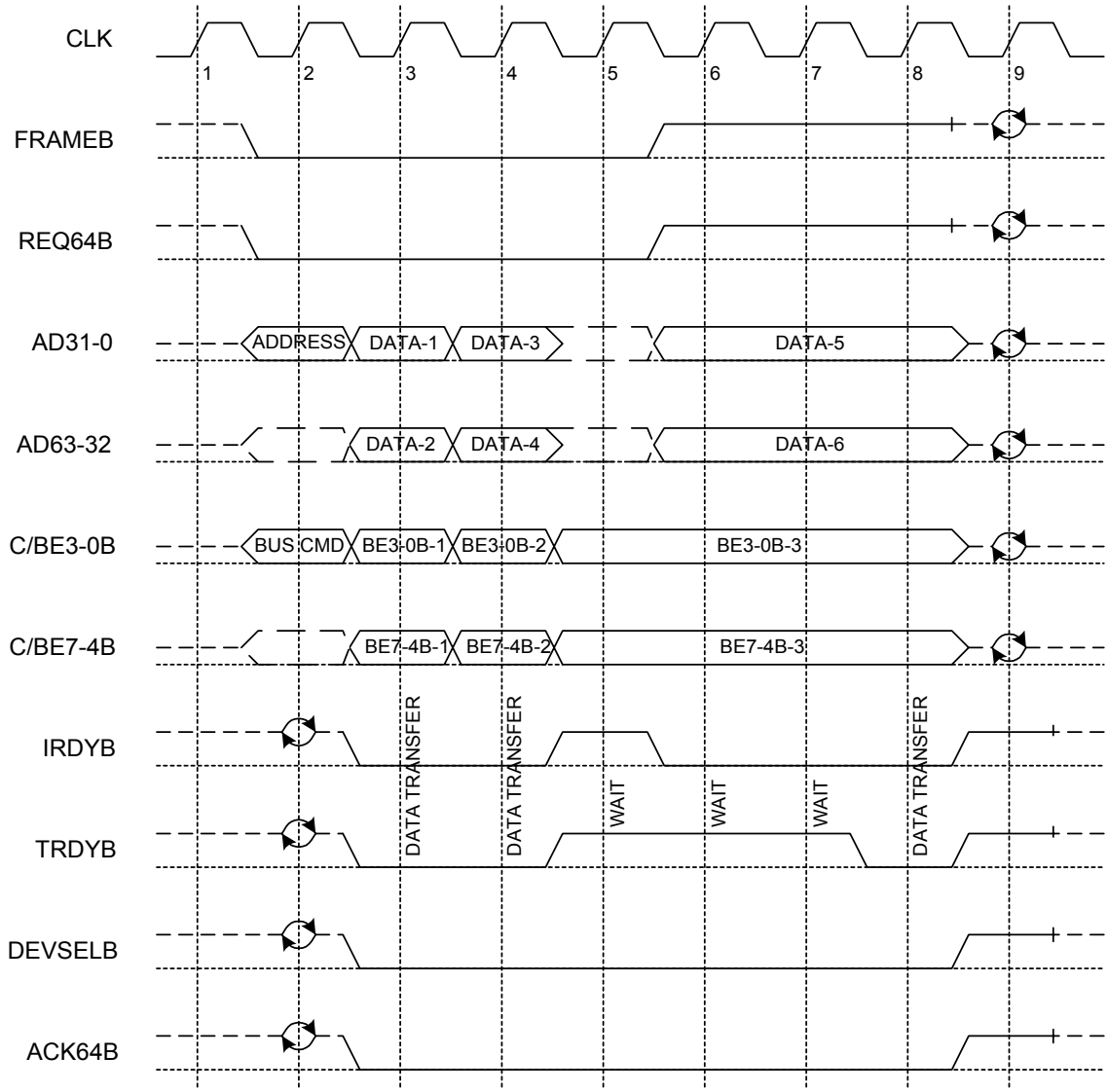
Memory Read below 4GB (32-bit address, 32-bit data transfer granted; 64-bit slot)



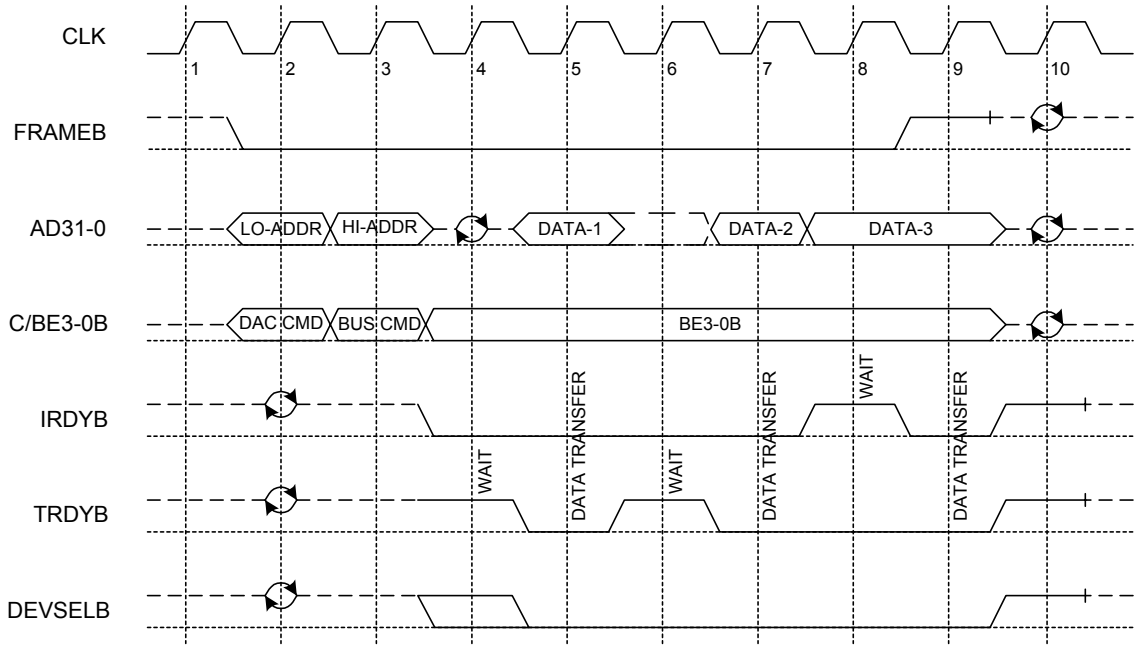
Memory Write below 4GB (32-bit address, 32-bit data transfer granted; 64-bit slot)



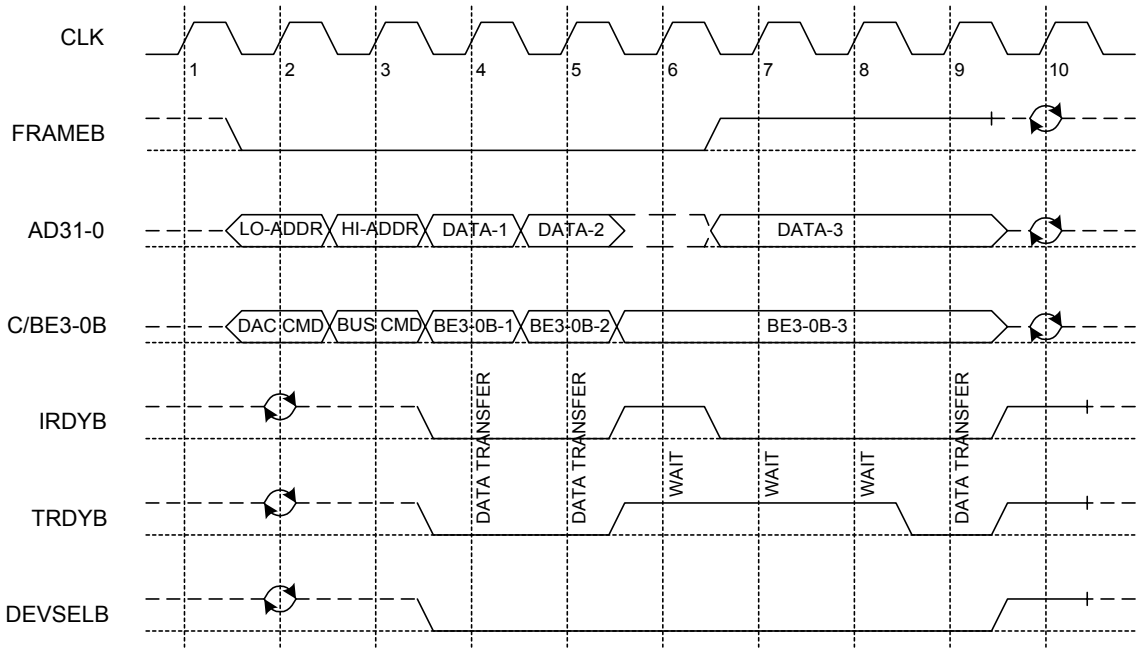
Memory Read below 4GB (32-bit address, 64-bit data transfer granted; 64-bit slot)



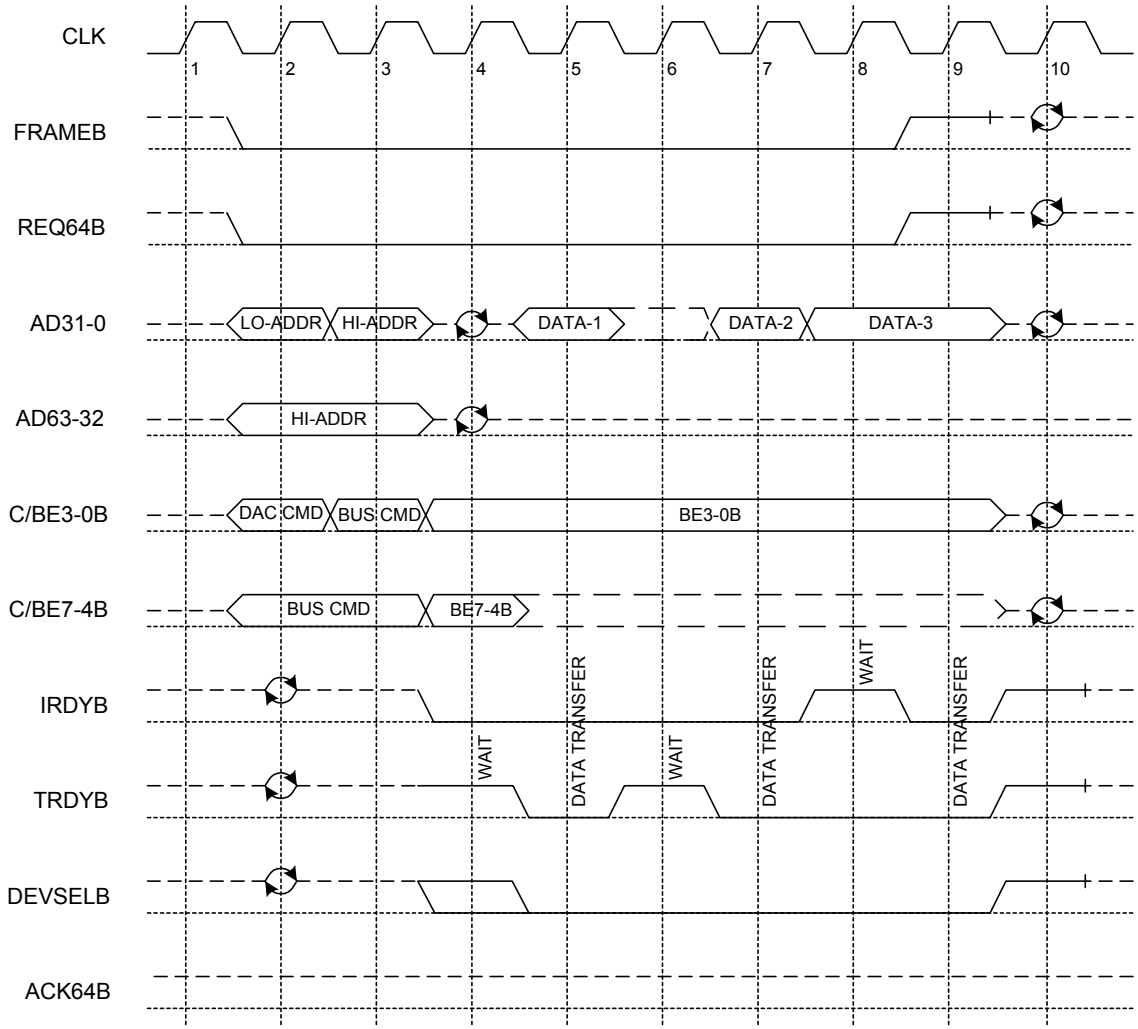
Memory Write below 4GB (32-bit address, 64-bit data transfer granted; 64-bit slot)



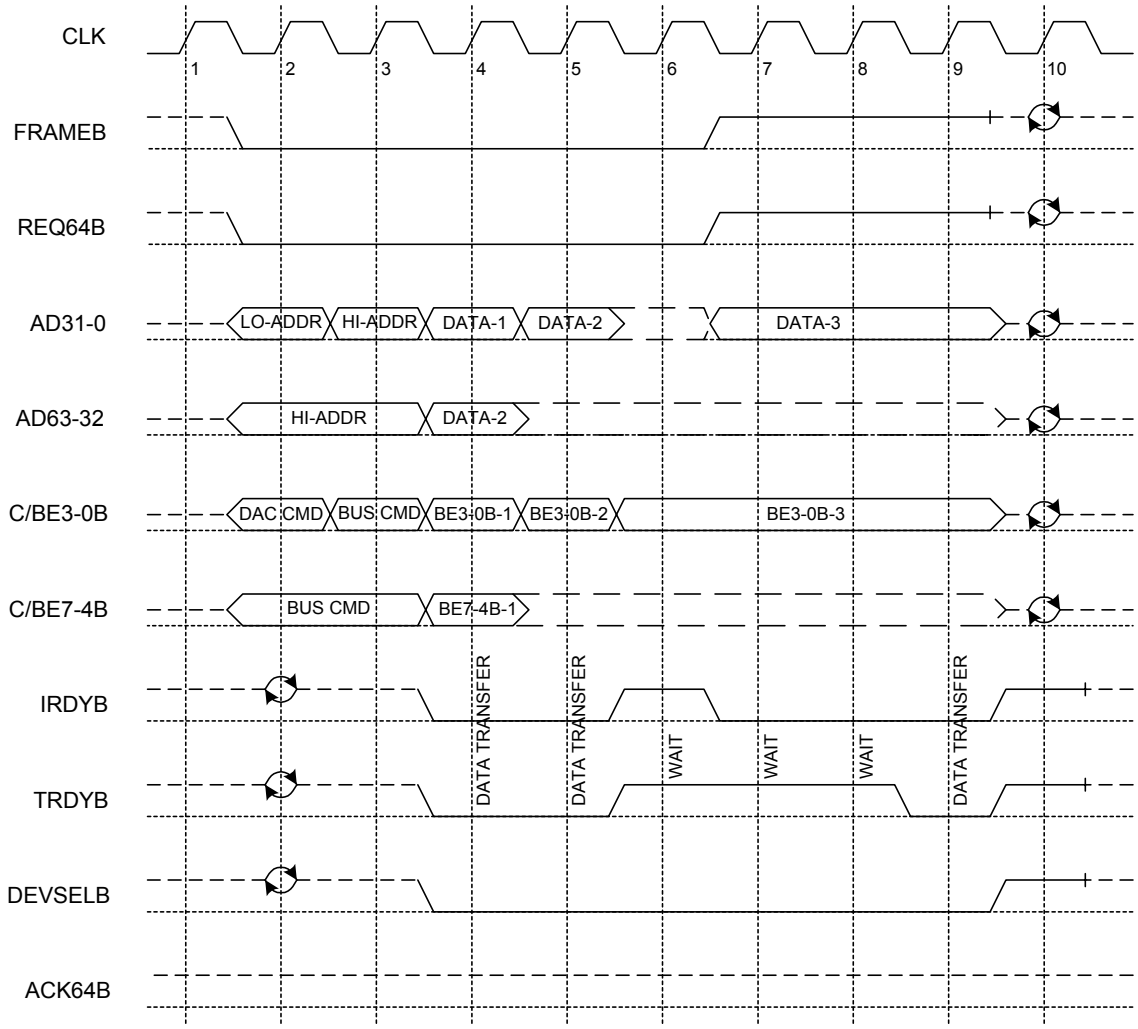
Memory Read above 4GB (DAC, 64-bit address, 32-bit data; 32-bit slot)



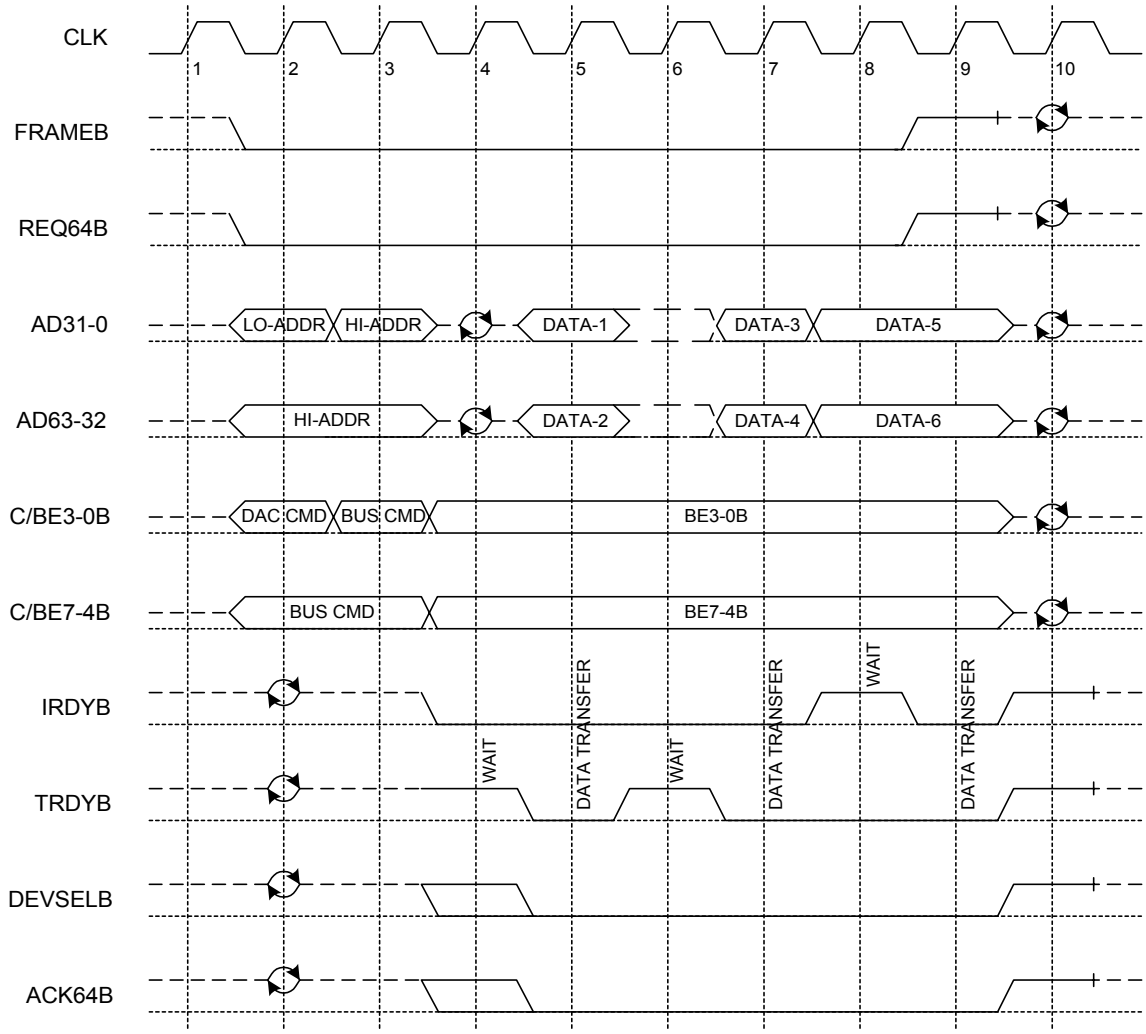
Memory Write above 4GB (DAC, 64-bit address, 32-bit data; 32-bit slot)



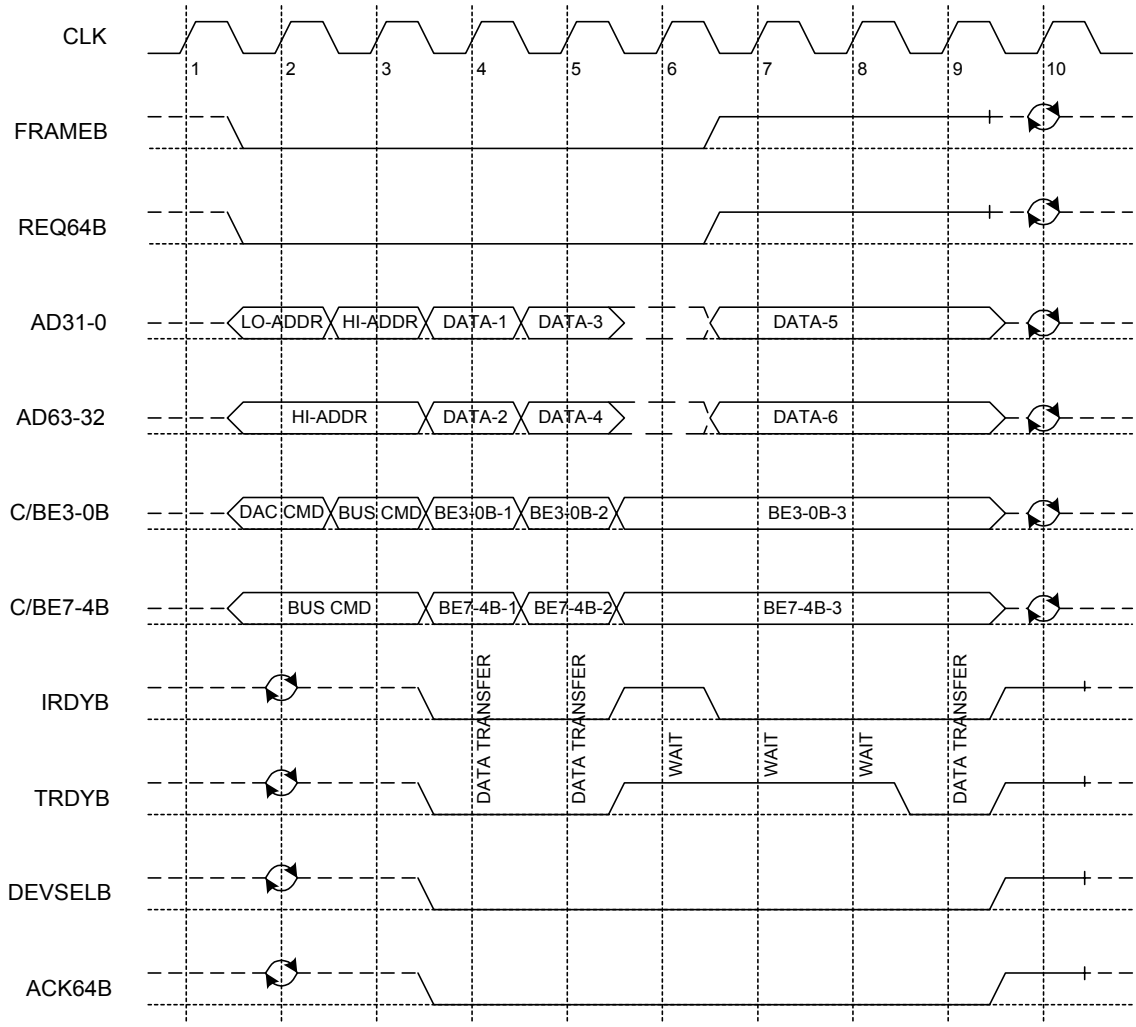
Memory Read above 4GB (DAC, 64-bit address, 32-bit data transfer granted; 64-bit slot)



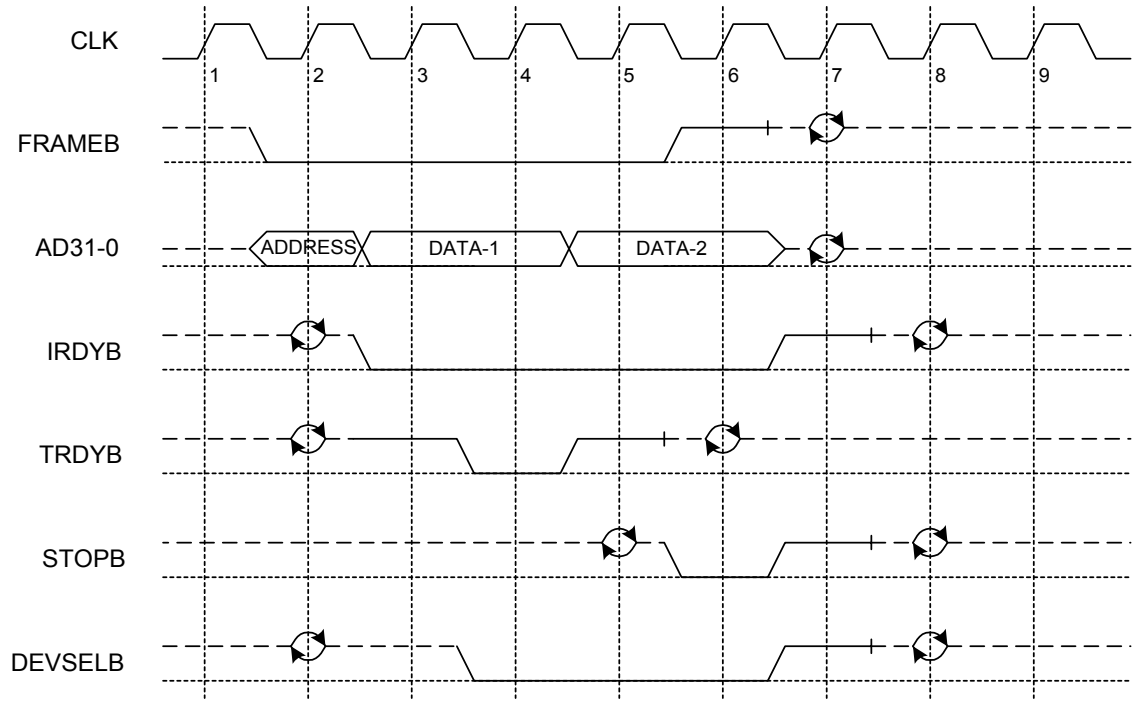
Memory Write above 4GB (DAC, 64-bit address, 32-bit data transfer granted; 64-bit slot)



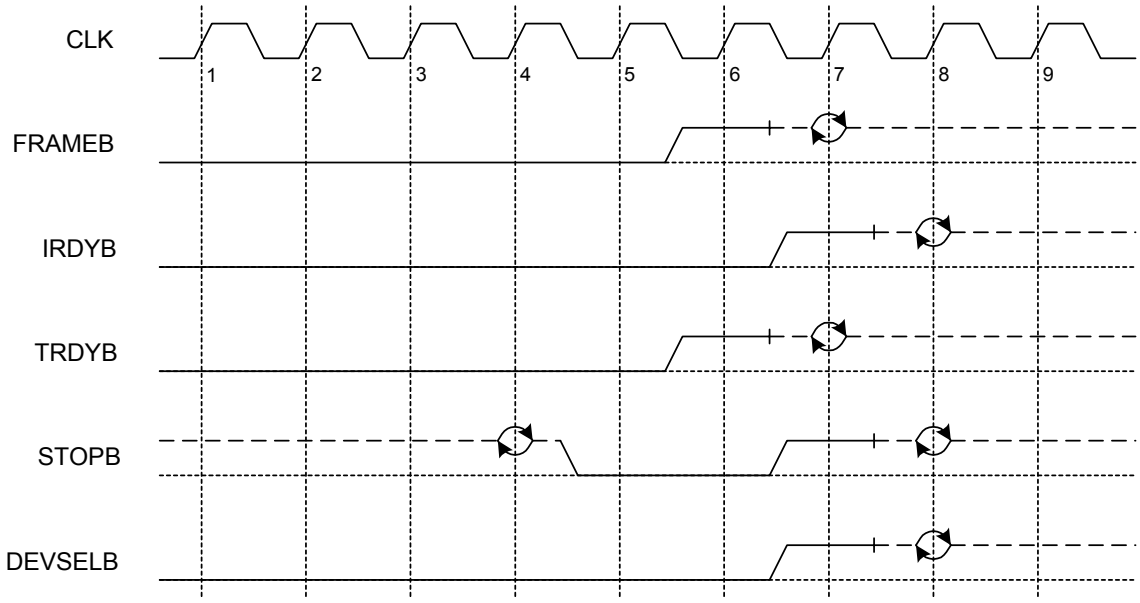
Memory Read above 4GB (DAC, 64-bit address, 64-bit data transfer granted; 64-bit slot)



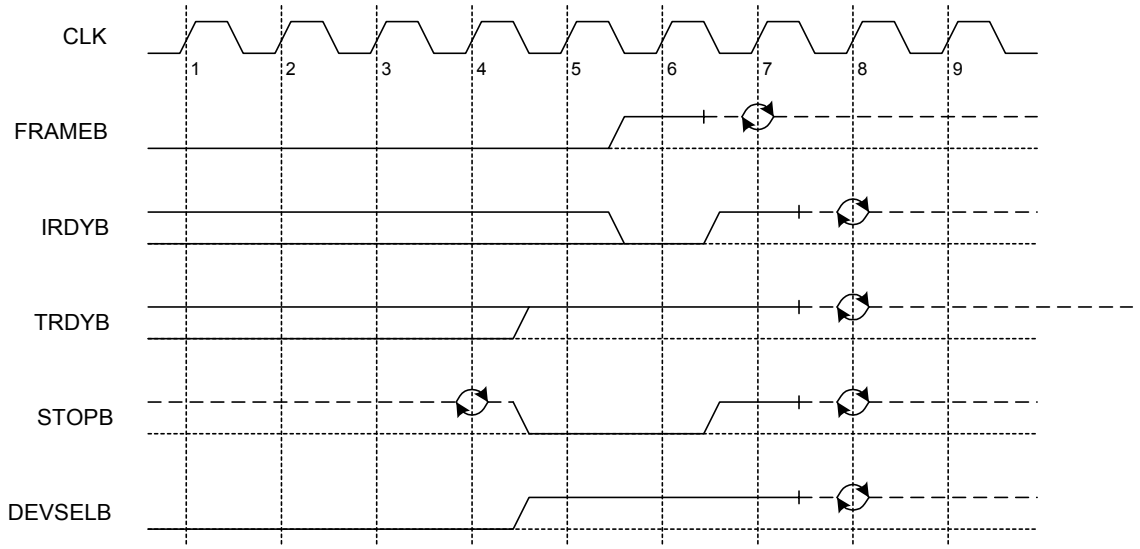
Memory Write above 4GB (DAC, 64-bit address, 64-bit data transfer granted; 64-bit slot)



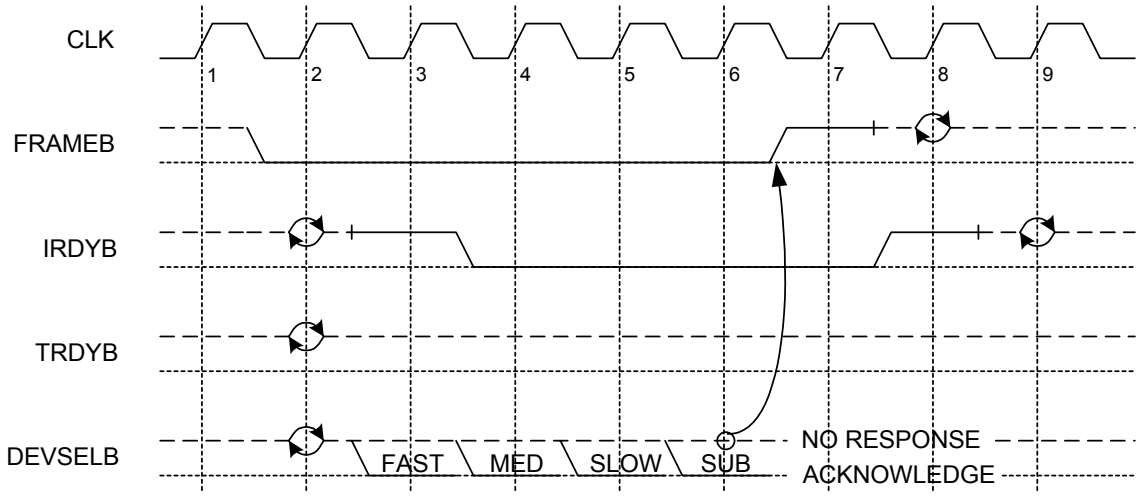
Target Initiated Termination - Retry



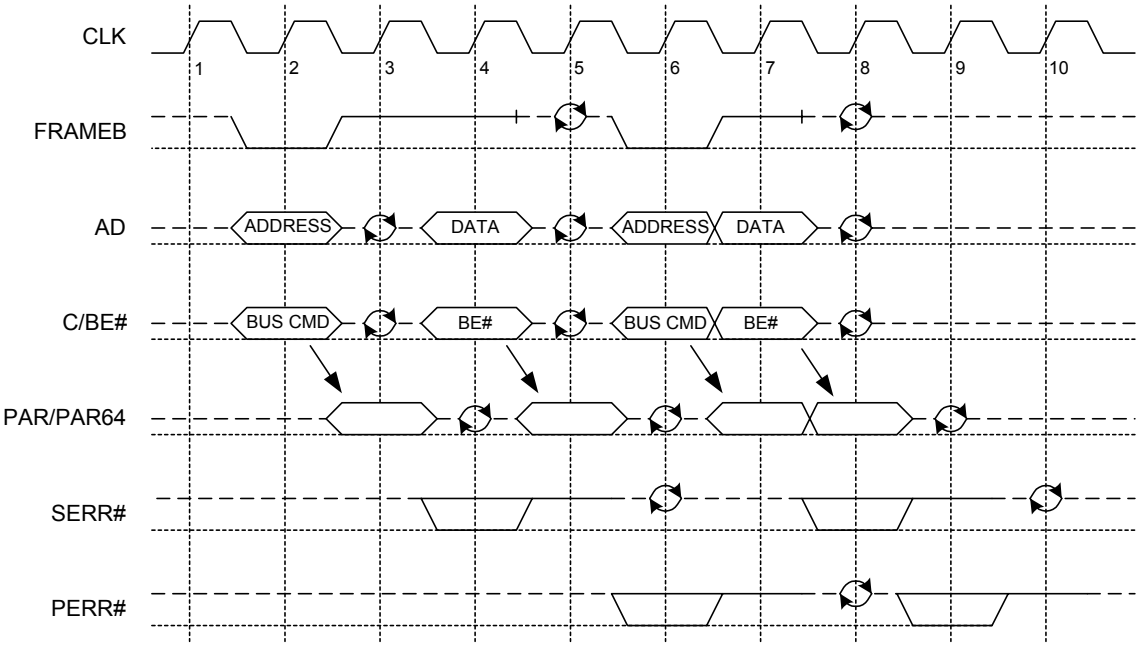
Target Initiated Termination - Disconnect



Target Initiated Termination - Abort



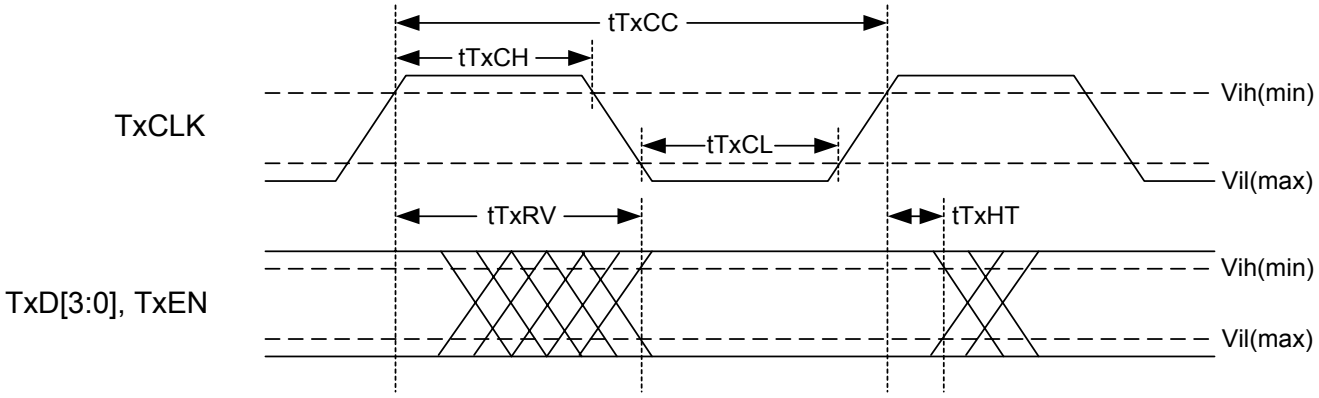
Master Initiated Termination - Abort



Parity Operation - One Example

11.3.4 MII Timing

MII Timing – MII PORT - Transmit

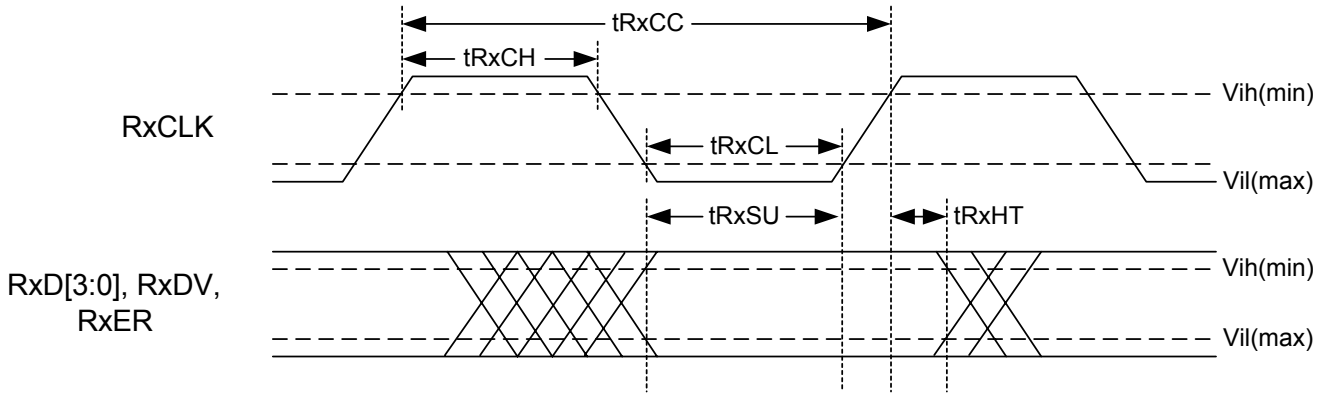


MII Transmit Timing

Symbol	Description	10MHz Min	10MHz Typical	10MHz Max	100MHz Min	100MHz Typical	100MHz Max	Units
tTxCC	Tx Clock Cycle		400			40		ns
tTxCH	Tx Clock High Time	140		260	14		26	ns
tTxCL	Tx Clock Low Time	140		260	14		26	ns
tTxRV	Tx Clock rise to TxD, TxEN valid			20			20	ns
tTxHD	TxD, TxEN Hold Time	5			5			ns

MII Transmit Timing Parameters

MII Timing – MII PORT - Receive

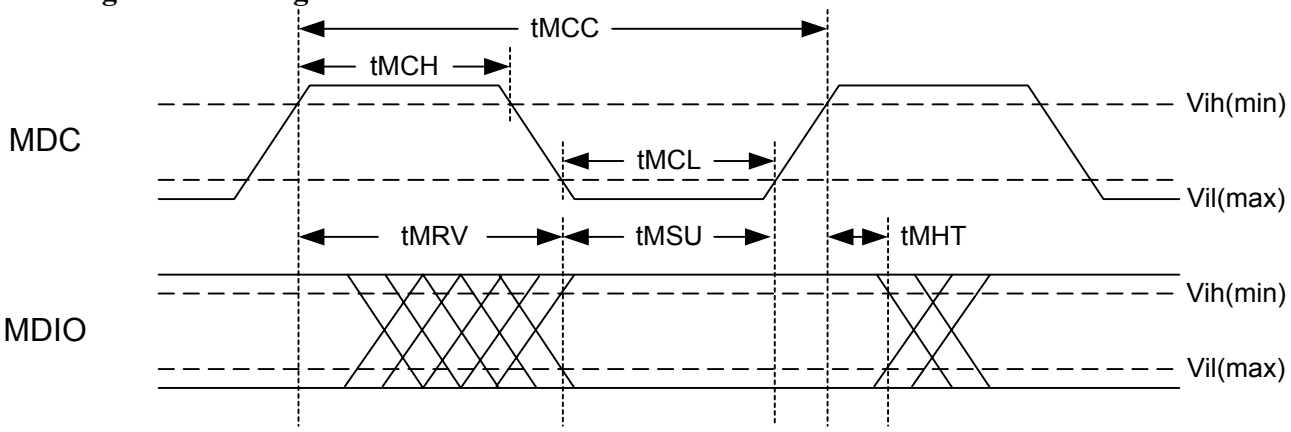


MII Transmit Timing

Symbol	Description	10MHz Min	10MHz Typical	10MHz Max	100MHz Min	100MHz Typical	100MHz Max	Units
tRxCC	Rx Clock Cycle		400			40		ns
tRxCH	Rx Clock High Time	140		260	14		26	ns
tRxCL	Rx Clock Low Time	140		260	14		26	ns
tRxSU	RxD, RxDV, RxER Setup Time	10		20	10		20	ns
tRxHD	RxD, RxDV, RxER Hold Time	5			5			ns

MII Transmit Timing Parameters

MII Timing – MII Management Port

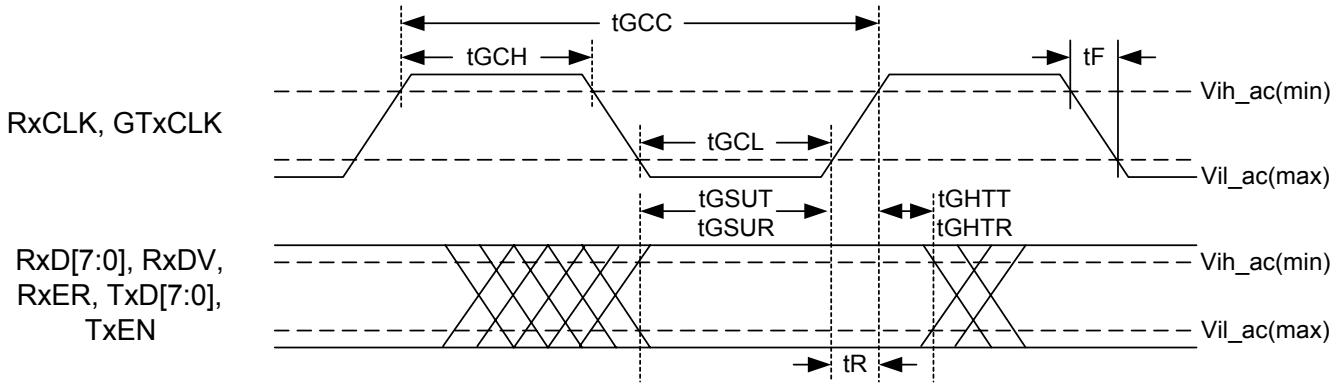


MII Management Timing

Symbol	Description	Min	Typical	Max	Units
tMCC	MDC Cycle Time	50			ns
tMCH	MDC High Time	25			ns
tMCL	MDC Low Time	25			ns
tMSU	MDIO Setup Time	10			ns
tMHT	MDIO Hold Time	5			ns
tMRV	MDC Clock rise to MDIO valid			40	ns

MII Management Timing Parameters

11.3.5 GMII Timing

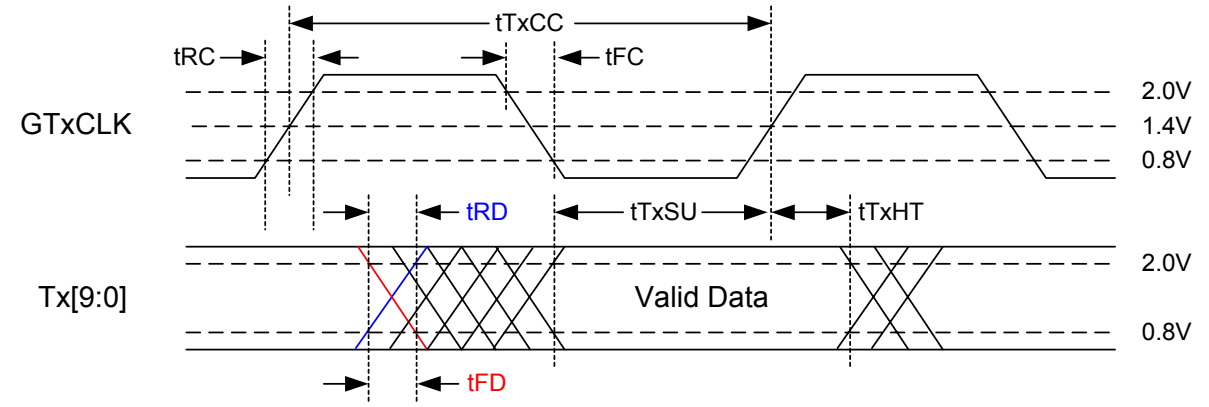


GMII Timing

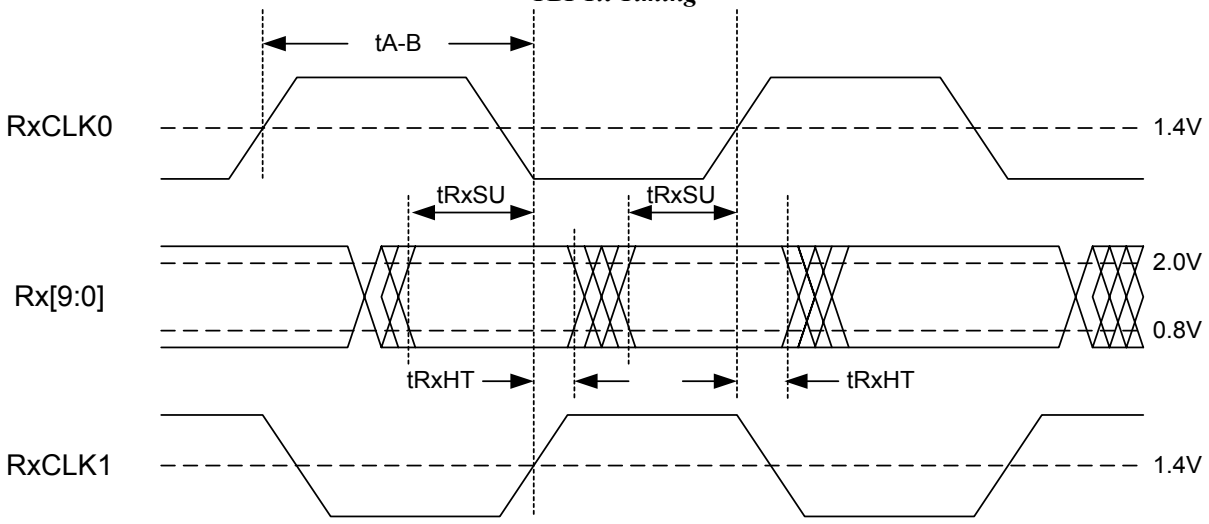
Symbol	Description	Min	Typical	Max	Units
Vil_ac	Input Low Voltage ac			0.7	V
Vih_ac	Input High Voltage ac	1.9			V
fGTxCLK, fRxCLK	GTxCLK, RxCLK frequency	125 - 100ppm	125	125 + 100ppm	MHz
tGCC	GTxCLK, RxCLK Cycle Time	7.5	8	8.5	ns
tGCH	GTxCLK, RxCLK High Time	2.5			ns
tGCL	GTxCLK, RxCLK Low Time	2.5			ns
tR	GTxCLK, RxCLK Rise Time			1	ns
tF	GTxCLK, RxCLK Fall Time			1	ns
RSR	GTxCLK, RxCLK Rising Slew Rate	0.6			V/ns
FSR	GTxCLK, RxCLK Falling Slew Rate	0.6			V/ns
tGSUT	TxD, TxEN Setup to ↑ of GTxCLK	2.5			ns
tGHTT	TxD, TxEN Hold from ↑ of GTxCLK	0.5			ns
tGSUR	RxD, RxDV, RxER Setup to ↑ of RxCLK	2			ns
tGHTR	RxD, RxDV, RxER Hold from ↑ of RxCLK	0			ns

GMII Timing Parameters

11.3.6 TBI Timing



TBI Tx Timing

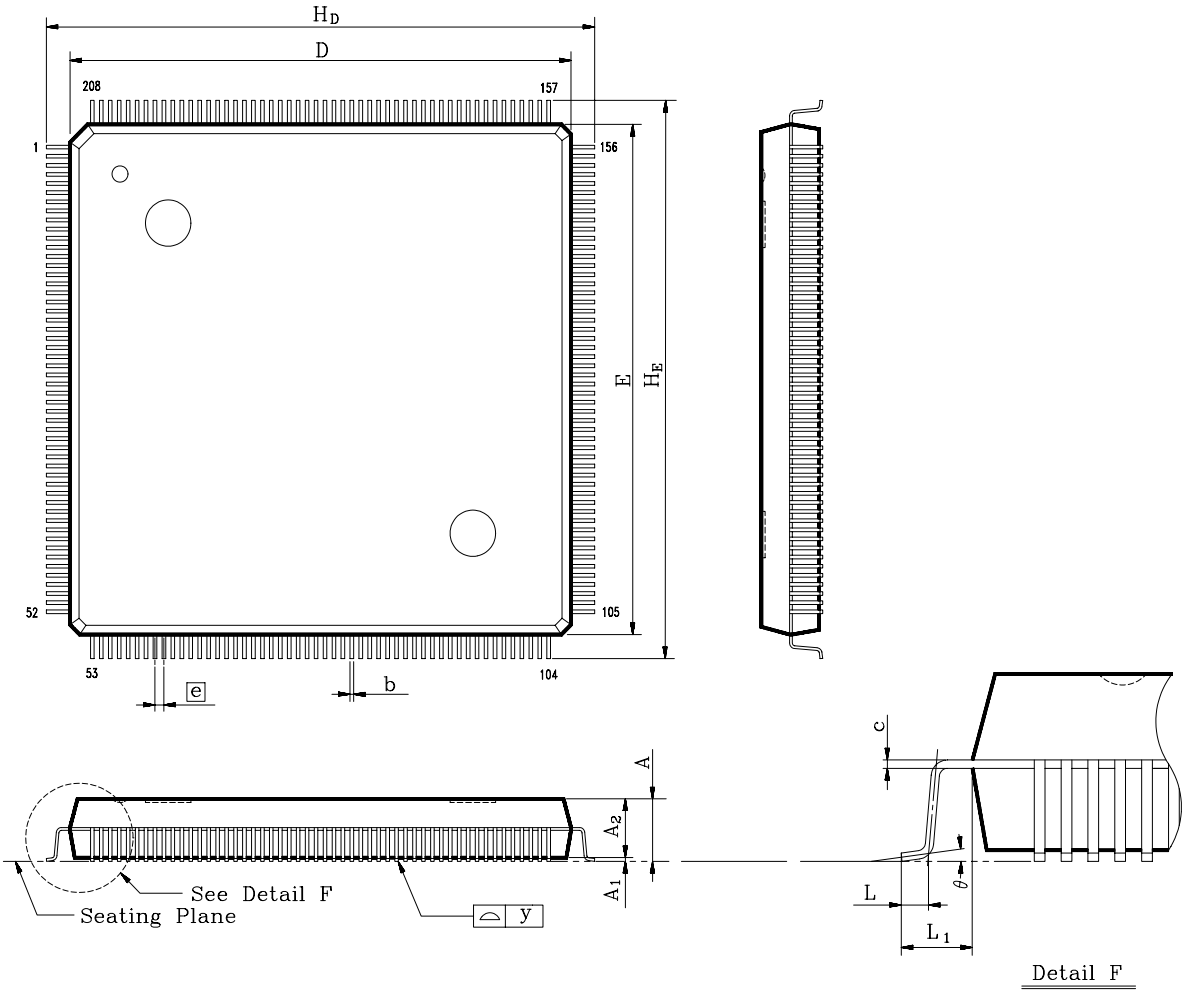


TBI Rx Timing

Symbol	Description	Min	Typical	Max	Units
tTxCC	Tx Clock Cycle		8		ns
fGTxCLK	GTxCLK frequency	125 – 100ppm	125	125 + 100ppm	MHz
tRC	Clock Rise Time of GTxCLK, RxCLK0, RxCLK1	0.7		2.4	ns
tFC	Clock Fall Time of GTxCLK, RxCLK0, RxCLK1	0.7		2.4	ns
tDUTY	Clock Duty Cycle of GTxCLK, RxCLK0, RxCLK1	40		60	%
tTxSU	Data Setup to ↑ of GTxCLK	2.0			ns
tTxHT	Data Hold from ↑ of GTxCLK	1.0			ns
tRD	Data Rise Time of Tx[9:0], Rx[9:0]	0.7			ns
rFD	Data Fall Time of Tx[9:0], Rx[9:0]	0.7			ns
fRxCLKx	RxCLK0, RxCLK1 frequency		62.5		MHz
tDRIFT	RxCLK0/1 Drift Rate	0.2			us/MHz
tRxSU	Data Setup to ↑ of RxCLK0/1	2.5			ns
tRxHT	Data Hold after ↑ of RxCLK0/1	1.5			ns
tA-B	TBI RxCLK Skew	7.5		8.5	ns

TBI Timing Parameters

12. Mechanical Dimensions



Symbol	Dimension in inch			Dimension in mm		
	Min	Typical	Max	Min	Typical	Max
A	0.136	0.144	0.152	3.45	**3.65**	3.85
A1	0.004	0.010	0.036	0.10	**0.25**	0.91
A2	0.119	0.128	0.136	3.02	**3.24**	3.46
B	0.004	0.008	0.012	0.10	**0.20**	0.30
C	0.002	0.006	0.010	0.04	**0.15**	0.26
D	1.093	1.102	1.112	27.75	**28.00**	28.25
E	1.093	1.102	1.112	27.75	**28.00**	28.25
e	0.012	0.020	0.031	0.30	**0.50**	0.80
HD	1.169	1.205	1.240	29.70	**30.60**	31.50
HE	1.169	1.205	1.240	29.70	**30.60**	31.50
L	0.010	0.020	0.030	0.25	**0.50**	0.75
L1	0.041	0.051	0.061	1.05	**1.30**	1.55
Y	-	-	0.004	-	-	0.10
Θ	0°	-	12°	0°	-	12°

Note:

1.Dimensions D & E do not include interlead flash.

2.Dimension b does not include dambar protrusion/intrusion.

3.Controlling dimension: Millimeter

4.General appearance spec. should be based on final visual Inspection spec.

TITLE : 208L QFP (28x28 mm**2) FOOTPRINT 2.6mm PACKAGE OUTLINE DRAWING			
LEADFRAME MATERIAL:			
APPROVE		DOC. NO.	530-ASS-P004
		VERSION	1
		PAGE	22 OF 22
CHECK		DWG NO.	Q208 - 1
		DATE	APR. 11.1997
REALTEK SEMICONDUCTOR CO., LTD			

Realtek Semiconductor Corp.
Headquarters
1F, No. 2, Industry East Road IX, Science-based
Industrial Park, Hsinchu, 300, Taiwan, R.O.C.
Tel : 886-3-5780211 Fax : 886-3-5776047
WWW: www.realtek.com.tw