MX98713

PMAC

100/10BASE PCI MAC CONTROLLER

1. FEATURES

* Directly supports 32-bit fast PCI bus interface

* Highly integrated with IEEE802.3 MAC and Nway in a single chip

* Supports full-duplex operation for both 100Mbps and 10Mbps

* Offers IEEE802.3u 100Mbps MII port supporting CAT3/CAT5 unshielded twisted-pair (UTP), shielded twisted-pair (STP) and fiber cables

* On-chip IEEE802.3 scrambler/descrambler, PCS, and 10Mbps interface further includes ENDEC, UTP/STP transceivers and filters

* MII management interface with Nway auto-negotiation for auto-speed selection

* PCI clock speed range from 16MHz to 33MHz, capable of zero wait state

* Large on-chip FIFO for both transmit and receive operations and no external memory is needed

* PCI bus master architecture with linked list buffer management to maximize flexibility & performance

* A native 32-bit direct memory access channel provides low CPU utilization

* Boot ROM supports for diskless application

* Offers two levels (internal and external) of loopback diagnostics capability

* Supports a variety of flexible address filtering modes :
  - normal 16 perfect addresses
  - inverse 16 perfect addresses
  - 512 hash-filtered addresses
  - 512 hash-filtered multicast addresses and one perfect address
  - pass all multicast
  - promiscuous

* MicroWire interface to external serial EEPROM which may contain Ethernet address, PCI vendor & device ID and other data

2. GENERAL DESCRIPTION

The MX98713 PCI MAC (PMAC) device is an IEEE 802.3u Media Access Controller dedicated for PCI interface and is designed to ease interfacing with CSMA/CD type local area networks, including 100Mbps-TX/FX/T4 Fast Ethernet, 10Mbps Thick Ethernet, Thin Ehternet and StarLAN with external network transceivers and 10Mbps Twisted-pair Ethernet without external transceiver. High speed PCI bus master interface is implemented to support 100Mbps fast Ethernet with fast packet buffer management. On-chip control registers and PCI configuration registers provide interface to host system for automatic bus master configuration and driver controls. As a PCI bus master, PMAC incorporates large on-chip FIFOs which provide effective local packet buffers; therefore, no external local buffer memory is needed.

The PMAC device implements all Media Access Control (MAC) layer functions for transmission and reception and Nway auto-negociation in accordance with the IEEE 802.3u standard. PMAC can be programmed to support various level of interconnects. Supported interconnects include standard Media Independent Interface (MII), 100BASE-TX Physical Coding Sublayer (PCS), NWAY Auto-negotiation for automatic speed selection and a direct 10BASE Twisted pair media interface.

The MX98713 can operate in full-duplex or half-duplex mode. A packet buffer is located in the host memory that is controlled by software driver for all incoming and outgoing packets. During reception, the PMAC stores packets in the receive buffer area, then indicates receiving status and control information in the descriptor area. This packet buffer is also used by transmission process which can transmit multiple packets from a single transmit command. Minimum-sized back-to-back packets at full line speed with interframe gap (IPG) of 0.96us in 100Mbps mode is effortless with the PMAC.

Fig. 1 depicts the MX98713 block diagram and its interface overview.

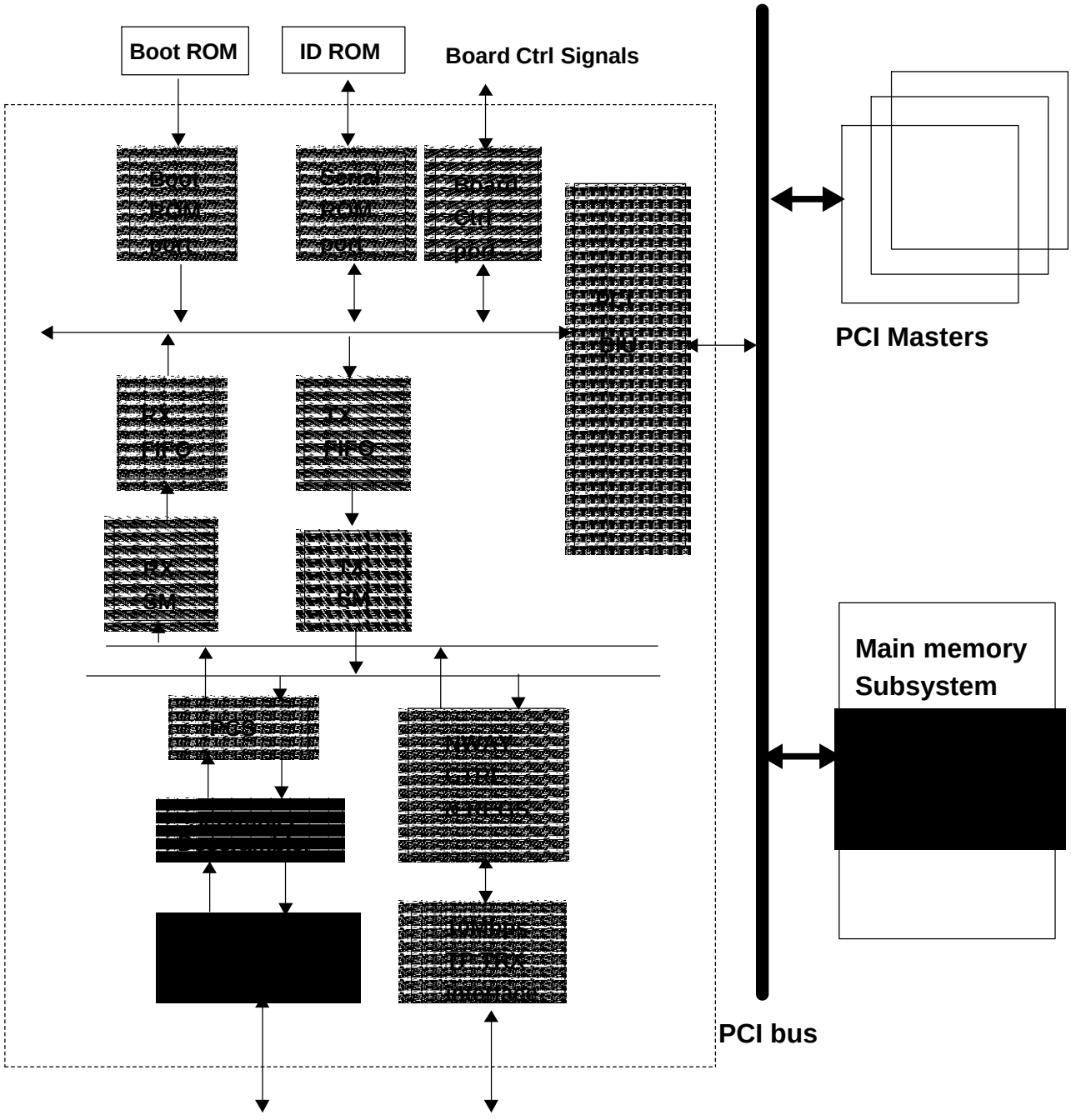
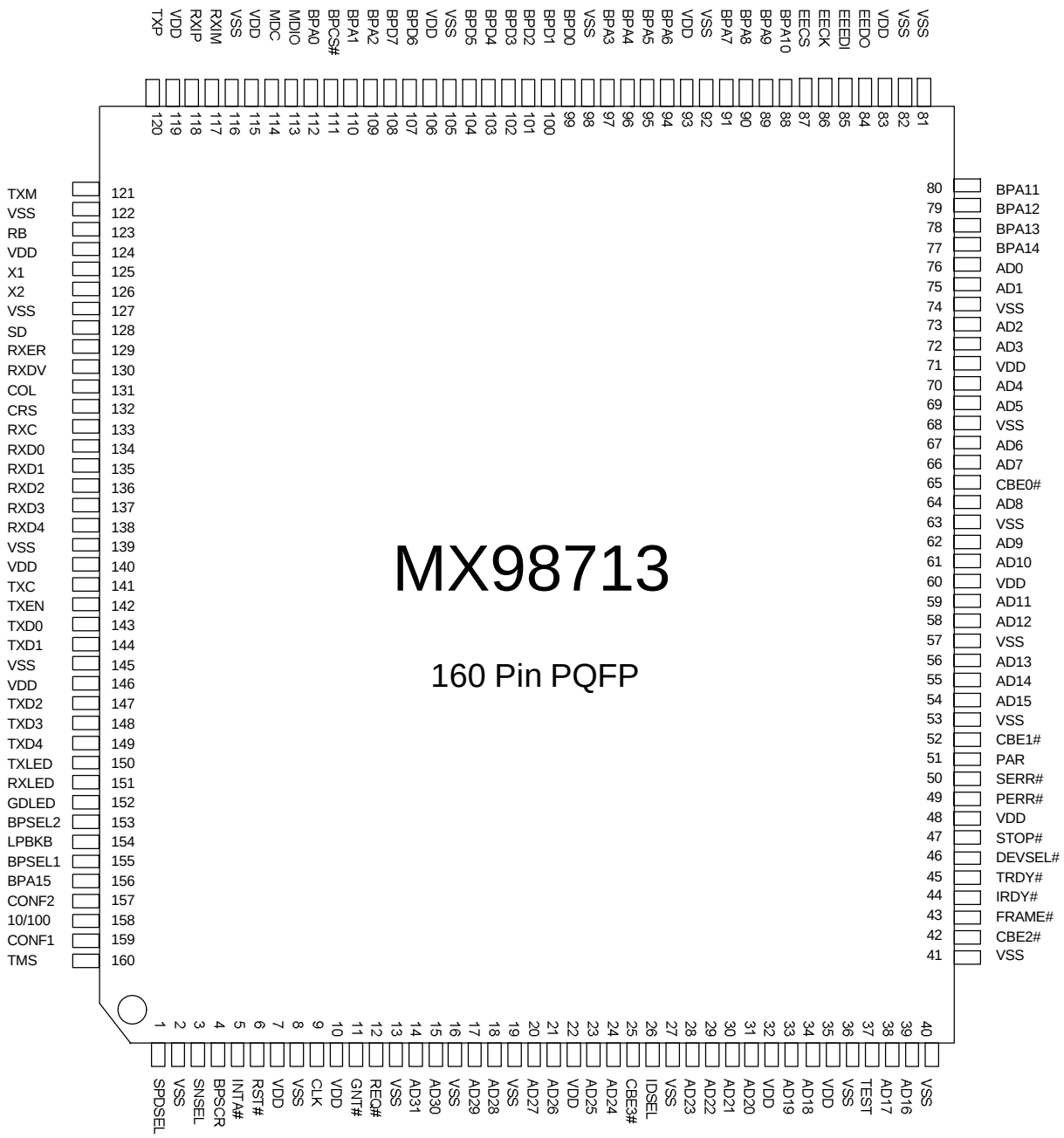


Fig. 1-- MX98713 PMAC Architecture And Interface Overview

3. PIN CONFIGURATIONS



4. MX98713 PIN DESCRIPTIONS

Pin Name	TYPE	Function and Driver Descriptions
AD[31:0]	**I/O**	**PCI address/data bus**: shared PCI address/data bus lines. Both little or big ending byte ordering are supported.
CBE[3:0]	**I/O**	**PCI command and byte enable bus**: shared PCI command byte enable bus; during the address phase of the transaction, these four bits provide the bus command. During the data phase, these four bits provide the byte enable.
FRAME#	**I/O**	**PCI FRAME# signal**: shared PCI cycle start signal, asserted to indicate the beginning of a bus transaction. While frame# is asserted, data transfers continue.
TRDY#	**I/O**	**PCI Target ready**: issued by the target agent, a data phase is completed on the rising edge of PCICLK when both IRDY# and TRDY# are asserted.
IRDY#	**I/O**	**PCI Master ready**: indicates the ability of bus master to complete the current data phase of the transaction. A data phase is completed on any rising edge of PCICLK when both IRDY# and TRDY# are asserted.
DEVSEL#	**I/O**	**PCI slave device select**: asserted by the target of the current bus access. When the MX98713 is the initiator of current bus access, the target must assert DEVSEL# within 5 bus cycles; otherwise, the cycle will be aborted.
IDSEL	**I**	**PCI initialization device select**: target specific device select signal for configuration cycles issued by host
PCICLK	**I**	**PCI bus clock input**: PCI bus clock targeted at 33MHZ
RST#	**I**	**PCI bus reset**: host system hardware reset
INTA#	**O/D**	**PCI bus interrupt request signal**: wired to INTA# lines

Pin Name	TYPE	Function and Driver Description
SERR#	**I/O**	**PCI bus system error signal**: If an address parity error is detected and CFCS bit 8 is enabled, SERR# and CFCS bit 30 will be asserted.
PERR#	**I/O**	**PCI bus data error signal**: As a bus master, when a data parity error is detected and CFCS bit 8 is enabled, CFCS bit 24 and CSR5 bit 13 will be asserted. As a bus target, a data parity check error will cause PERR# to be asserted.
PAR	**I/O**	**PCI bus parity bit**: shared PCI bus even parity bit for 32 bits address bus and CBE bus.
STOP#	**I/O**	**PCI Target requested transfer stop signal**: as bus master, assertion of STOP# causes PMAC either to retry, disconnect, or abort.
REQ#	**O**	**PCI bus request signal**: to initiate a bus master cycle request
GNT#	**I**	**PCI bus grant acknowledge signal**: asserts to indicate to PMAC that access to the bus is granted
TXLED	**O**	**TX activity indicator** : directly sink external LED circuit must be cascaded in serial with a resistor of 270~330ohm to Vdd.
RXLED	**O**	**RX activity indicator**: directly sink external LED circuit, must be cascaded in serial with a resistor of 270~330ohm to Vdd.
GDLED	**O**	**Good Link/Signal detect indicator**: directly sink external LED circuit with a cascaded resistor, indicating good link in 10Base-T setup or signal detect good in 100Base-TX setup.
LPBKB	**O**	**PHY device external loopback control** : driven by the MX98713 to force PHY device to do loopback.
BPSEL2	**I**	**Boot PROM size select bit 2** : together with BPSEL1 to inform the MX98713 the memory size of boot PROM, 00 indicates 8K Byte, 01 indicates 16K Byte, 10 indicates 32K Byte and 11 indicates 64K Byte.
BPSEL1	**I**	**Boot PROM size select bit 1**: together with BPSEL2 to inform the MX98713 the memory size of boot PROM, 00 indicates 8K Byte, 01 indicates 16K Byte, 10 indicates 32K Byte and 11 indicates 64K Byte.
BPA15	**O**	**Boot PROM address bit 15**: driven by the MX98713, together with BPA[14:0] to access external boot PROM in size up to 64KByte.

Pin Name	TYPE	Function and Driver Description
BPA[14:0]	**O**	**Boot PROM address lines**: driven by the MX98713, together with BPA15 to access external boot PROM in size up to 64KByte.
MDC	**O**	**MII management interface clock**: sourced by the MX98713
MDIO	**I/O**	**MII management interface IO data bit**
EECS	**O**	**Net ID ROM chip select**
EECK	**O**	**Net ID ROM interface clock output**
EEDI	**I**	**Net ID ROM input data bit**
EEDO	**O**	**Net ID ROM output data bit**
SD	**I**	**Signal detect indication**: supplied by external PMD device.
COL	**I**	**Collision detect of MII/SYM interface**: sourced by external physical layer protocol (PHY) device**.**
CRS	**I**	**Carrier sense of MII/SYM interface**: sourced by external physical layer protocol (PHY) device**.**
RXDV	**I**	**Receive data valid signal of MII/SYM interface**: asserted by external PHY when receive data is presented on RXD lines**.**
RXER	**I**	**Receive error signal of MII/SYM interface**: synchronous to MII_RXC and asserted by external PHY when a data decoding error occurs**.**

Pin Name	TYPE	Function and Driver Description
RXC	**I**	**Receive clock of MII/SYM interface**: supports either 25MHz or 2.5MHz clock. Sourced by external PHY.
RXD[3:0]	**I**	**Parallel Receive data lines**: driven by external PHY and is synchronous to RXC clock. In MII mode, these are received 4 data lines. In PCS mode, combined with RXD4 to form 5 parallel data lines in symbol form.
RXD4	**I**	**Received data line in PCS mode**: together with RXD[3:0] to provide five parallel lines of data in symbol and in PCS mode.
TXC	**I**	**Transmit clock of MII/SYM interface**: supports either 25MHz or 2.5 MHz clock. Sourced by external PHY.
TXD[3:0]	**O**	**Parallel Transmit data lines**: driven by PMAC synchronously to TXC clock. Data is latched by external PHY at the rising edge of TXC. In PCS mode, combined with TXD4 to form 5 parallel data lines in symbol form.
TXD4	**O**	**Transmit data line in PCS mode**: together with TXD[3:0] to provide five parallel lines of data in symbol and in PCS mode.
TXEN	**O**	**Transmit enable signal of MII/SYM interface**
BPD[7:0]	**I**	**Boot PROM data lines**: byte-wide data bus
RXIP	**I**	**Twisted pair receive differential input**: together with RXIM to provide 10BASE-T differential receive input.

Pin Name	TYPE	Function and Driver Description
RXIM	**I**	**Twisted pair receive differential input**: Together with RXIP to provide 10 BASE-T receive differential input
TXP	**O**	**Twisted pair transmit differential output**: Together with TXM to provide 10 BASE-T transmit differential output
TXM	**O**	**Twisted pair transmit differential output**: Together with TXP to provide 10 BASE-T transmit differential output
RB	**I**	**Bias control**: An external resistor (value to be determined) connects to this pin and then to ground for operating bias control
X1	**I**	**Crystal or external oscillator input**: frequency of 20MHz, used by 10 BASE-T interface.
X2	**O**	**Crystal feedback output**: Used in crystal connections only and should be left completely unconnected when using an oscillator module.
10/100	**O**	**10 BASE-T/ 100 BASE-TX enable**: When High, it indicates the 10 BASE-T enable. When Low, it indicates the 100 BASE-TX enable.
CONF2	**I**	**Configuration input bit 2**: Should be unconnected for normal operation
CONF1	**I**	**Configuration input bit 1**: Should be unconnected for normal operation
SPDSEL	**I**	**Speed Select**: Reserved for test, connected to Vdd for normal operation.
SNSEL	**I**	**Serial mode select**: Reserved for test, connected to Vdd for normal operation.
BPSCR	**I**	**Bypass Scrambler mode**: Reserved for test; ground this pin for normal operation.
TMS	**I**	**NWAY test mode select**: Reserved for test, connected to Vdd for normal operation.
TEST	**I**	**TEST pin**: must be grounded.

5. FUNCTIONAL AND OPERATIONAL DESCRIPTIONS

5.1. PCI CONFIGURATION REGISTERS

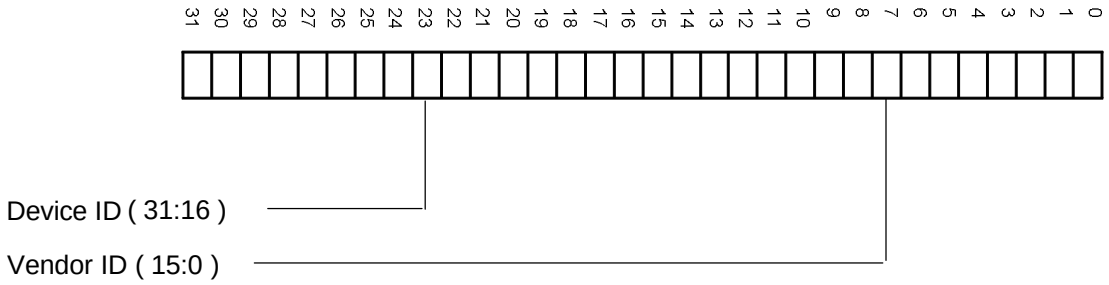
5.1.1. PCI CONFIGURATION MAPPING

System BIOS will examine the configuration requirements of each PCI card on motherboard at boot-up procedure and assign every PCI card a unique I/O or memory base address. A total of 64 bytes are defined as PCI configuration space located on each PCI card which can be accessed by an offset address during PCI configuration cycles. PCI register mapping is demonstrated as follows :

00-01h	Vendor ID
02-03h	Device ID
04-05h	Command register
06-07h	Status register
08h	Revision ID
09-0Bh	Class code
0Ch	Cache line size
0Dh	Latency timer
0Eh	Header type
0Fh	BIST
10-13h	IO base address
14-17h	Memory base address
18-1Bh	Base address 1 (not used)
1C-1Fh	Base address 2 (not used)
20-23h	Base address 3 (not used)
24-27h	Base address 4 (not used)
28-2Bh	Reserved
2C-2Fh	Reserved
30-33h	Expansion ROM base address
34-37h	Reserved
38-3Bh	Reserved
3Ch	Interrupt line
3Dh	Interrupt pin
3Eh	Min_Gnt
3Fh	Max_Lat
40h	Driver area for the driver's special usage

5.1.2. PCI ID RREGISTER (PFID)

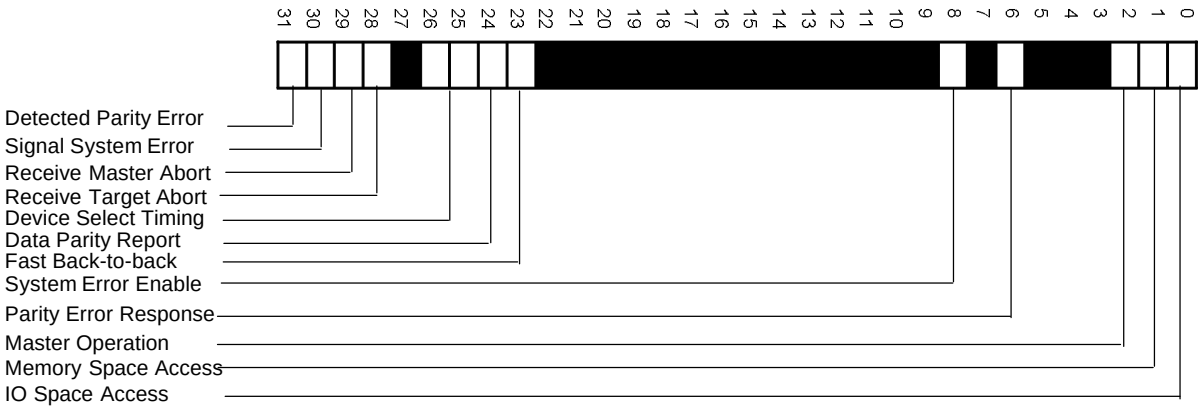
PFID Register (03h-00h)



These two fields used as a loaded from external serial PROM or used as a preset value of "10D9" at user's choice. Location 3Dh in serial PROM is device ID and 3Eh is vendor ID. If location 3Eh contains "FFFF" value, which is an invalid ID, then internal preset value of "10D9" is used by PMAC instead; otherwise, both 3Dh and 3Eh are loaded from serial PROM. When location 3Eh contains "FFFF", device ID is internally preset to "0512" for the MX98713.

5.1.3. PCI CCOMMAND AND STATUS RREGISTER (PFCS)

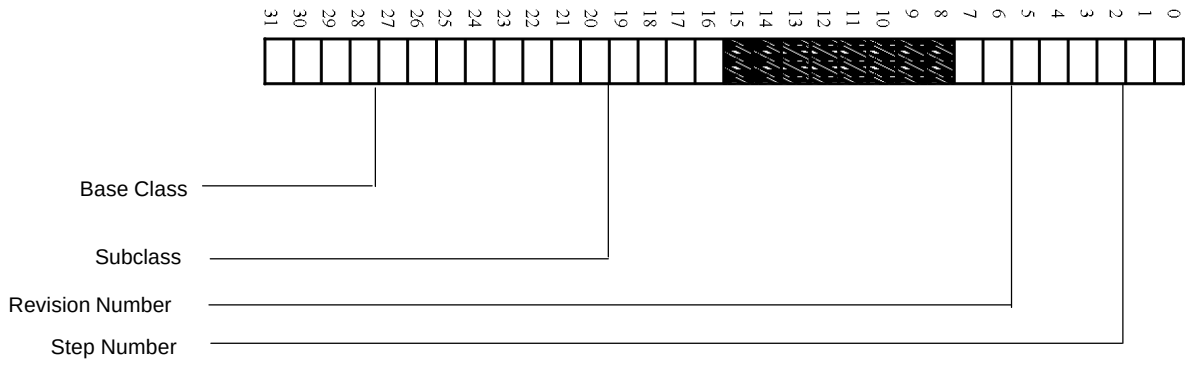
PFCS Register (07h-04h)



The bit content will be reset to 0 when a 1 is written to the corresponding bit location.
bit 0 : IO Space Access, set to 1 to enable IO access
bit 1: Memory Space Access, set to 1 to enable memory access
bit 2: Master Operation, set to 1 to support bus master mode
bit 3: bit 5 :not used
bit 6: Parity Error Response, set to 1 to enable the PMAC to assert PERR# if parity error detected.
bit 7: not used
bit 8: System Error Enable, set to 1 to enable the PMAC to assert SERR# when parity error is detected on address lines and CBE[3:0]# .
bit 22 - bit 9: not used
bit 23: Fast Back-to-back, always set by the PMAC to accept fast back-to-back transactions that are not sent to the same bus device.
bit 24: Data Parity Report, is set to 1 by the PMAC only if PMAC is bus master, it sends or causes PERR# active and PFCS<6> is also set.
biut 26 -bit 25: Device Select Timing, fixed at 01 which indicates a medium assertion speed of DEVSEL#.
bit 27: not used
bit 28: Receive Target Abort, is set to indicate the PMAC master transaction is terminated by a target abort.
bit 29: Receive Master Abort, is set to indicate the PMAC terminated a master transaction with Master abort
bit 30: Signal System Error, is set to indicate the PMAC asserted SERR#.
bit 31: Detected Parity Error, is set whenever a parity error detected regardless of PFCS<6>.

5.1.4. PCI REVISION REGISTER (PFRV)

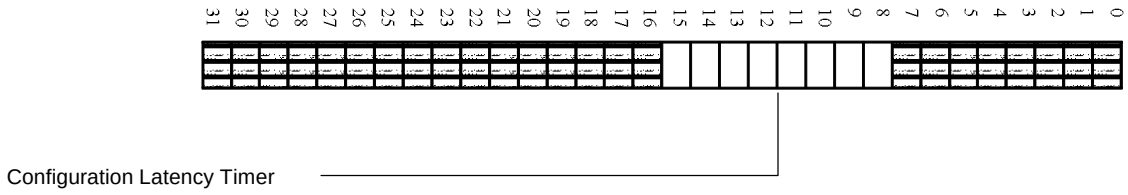
PFRV Register (0Bh-08h)



bit 3 - bit 0 : Step Number, fixed to 0h and incremented for subsequent steps of the version.
bit 7 - bit 4 : Revision Number, fixed to 0h and is incremented for subsequent revisions.
bit 15 - bit 8 : not used
bit 23 - bit 16 : Subclass, fixed to 0h.
bit 31 - bit 24 : Base Class, fixed to 2h.

5.1.5. PCI LATENCY TIMER REGISTER (PFLT)

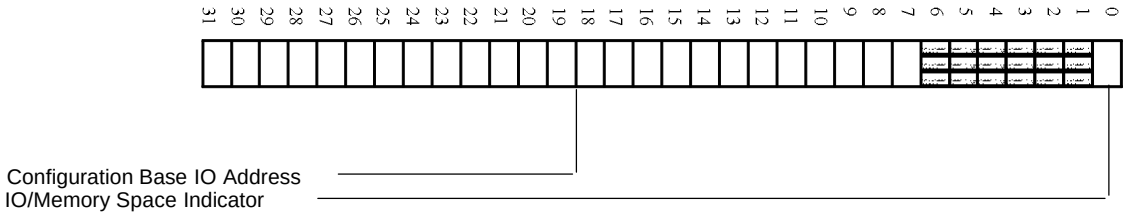
PFLT Register (0Fh-0Ch)



When the PMAC asserts FRAME#, it enables its latency timer to begin counting. If the PMAC deasserts FRAME# prior to timer expiration, timer will be ignored. Otherwise, after timer expires, the PMAC initiates transaction termination as soon as its GNT# is deasserted.

5.1.6. PCI IO BASE ADDRESS REGISTER (PBIO)

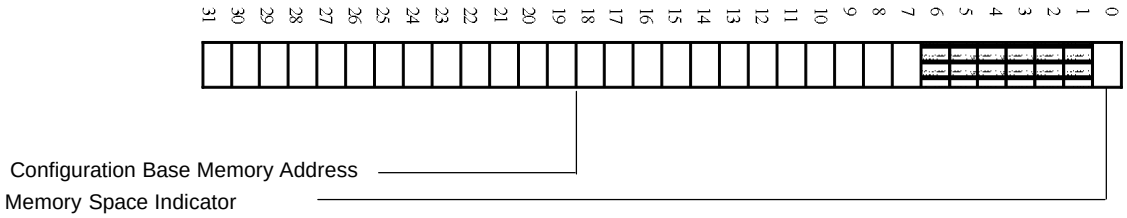
PBIO Register (13h-10h)



bit 0 : IO/Memory Space Indicator, fixed to 1 will map into the IO space. This is a read only field.
bit 6 - bit 1 : not used.
bit 31 - bit 7 : Defines the address assignment mapping of PMAC CSR registers.

5.1.7. PCI MEMORY BASE ADDRESS REGISTER (PBMA)

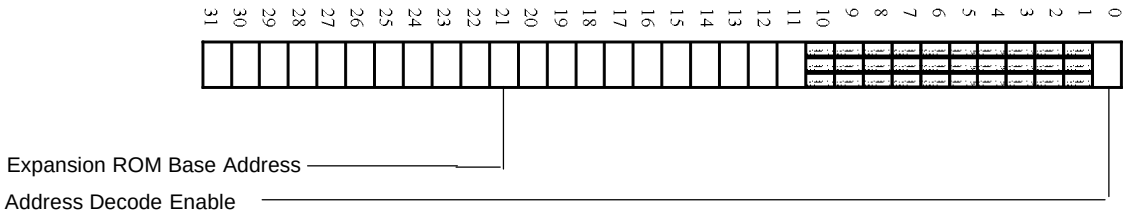
PBMA Register (17h-14h)



bit 0 : Memory Space Indicator, fixed to 0 will map into the memory space. This is a read only field.
bit 6 - bit 1 : not used.
bit 31 - bit 7 : Defines the address assignment mapping of PMAC CSR registers.

5.1.8.PCI BASE EXPANSION ROM ADDRESS REGISTER (PBER)

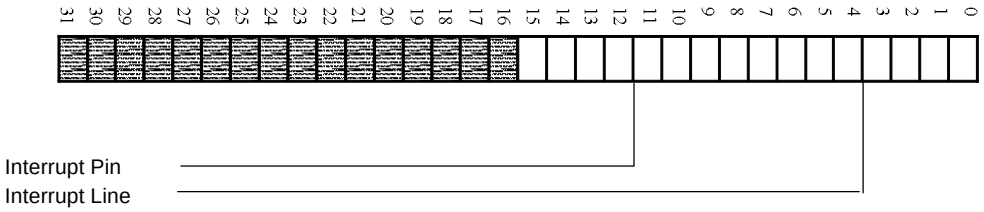
PBER Register (33h- 30h)



bit 0 : Address Decode Enable, decoding will be enabled when both enable bit in PFCS<1>, and this expansion ROM register bit is 1.
bit 10 - bit 1 : not used.
bit 31 - bit 11 : Defines the 21 bits of expansion ROM base address.

5.1.9. PCI INTERRUPT REGISTER (PFIT)

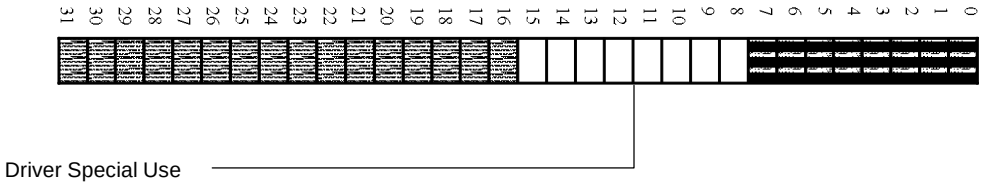
PFIT Register (3Fh- 3Ch)



bit 7 - bit 0 : Interrupt Pin, fixed to 01h which use INTA#.
bit 15 - bit 8 : Interrupt Line, system BIOS will write the routing information into this field, and driver can use this information to determine the priority and interrupt vector.
bit 31 - bit 16 : not used.

5.1.10. PCI DRIVER AREA REGISTER (PFDA)

PFDA Register (40h)



bit 7 - bit 0 : not used.
bit 15 - bit 8 : driver is free to read and write this field for any driver special purpose.
bit 31 - bit 16 : not used.

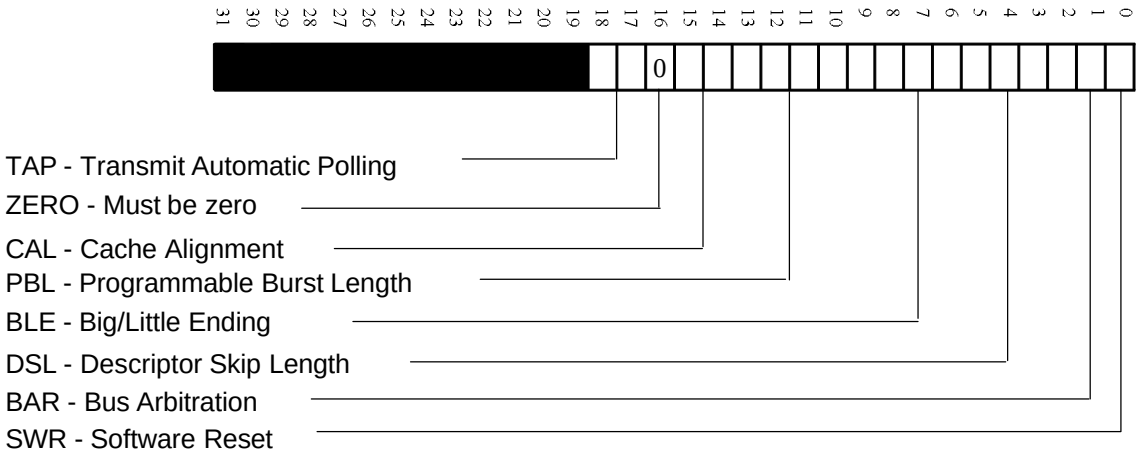
5.2. HOST INTERFACE REGISTERS

The PMAC Control and Status Registers (CSRs) are located in the host I/O or memory address space. The CSRs are double word aligned and 32 bits long. Definitions and address for all CSRs are demonstrated below:

CSR Mapping

Register	Meaning	Offset from CSR Base Address (PBIO and PBMA)
CSR0	Bus mode	00h
CSR1	Transmit poll demand	08h
CSR2	Receive poll demand	10h
CSR3	Receive list demand	18h
CSR4	transmit list base address	20h
CSR5	Status	28h
CSR6	Operation mode	30h
CSR7	Interrupt enable	38h
CSR8	Missed frame counter	40h
CSR9	Serial ROM and MII management	48h
CSR10	reserved	50h
CSR11	General-purpose timer	58h
CSR12	General-purpose port	60h
CSR13	reserved	68h
CSR14	reserved	70h
CSR15	Watchdog timer	78h
CSR16	Test Operation Register	80h

5.2.1. BUS MODE REGISTER (CSR0)

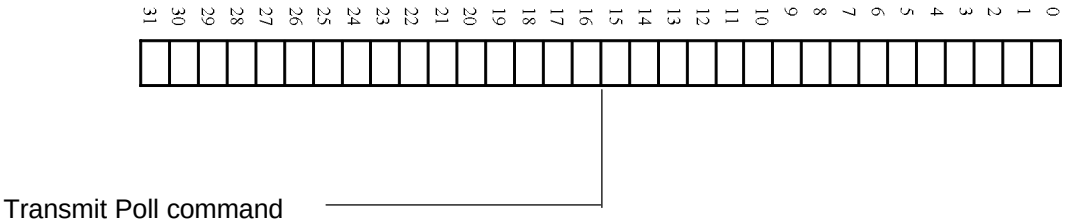


Field	Name	Description
0	SWR	Software Reset, when set, PMAC resets all internal hardware with the exception of the configuration area and port selection.
1	BAR	Bus Arbitration, when set, a round-robin arbitration scheme is applied resulting in equal sharing of internal bus. When reset, receive channel has higher priority over transmit channel in case of possible danger of receive FIFO overrun situation.
6:2	DSL	Descriptor Skip Length, specifies the number of long words to skip between two descriptors for implicit chained structure.
7	BLE	Big/Little Endian, set for big endian byte ordering mode, reset for little endian byte ordering mode
13:8	PBL	Programmable Burst Length, specifies the maximum number of long words to be transferred in one DMA transaction. default is 0 which means 4 double words, possible values can be 1,2,4,8,16 or 32.
15:14	CAL	Cache Alignment, programmable address boundaries of data burst stop, PMAC can handle non-cache-aligned fragment as well as cache-aligned fragment efficiently.
18:17	TAP	Transmit Auto-Polling time interval, defines the time interval for PMAC to performs transmit polling command automatically at transmit suspended state.

Table 1 -- Transmit Auto Polling bits

CSR<18:17>	Time Interval
00	No transmit auto-polling, a write to CSR1 is required to poll
01	auto-poll every 200 us
10	auto-poll every 800 us
11	auto-poll every 1.6 ms

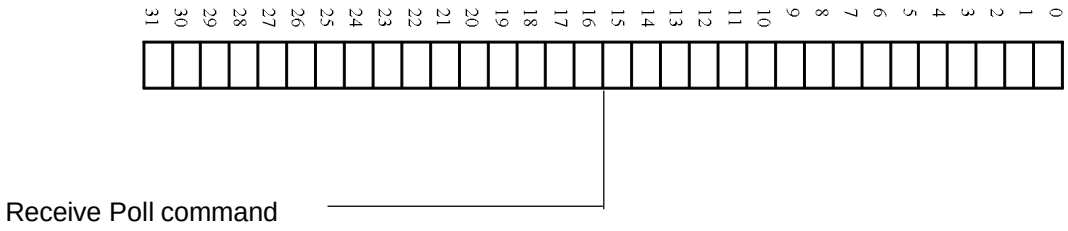
5.2.2. TRANSMIT POLL COMMAND (CSR1)



Value after reset is "FFF80000"h

Field	Name	Description
31:0	TPC	Write only, when written with any value, PMAC will read transmit descriptor list in host memory pointed by CSR4 and then process the list.

5.2.3. RECEIVE POLL COMMAND (CSR2)

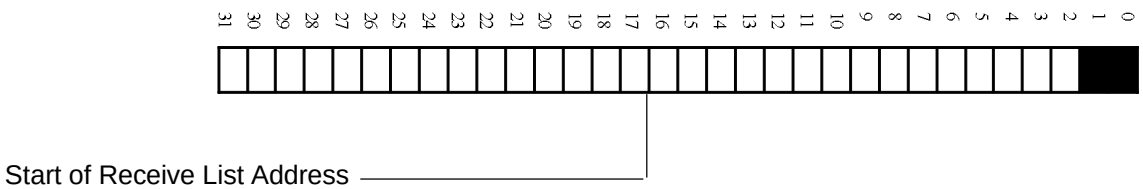


Value after reset is "FFFFFFFF"h

Field	Name	Description
31:0	RPC	Write only, when written with any value, PMAC reads receive descriptor list in host memory pointed by CSR4 and processes the list.

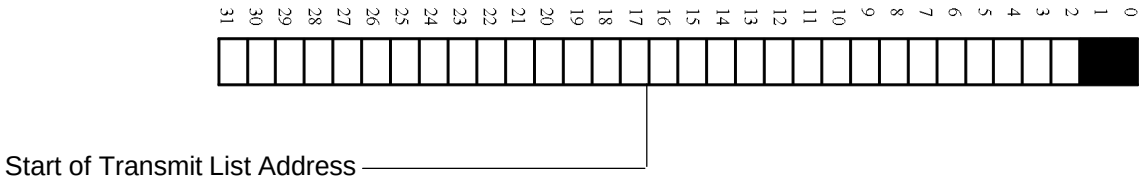
5.2.4. DESCRIPTOR LIST ADDRESS (CSR3, CSR4)

CSR3 for Receive List Base Address



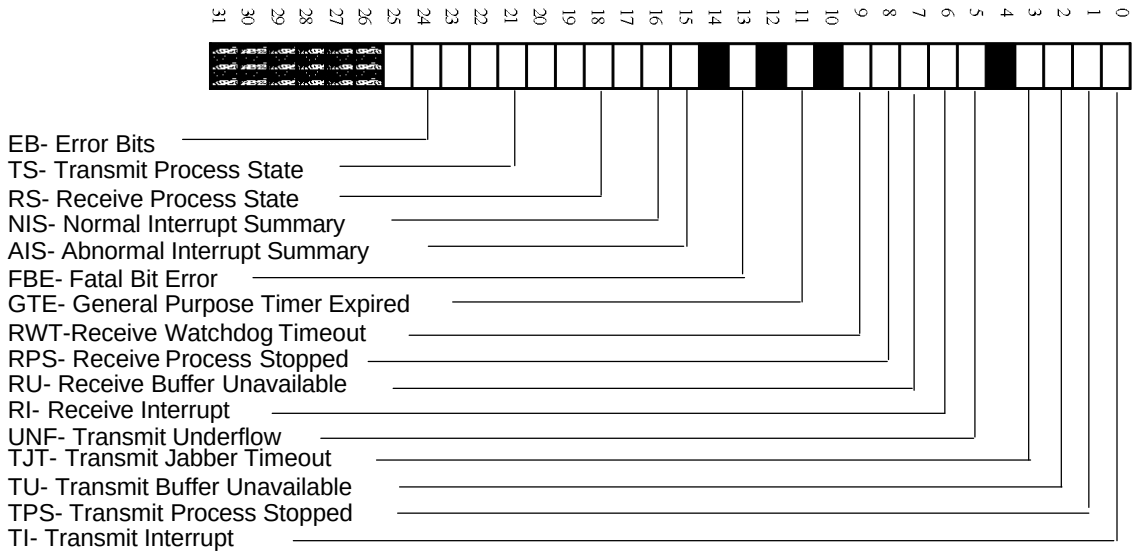
Value after reset is unpredictable.

CSR4 for Transmit List Base Address



Value after reset is unpredictable

5.2.5. STSTUS REGISTER (CSR5)



Value after reset is "FC005410"h

Field	Name	Description
25:23	EB	Error Bits, read only bits indicating the type of error that induces fatal bus error.
22:20	TS	Transmit Process State, read only bits indicating the state of transmit process.
19:17	RS	Receive Process State, read only bits indicating the state of receive process.
16	NIS	Normal Interrupt Summary, is the logical OR of CSR5<0>, CSR5<2> and CSR5<6>.
15	AIS	Abnormal Interrupt Summary, to show the results of logical OR of CSR5<1>, CSR5<3>, CSR5<5>, CSR5<7>, CSR5<8>, CSR5<9>, CSR5<11> and CSR5<13>.
13	FBE	Fatal Bus Error, indicating a system error occurred, PMAC will disable all bus access.
11	GTE	General Purpose Timer Expired, indicating CSR11 counter has expired.
9	RWT	Receive Watchdog Timeout, reflects the network line status where receive watchdog timer has expired while the other node is still active on the network. If overflow also occurs, the packet might not be received.
8	RPS	Write only, when written with any value, PMAC reads receive descriptor list in host memory pointed by CSR4 and processes the list.
7	RU	Receive Buffer Unavailable, the reception process is suspended because the next descriptor in the receive list is owned by host. If no receive poll command is issued, the reception process will resume when the next recognized incoming frame is received.
6	RI	Receive Interrupt, indicating the completion of a frame reception.
5	UNF	Transmit Underflow, indicating transmit FIFO has run empty before the completion of a packet transmission.
3	TJT	Transmit Jabber Timeout, indicating the PMAC has been excessively active. The transmit process is aborted and placed in the stopped state. TDES0<1> is set also.
2	TU	Transmit Buffer Unavailable, transmit process is suspended because the next descriptor in the transmit list is owned by host.
1	TPS	Transmit Process Stopped.
0	TI	Transmit Interrupt. indicating a frame transmission was completed.

Table 2 -- Fatal Bus Error Bits

CSR5<25:23>	Process State
000	parity error for either SERR# or PERR#, cleared by software reset.
001	master abort
010	target abort
011	reserved
1XX	reserved

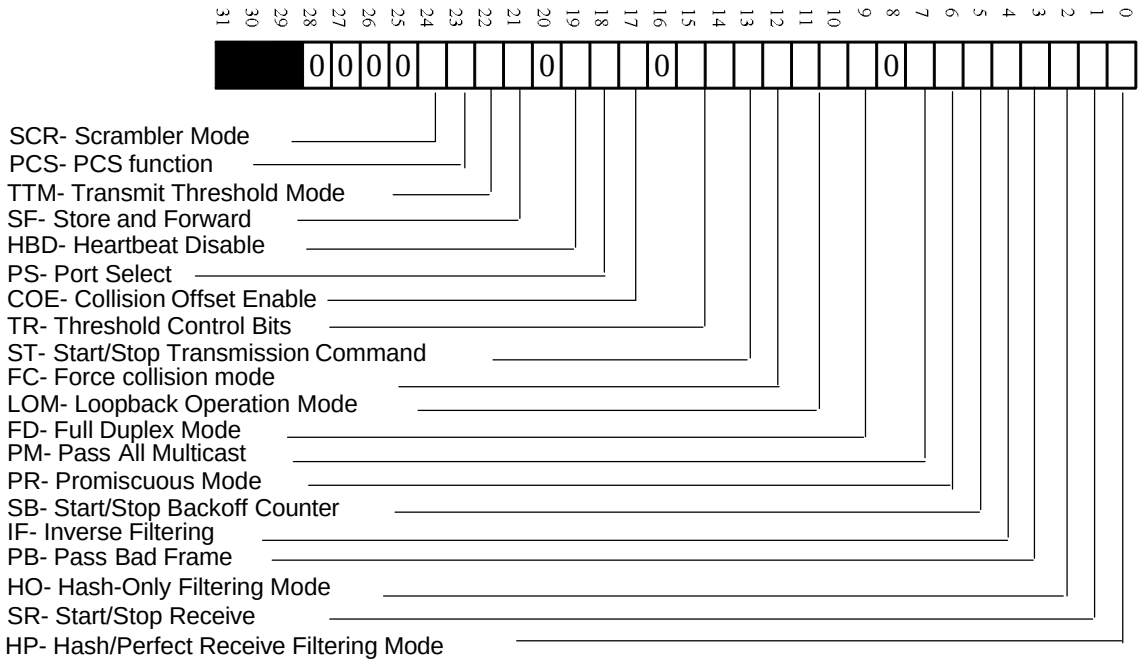
Table 3 -- Transmit Process State

CSR5<22:20>	Process State
000	Stopped-reset or transmit jabber expired.
001	Fetching transmit descriptor
010	Waiting for ending of transmission
011	filling transmit FIFO
100	reserved
101	Setup packet
110	Suspended, either FIFO underflow or unavailable transmit descriptor
111	close transmit descriptor

Table 4 -- Receive Process State

CSR5<19:17>	Process State
000	Stopped-reset or stop receive command.
001	Fetching receive descriptor
010	checking for end of receive packet
011	Waiting for receive packet
100	Suspended, receive buffer unavailable
101	closing receive descriptor
110	Purging the current frame from the receive FIFO due to unavailable receive buffer
111	queuing the receive frame from the receive FIFO into host receive buffer

5.2.6. OPERATION MODE REGISTER (CSR6)



Value after reset is "E0000040"h

Field	Name	Description
24	SCR	Scrambler Mode, set to enable scrambler function and the MII/SYM port transmit and receive scrambled symbols.
23	PCS	Set to enable PCS functions and the MII/SYM port operates in symbol mode. CSR6<18> must be set in order to operate in MII/ SYM port.
22	TTM	Transmit Threshold Mode, set for 10Mbps and reset for 100Mbps.
21	SF	Store and Forward, when set, transmission starts only if a full packet is in transmit FIFO; the threshold values defined in CSR6<15:14> is ignored
19	HBD	Heartbeat Disable, set to disable SQE function in 10Mbps mode. This bit should be set in MII/SYM port.
18	PS	Port Select, set for MII/SYM port. A software reset does not affect this bit.
17	COE	Collision Offset Enable, set to enable a modified backoff algorithm during low collision situation, reset for normal backoff algorithm.
15:14	TR	Threshold Control Bits, these bits control the selected threshold level for PMAC's transmit FIFO; transmission starts when frame size within the transmit FIFO is larger than the selected threshold. Full frames with a length less than the threshold are also transmitted.

13	ST	Start/Stop Transmission Command, set to place transmission process in running state and will try to transmit current descriptor in transmit list. When reset, transmit process is placed in stop state.
12	FC	Force Collision Mode, used in collision logic test in internal loopback mode, set to force collision during next transmission attempt. This can result in excessive collision reported in TDES0<8> if 16 or more collisions.
11:10	LOM	Loopback Operation Mode, see table 7.
9	FD	Full-Duplex Mode, set for simultaneous transmit and receive operation, heartbeat check is disabled, TDES0<7> should be ignored, and internal loopback is not allowed. His bit is in the UII port. When not MII port, Auto-negotiation process decides full-duplex or half-duplex.
7	PM	Pass All Multicast, set to accept all incoming frames with a multicast destination address are received. Incoming frames with physical address are filtered according to the CSR6<0> bit.
6	PR	Promiscuous Mode, any incoming valid frames are accepted.
5	SB	Start/Stop Backoff Counter, when reset, the backoff timer is not affected by the network carrier activity. Otherwise, timer will start counting when carrier drops.
4	IF	Inverse Filtering, read-only bit, set to operate in inverse filtering mode; only valid during perfect filtering mode.
3	PB	Pass Bad Frames, set to pass bad frame mode, all incoming frames passing the address filtering are accepted including runt frames, collided fragments, truncated frames caused by FIFO overflow.
2	HO	Hash-Only Filtering Mode, read-only bit, set to operate in imperfect filtering mode for both physical and multicast addresses.
1	SR	Start/Stop Receive, set to place receive process in running state where descriptor acquisition is attempted from current position in the receive list. Reset to place the receive process in stop state.
0	HP	Hash/Perfect Receive Filtering Mode, read only bit, set to use hash table to filter multicast incoming frames. If CSR6<2> is also set, then the physical addresses are imperfect address filtered too. If CSR6<2> is reset, then physical addresses are perfect address filtered, according to a single physical address as specified in setup frame.

Table 5 -- Transmit Threshold

CSR6<21>	CSR6<15:14>	CSR6<22>=0	CSR6<22>=1 (Threshold bytes)
0	00	128	72
0	01	256	96
0	10	512	128
0	11	1024	160
1	XX	(Store and Forward)	

Table 6 -- Port Data Rate Selection

CSR6<18>	CSR6<22>	CSR6<23>	CSR6<24>	Port	Data Rate	Function
1	1	0	0	MII/SYM	10Mbps	10 Base MII
1	0	0	0	MII/SYM	100Mbps	100MB/s MII
1	0	1	0	MII/SYM	100Mbps	PCS for 100Base-FX
1	0	1	1	MII/SYM	100Mbps	PCS and SCR for 100Base-TX

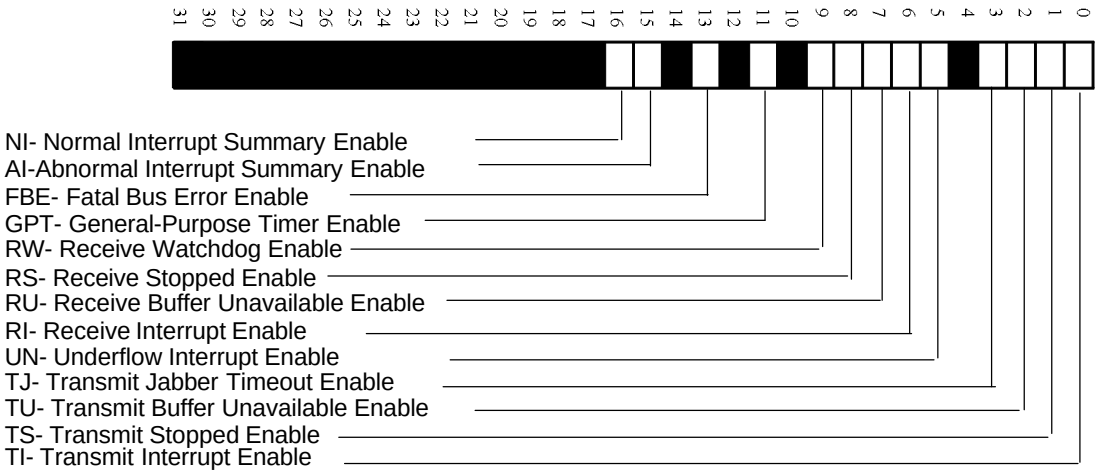
Table 7 -- Loopback Operation Mode

CSR6<11:10>	Operation Mode
00	Normal
01	Internal Loopback, for serial and MII port only
10	External Loopback
11	Reserved

Table 8 -- Filtering Mode

CSR6<7>	CSR6<6>	CSR6<4>	CSR6<2>	CSR6<0>	Filtering Mode
0	0	0	0	0	16 perfect filtering
0	0	0	0	1	512-bit hash + 1 perfect filtering
0	0	0	1	1	512-bit hash for multicast and physical addresses
0	0	1	0	0	Inverse filtering
X	1	0	0	X	Promiscuous
0	1	0	1	1	Promiscuous
1	0	0	0	X	Pass All Multicast
1	0	0	1	1	Pass All Multicast

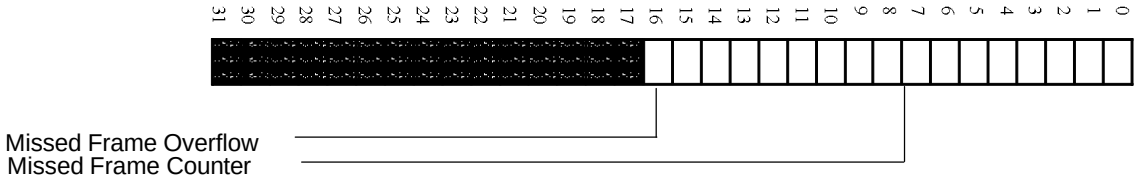
5.2.7. INTERRUPT MASK REGISTER (CSR7)



Value after reset is "FFFE5410"h

Field	Name	Description
16	NI	Normal Interrupt Summary Enable, set to enable CSR5<0>, CSR5<2>, CSR5<6>.
15	AI	Abnormal Interrupt Summary enable, set to enable CSR5<1>, CSR5<3>, CSR5<5>, CSR5<7>, CSR5<8>, CSR5<9>, CSR5<11> and CSR5<13>.
13	FBE	Fatal Bus Error Enable, set together with with CSR7<15> enables CSR5<13>.
11	GPT	General_-Purpose Timer Enable, set together with CSR7<15> enables CSR5<11>.
9	RW	Receive Watchdog Timeout Enable, set together with CSR7<15> enables CSR5<9>.
8	RS	Receive Stopped Enable, set together with CSR7<15> enables CSR5<8>.
7	RU	Receive Buffer Unavailable Enable, set together with CSR7<15> enables CSR5<7>.
6	RI	Receive Interrupt Enable, set together with CSR7<16> enables CSR5<6>.
5	UN	Underflow Interrupt Enable, set together with CSR7<15> enables CSR5<5>.
3	TJ	Transmit Jabber Timeout Enable, set together with CSR7<15> enables CSR5<3>.
2	TU	Transmit Buffer Unavailable Enable, set together with CSR7<16> enables CSR5<2>.
1	TS	Transmit Stop Enable, set together with CSR7<15> enables CSR5<1>.
0	TI	Transmit Interrupt Enable, set together with CSR7<16> enables CSR5<0>.

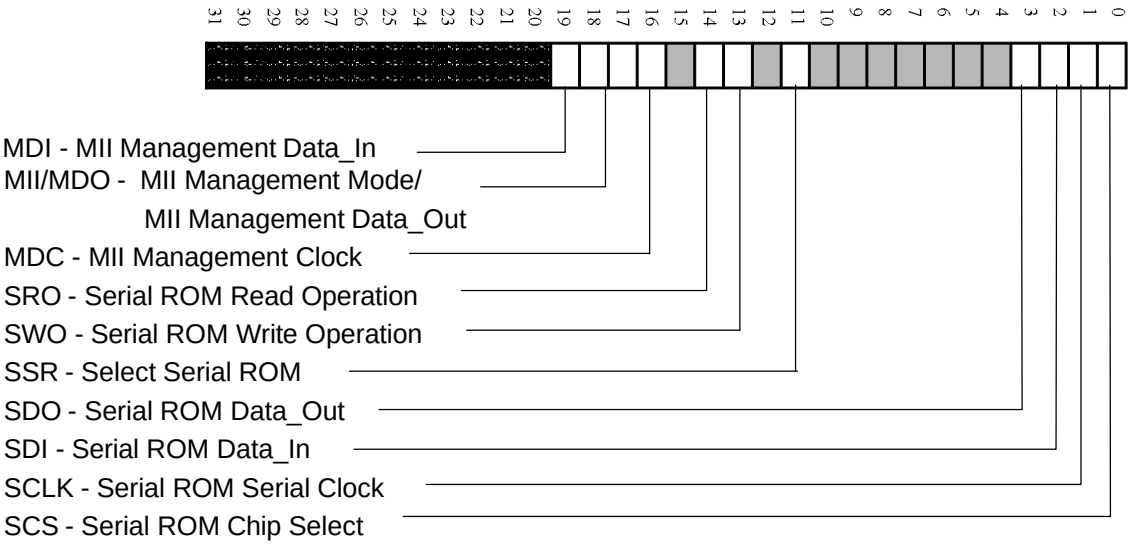
5.2.8. MISSED FRAME COUNTER (CSR8)



Value after reset is "FFFE0000"h

Field	Name	Description
16	MFO	Missed Frame Overflow, set when missed frame counter overflow, reset when CSR8 is read.
15:0	MFC	Missed Frame Counter, indicates the number of frames discarded because no host receive descriptor was available.

5.2.9. SERIAL ADDRESS ROM AND MII MANAGEMENT REGISTER (CSR9)



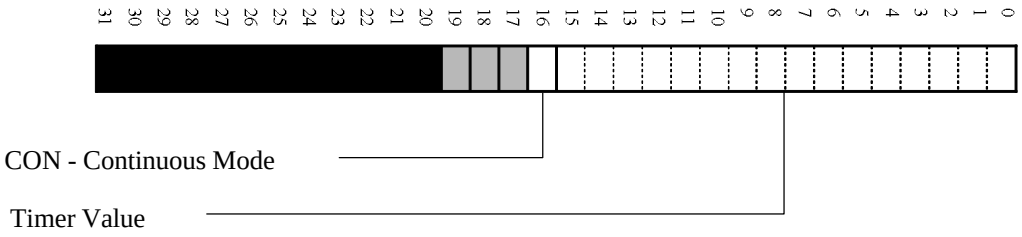
Value after reset is "FFF097F0"h

Field	Name	Description
19	MDI	Management data read from MDIO pin.
18	MMD	Defines the operation mode of the PHY.
17	MDO	The management data writes to the PHY through MDIO pin.
16	MDC	MII management clock is used as timing reference of MDIO signal
14	SRO	When set together with SSR(CSR9<11>), the MX98713 performs a read cycle from the serial ROM. When set and SSR is reset, the MX98713 performs a write cycle to PHY.
13	SWO	When set together with SSR, the MX98713 executes a write cycle to the serial ROM. When set and SSR is reset, the MX98713 executes a write cycle to the PHY.
11	SSR	When set together with either SRO(CSR9<14>) or SWO(CSR9 <13>), the MX98713 selects the serial ROM.
3	SDO	Serial ROM data out from serial ROM into the MX98713.
2	SDI	Serial ROM data input to serial ROM from the MX98713.
1	SCLK	Serial clock output to serial ROM.
0	SCS	Chip select output to serial ROM.

Table 9 -- MII Management Operation Mode

CSR9<18>	CSR9<17>	Write	Read	Value
0	0	yes	-	0
0	1	yes	-	1
1	X	-	yes	-

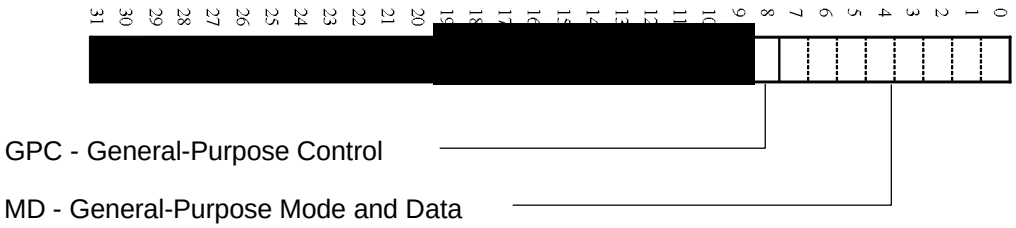
5.2.10. GENERAL PURPOSE TIMER (CSR11)



Timer value after reset is "FFFE0000"H.

Field	Name	Description
16	CON	When set,the general purpose timer is in continuous operating mode. When reset, the timer is in one-shot mode.
15:0	Timer	Value contains the timer value in a cycle time of 204.8us.

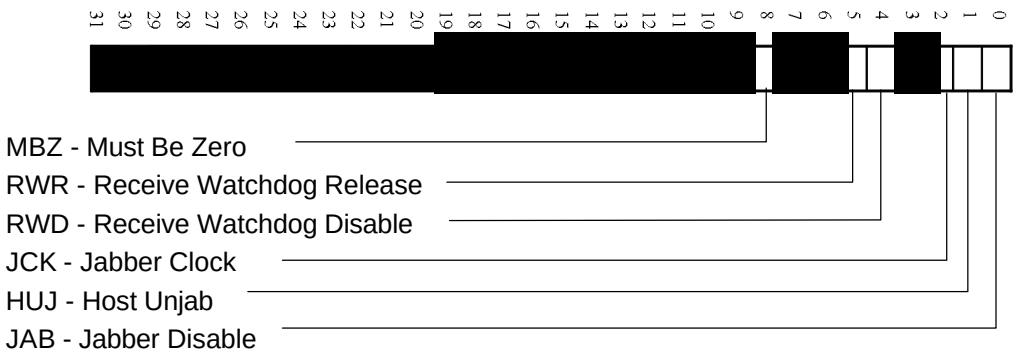
5.2.11. GENERAL PURPOSE PORT (CSR12)



The register value after reset is "FFFFFEXX"h.

Field	Name	Decription
8	GPC	Determines whether accessing CSR12<7:0> affects either the direction of each pin (input or output) or the data of each pin(1 or 0). The interaction of this bit and CSR12<7:0> is described in the following field.
7:0	MD	When CSR12<8> is set the value that is written by the host to CSR12<7:0> sets the direction of each pin to be either an input pin(1) or an output pin(0). When a hardware reset is initiated, all gep pins become input pins. When GPC is reset any host write access to CSR12<7:0> sets value on the pins that are configured as output pins. When GPC is reset any host read access to CSR12<7:0> reflects the input values on any pins defined as input pins and output values on any pins defined as output pins. The application of the general-purpose pins in board design should be correlated with the way the port driver software is using it.

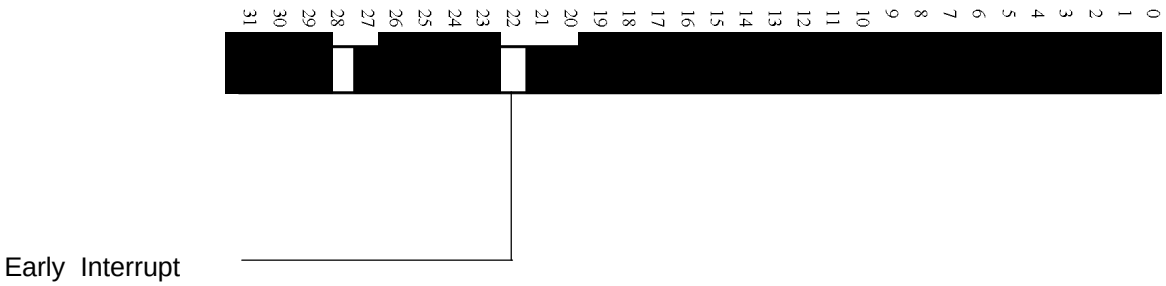
5.2.12. WATCHDOG TIMER (CSR15)



The register value after reset is "FFFFFEC8"h.

Field	Name	Description
8	MBZ	This bit should always be programmed to 0.
5	RWR	Defines the time interval of no carrier from receive watchdog expiration until reenabling the receive channel. When set the receive watchdog is released 40-48 bit times from the last carrier deassertion. When reset the receive watchdog is released 16 to 24 bit times from the last carrier deassertion.
4	RWD	When set the receive watchdog counter is disable. When reset, receive carriers longer than 2560 bytes are guaranteed to cause the watchdog counter to time out. Packets shorter than 2048 bytes are guaranteed to pass.
2	JCK	When set transmission is cut off after a range of 2048 bytes to 2560 bytes is transmitted, When reset transmission for the 10Mbps port is cut off after a range of 26 ms to 33ms. When reset transmission for the 100Mbps port will be cut off after the period of 2.6ms to 3.3ms.
1	HUJ	Defines the time interval between transmit jabber expiration until reenabling of the transmit channel. When set the transmit channel is relased immediately after the jabber expiration. When reset the jabber is released 365ms to 420ms after jabber expiration for 10Mbps port. When reset the jabber is released 36.5ms to 42ms after the jabber expiration for 100Mbps port.
0	JBD	Jabber Disable, set to disable transmit jabber function.

5.2.13. MISCELLANEOUS CONTROL REGISTER (CRS16)



Field	Name	Description
22	ErInt	Set to 1 will enable early interrupt assertion before end of current packet receiving or transmission. PMAC will determine a good time to assert interrupt depending on the size of current packet.
Others		Reserved bits must be preserved as initialized value by MXIC's driver.