FreeBSD ARM64: Porting on a new board

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Who am I ?

- ARM Kernel Hacker for 2 and half year
- Self proclaimed maintainer for Allwinner SoCs (and now RockChip)
- Self proclaimed DTS Maintainer in FreeBSD
- U-Boot Maintainer
- Upstream guy in Linux for DTS and U-Boot

Agenda

- ARM/SoC/SBC
- Bootloader
- Serial
- First kernel boot
- Clocks and Resets
- Clock API

What is an SoC ?

- SoC == System On Chip
- ARM does not manufacture processor
- SoC vendor buys IP from ARM for the core
- Sometimes they also buy IP from other companies
- An SoC integrates a processor and peripherals

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Single Board Computer

- SBC = Single Board Computer
- Generaly from another company than the SoC one
- Integrates SoC and other chips (PMU, PHY etc ...)
- Also adds GPIOs, SD/MMC, ethernet connectors etc ...

Pine64 Rock64

- RK3328 based SBC
- 1Gbps Ethernet
- USB3
- eMMC socket
- ...
- Donated by Pine64, Thank you TL Lim

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- Porting to a new arch is hard, new SoC not that much

Bootloader requirement

- EFI aware

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- And it supports tftpboot
- andreast@FreeBSD.Org updated to recent u-boot

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- There is a good chance that the uart controller is already supported

First Boot

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- using a mfsroot can be handy

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- Each SoCs is different
- Most of the time Vendors reuse the clock models between SoCs

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Resets

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- Usually just a bit in one register

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- Right way is to use the clock api

Clock API

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- Clock driver registers clocks
- Driver can enable/disable/change frequency of clock in a SoCs independant way.
- Sadly no man pages

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- All SoCs specific clock needs to be created

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- *clknode_recalc* Refresh the cached value of the current clock frequency
- *clknode_setfreq* Change the frequency of the clock

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Clock API - Create a Clock Unit Driver

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- 3) Register the clknode with *clknode_register*
- Repeat 2 and 3 for every clock on the SoC and finalize the clock domain with *clkdom_finit*
- Use *clk_set_assigned* to parse the 'assigned-clock' properties

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assigned-clock example (1)

```
assigned-clocks =
<&cru DCLK_LCDC>, <&cru SCLK_PDM>,
<&cru SCLK_RTC32K>, <&cru SCLK_UART0>,
<&cru SCLK_UART1>, <&cru SCLK_UART2>,
<&cru ACLK_BUS_PRE>, <&cru ACLK_PERI_PRE>,
<&cru ACLK_VIO_PRE>, <&cru ACLK_RGA_PRE>,
<&cru ACLK_VOP_PRE>, <&cru ACLK_RKVDEC_PRE>,
<&cru ACLK_RKVENC>, <&cru ACLK_VPU_PRE>,
<&cru SCLK_VDEC_CABAC>, <&cru SCLK_VDEC_CORE>,
<&cru SCLK_VENC_CORE>, <&cru SCLK_VENC_DSP>,
<&cru SCLK_SDIO>, <&cru SCLK_TSP>,
<&cru SCLK_WIFI>, <&cru ARMCLK>,
<&cru PLL_GPLL>, <&cru PLL_CPLL>,
<&cru ACLK_BUS_PRE>, <&cru HCLK_BUS_PRE>,
<&cru PCLK_BUS_PRE>, <&cru ACLK_PERI_PRE>,
<&cru HCLK_PERI>, <&cru PCLK_PERI>,
<&cru SCLK_RTC32K>;
```

assigned-clock example (2)

```
assigned-clock-parents =
<&cru HDMIPHY>, <&cru PLL_APLL>,
<&cru PLL_GPLL>, <&xin24m>,
<&xin24m>, <&xin24m>;
assigned-clock-rates =
<0>, <61440000>,
<0>, <24000000>,
<24000000>, <24000000>,
<15000000>, <15000000>,
<100000000>, <100000000>,
<100000000>, <100000000>,
<50000000>, <100000000>,
<100000000>, <100000000>,
<50000000>, <50000000>,
<50000000>, <50000000>,
<24000000>, <600000000>,
<491520000>, <1200000000>,
<150000000>, <75000000>,
<75000000>, <150000000>,
<75000000>, <75000000>,
<32768>;
```

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- Register as a reset provider with hwreset_register_ofw_provider

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- Enable/Disable using *clk_enable,disable,stop*
- Set/Get frequency using *clk_set,get_freq*
- Free the clock using *clk_release*

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- Use the *hw.clock* sysctl

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- Starts we a few clocks - Mandatory PLLs, AHB clocks etc ... Also start with no set_freq method
- Use *clkdom_dump* after *clkdom_finit* under boot verbose
- Use the *hw.clock* sysctl
- Make sure that your clock is really working and that it is not a bootloader leftover

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  Some Vendor often use a common IP as a base
- Beware of docs, sometimes you need to read linux drivers ...

Questions ?

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