SonicVibes PCI Audio Accelerator

Preliminary

May 1997

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NOTATIONAL CONVENTIONS

The following notational conventions are used in this data book:

Signal names are shown in all uppercase letters. For example, XD.

A bar over a signal name indicates an active low signal. For example, $\overline{\text{OE}}$.

n-m indicates a bit field from bit n to bit m. For example, 7-0 specifies bits 7 through 0, inclusive.

n:m indicates a signal (pin) range from n to m. For example D[7:0] specifies data lines 7 through 0, inclusive

Use of a trailing letter H indicates a hexadecimal number. For example, 7AH is a hexadecimal number.

Use of a trailing letter b indicates a binary number. For example, 010b is a binary number.

When numerical modifiers such as K or M are used, they refer to binary rather than decimal form. Thus, for example, 1 KByte would be equivalent to 1024, not 1,000 bytes.

NOTICES

Additional information may be obtained from:

S3 Incorporated, Literature Department P.O. Box 58058, Santa Clara, CA 95052-8058.

Telephone: 408-588-8000, Fax: 408-980-5444

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Section 1: Introduction

Audio Card on a Chip™ Design

- Complete set of audio functions
- Single chip implementation

General Functions

- Sound Blaster Pro™ games compatibility
- S3FM™ games-compatible FM synthesis
- General MIDI synthesis
- Microsoft® DirectSound™ acceleration via high speed PCI bus
- Microsoft DirectMusic™ accelerator
- InfiniPatch™ downloadable samples using system RAM
- SRS™ 3D audio enhancement

Advanced Wavetable Synthesis

- 32 oscillators for General MIDI wavetable synthesis
- Channelized reverberation and chorus
- Hardware MIDI interpreter
- General MIDI compliant 1 & 2 MB FAT Labs™ sealed patchsets

Analog Features

- Single, true 16-bit ΣΔ stereo CODEC for reduced analog circuitry
- Sophisticated sample rate conversion for high quality digital mixing (patent pending)
- InfiniRate™ full-duplex operation with independent playback/record rate from 4 to 48 kHz
- Automuting after periods of digital silence
- Complex analog mixer for PCM, Wavetable, FM plus MIC and 4 stereo external analog sources exceeds MPC3 requirements

PCI System Interface

- Glueless master/slave PCI 2.1 for high performance PC audio system
- Distributed DMA support for hardware legacy support

Extensive User Hardware Interface

- 16 levels, speed compensated joystick timer and interface
- MPU-401 MIDI UART for external devices
- Hardware master volume control
- AUX1, AUX2, CD, Line In and MIC inputs
- Lineout to amplified speakers

Software Support

- Windows® 95 driver
- Windows NT™ driver
- DOS and Windows installation program
- DOS configuration utility and mixer applet
- 3rd party SonicVibes-enabled audio applications

QuickRamp™ Manufacturing Package

- Reference design schematics with BOM (soft and hard copies)
- Gerber files
- PADS® layout file
- Software drivers and applications
- Documentation

Single Crystal Operation at 24.576 MHz

Advanced Power Management 1.2 Compliance

160-pin PQFP or 176-pin TQFP Package

The single chip S3® SonicVibes™ audio accelerator is a PCI-tuned mixed signal audio signal processing accelerator for high integration, high quality PC product designs.

The single chip provides all the audio functions normally found on a sound card and provides them with higher quality. The bus master PCI interface ensures extremely low system overhead for audio data transfers, allowing use of system memory for storage of MIDI patchsets instead of a dedicated ROM. It also enables downloadable samples as expressed through Microsoft DirectMusic using system memory resources and S3's InfiniPatch technology. Real mode applications are supported through DDMA (Distributed DMA).

The high quality audio CODEC provides well integrated yet uncompromised 16-bit ΣΔ analog-to-digital and digital-to-analog conversions. The codec feeds a low distortion, complex mixer. The post-mixer

SRS stereo expansion and 3D surround simulation increase the high quality audio experience even on regular speakers.

All memory needed for data and program of digital signal processing is integrated within the chip. This and the other integrated features minimize the logic required for a complete audio solution.

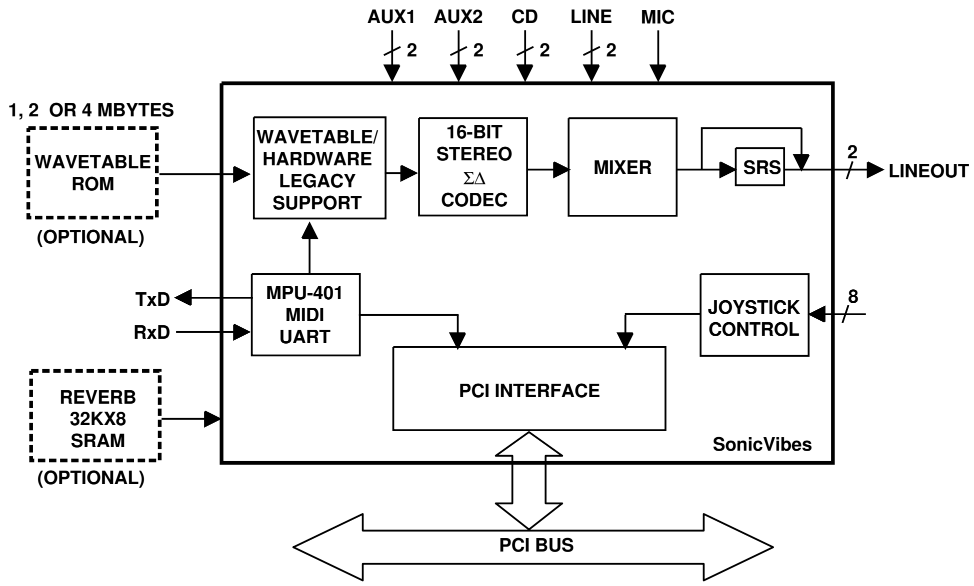

Figure 1-1. System Block Diagram

Section 2: Mechanical Data

2.1 THERMAL SPECIFICATIONS

Parameter	Min	Typ	Max	Unit
Thermal Resistance Θ_{JA} (Still Air) - 160 pin		24		°C/W
Thermal Resistance Θ_{JA} (Still Air) - 176 pin		27		°C/W
Junction Temperature			125	°C

2.2 MECHANICAL DIMENSIONS

The mechanical dimensions for the 160-pin PQFP package are given in Figure 2-1. Those for the 176-pin TQFP package are given in Figure 2-2.

Vendor-specific package mechanical drawings are provided with S3 qualification reports.

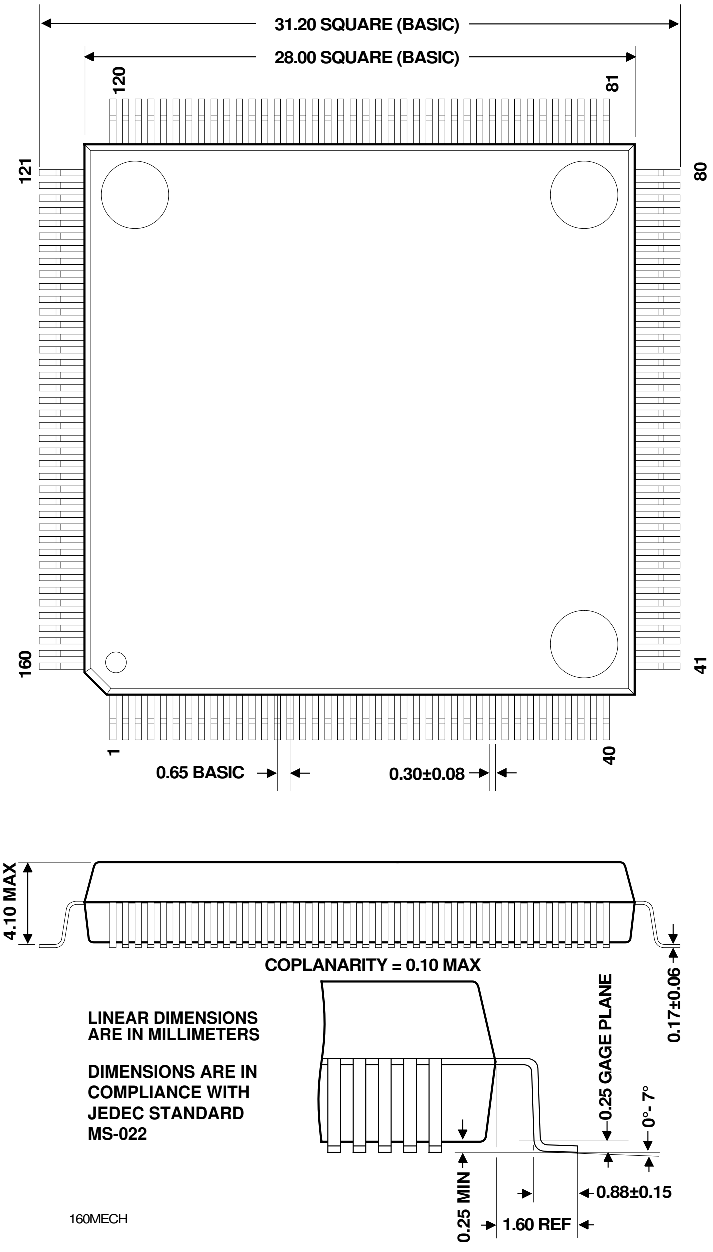

Figure 2-1. 160-pin PQFP Mechanical Dimensions

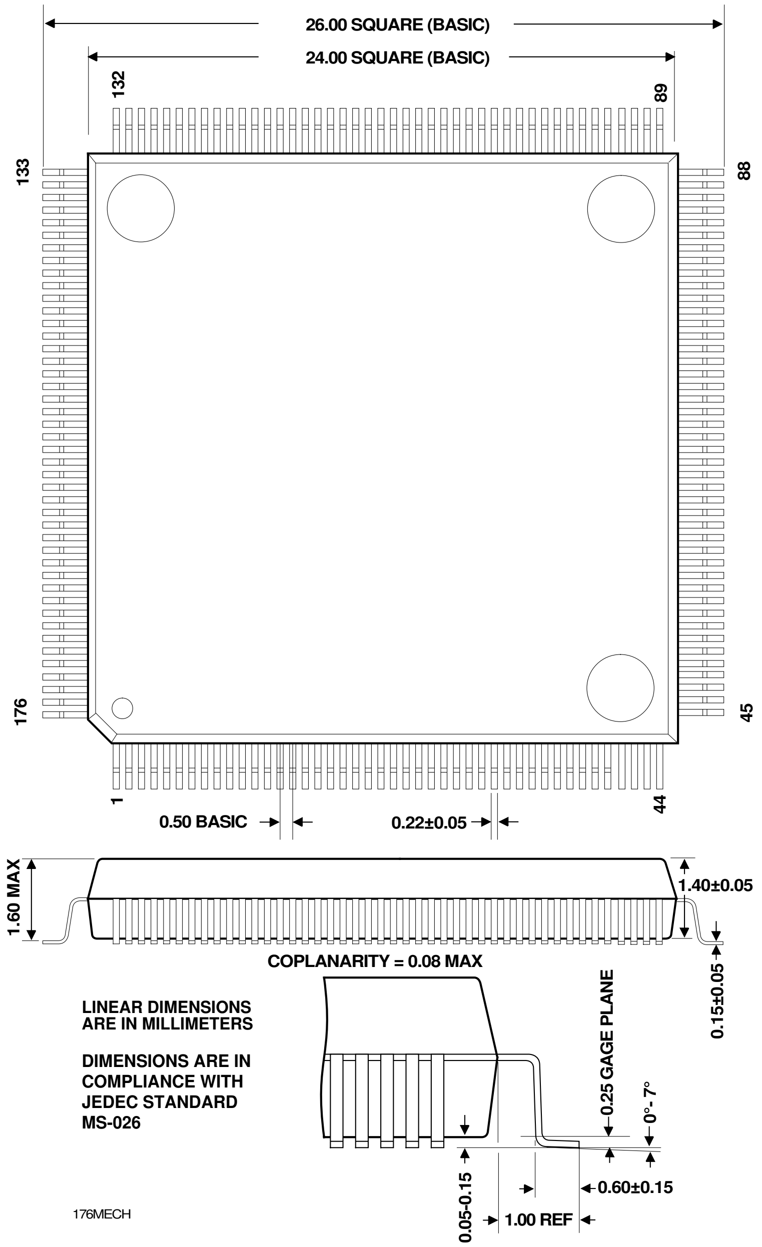

Figure 2-2. 176-pin TQFP Mechanical Dimensions

Section 3: Pins

3.1 PINOUT DIAGRAMS

The pinout for a 160-pin PQFP package is shown in Figure 3-1. The pinout for a 176-pin TQFP package is shown in Figure 3-2.

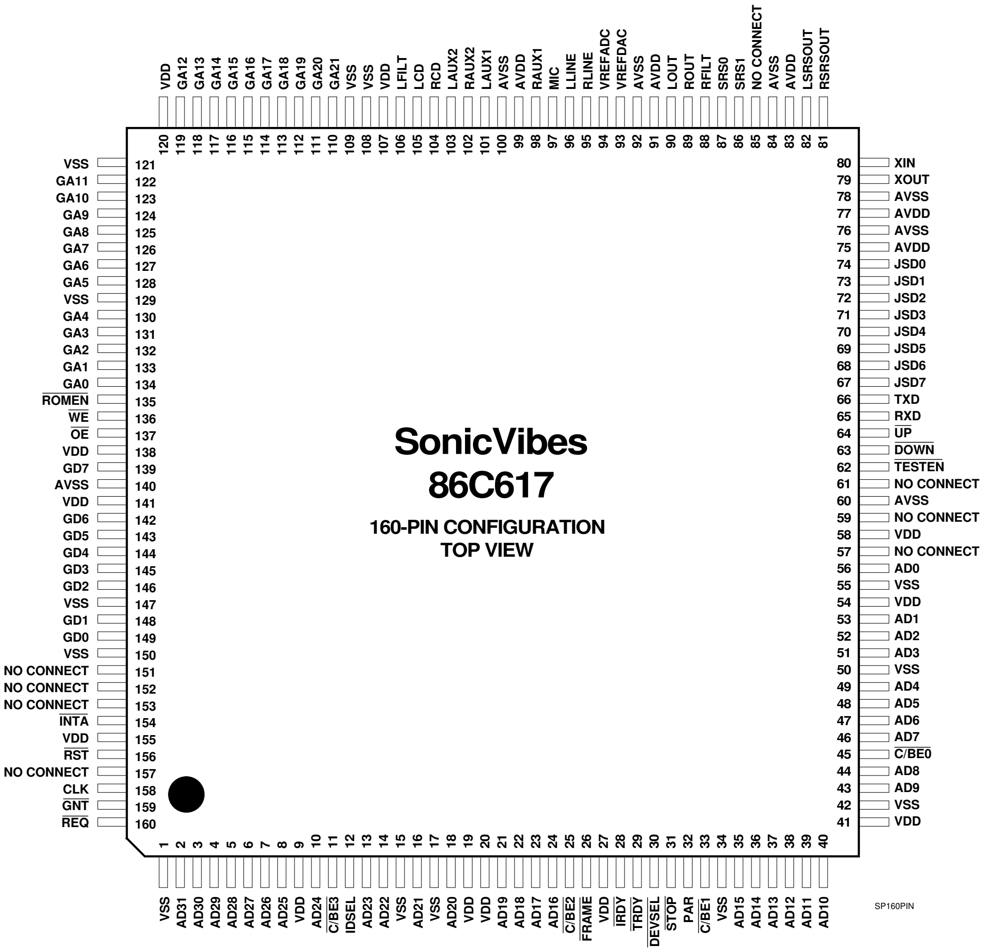

Figure 3-1. 160-pin Package Pinout

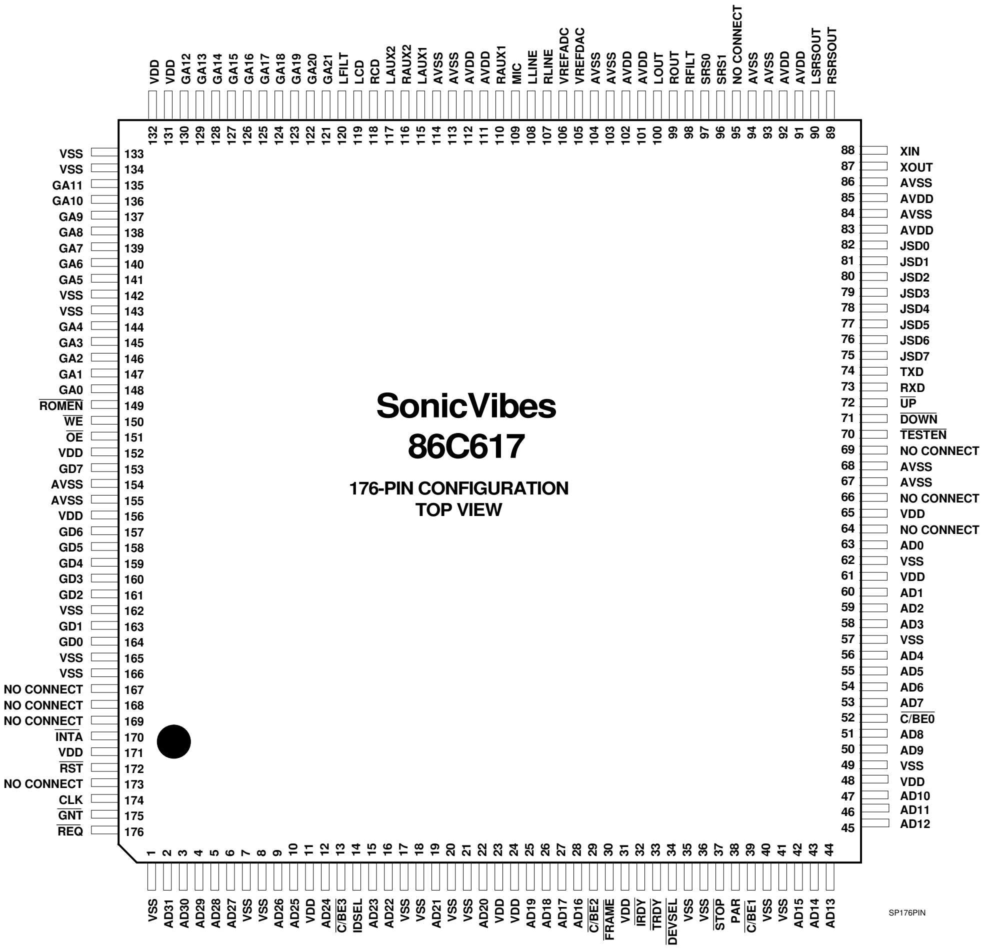

Figure 3-2. 176-pin Package Pinout

3.2 PIN DESCRIPTIONS

The following table provides a brief description of each pin on SonicVibes. The following abbreviations are used for pin types.

I - Input signal
O - Output signal
B - Bidirectional signal

Table 3-1. Pin Descriptions

Symbol	Type	Drive (mA)	Description
PCI BUS INTERFACE			
AD[31:0]	B	16/8	Multiplexed Address/Data Bus. A bus transaction (cycle) consists of an address phase followed by one or more data phases.
$\overline{\mathrm{C/BE}}$[3:0]	B	8	Bus Command/Data Byte Enables. These signals carry the bus command during the address phase and the byte enables during the data phase. These signals are outputs during bus master DMA operation.
CLK	I		PCI System Clock.
$\overline{\mathrm{INTA}}$	O		PCI Interrupt Request.
$\overline{\mathrm{IRDY}}$	B	8	Initiator Ready. This signal is an output during bus master DMA operation and an input when the SonicVibes operates as a slave.
$\overline{\mathrm{TRDY}}$	B	8	Target Ready. This signal is an input during bus master DMA operation and an output when the SonicVibes operates as a slave.
$\overline{\mathrm{DEVSEL}}$	B	8	Device Select. SonicVibes drives this signal active when it decodes its address as the target of the current access. This signal is an input during bus master DMA operation.
IDSEL	I		Initialization Device Select. This input is the chip select for PCI configuration register reads/writes.
$\overline{\mathrm{RST}}$	I		System Reset. Asserting this signal forces the registers and state machines to a known state. (200k pull-up)
$\overline{\mathrm{FRAME}}$	B	8	Cycle Frame. This signal is asserted by the bus master to indicate the beginning of a bus transaction. It is deasserted during the final data phase of a bus transaction. This signal is an output during bus master DMA operation.
PAR	B	8	Parity. SonicVibes asserts this signal to verify even parity during reads. This signal is an input during bus master DMA operation.
$\overline{\mathrm{STOP}}$	B	8	Stop. SonicVibes asserts this signal to indicate a target disconnect. This signal is an input during bus master DMA operation.
$\overline{\mathrm{REQ}}$	O	16/8	Request. SonicVibes asserts this signal to request control of the PCI bus for bus master DMA operation.
$\overline{\mathrm{GNT}}$	I		Grant. When active, this signal indicates that SonicVibes has control of the PCI bus for bus master DMA operation.

Table 3-1. Pin Descriptions (continued)

Symbol	Type	Drive (mA)	Description
WAVETABLE ROM AND SRAM INTERFACE			
GA[21:0]	O	8	ROM/SRAM Address Bus. (200k pull-ups on GA[21:19])
GD[7:0]	B	8	ROM/SRAM Data Bus. (200k pull-ups on GD[7:0])
$\overline{\text{WE}}$	O	8	SRAM Write Enable.
$\overline{\text{OE}}$	O	8	SRAM Output Enable.
$\overline{\text{ROMEN}}$	O	8	ROM Address Enable.
JOYSTICK AND MIDI INTERFACE			
JSD[7:0]	I		Joystick Inputs. (200k pull-ups on JSD[7:4])
RXD	I		MPU-401 UART Receive Data.
TXD	O	8	MPU-401 UART Transmit Data.
MISCELLANEOUS INTERFACES			
XIN			Reference Frequency Input. If an external crystal is used, it is connected between XOUT and this pin. A stable external frequency source can also be input via this pin.
XOUT			Crystal Output. If an external 24.576 MHz crystal is used, it is connected between XIN and this pin. This pin drives the crystal via an internal oscillator.
VREFADC	O		Voltage Reference Bypass for ADC.
VREFDAC	O		Voltage Reference Bypass for DAC.
$\overline{\text{UP}}$	I		Increase Audio Volume Input.
$\overline{\text{DOWN}}$	I		Decrease Audio Volume Input.
SRS[1:0]	I		SRS Control.
$\overline{\text{TESTEN}}$	I		Test Enable. Used for S3 testing. This pin must never be grounded in operational use. (200k pull-up)

Table 3-1. Pin Descriptions (continued)

Symbol	Type	Drive (mA)	Description
AUDIO INTERFACE			
LOUT	O		Left Channel Audio Output.
ROUT	O		Right Channel Audio Output.
LSRSOUT	O		Left Channel SRS Output.
RSRSOUT	O		Right Channel SRS Output.
LAUX[1:2]	I		Left Channel Auxillary Inputs.
RAUX[1:2]	I		Right Channel Auxillary Inputs.
LCD	I		Left Channel CD Input.
RCD	I		Right Channel CD Input.
LLINE	I		Left Channel Line Input.
RLINE	I		Right Channel Line Input.
LFILT	O		Left Channel ADC Anti-aliasing Filter.
RFILT	O		Right Channel ADC Anti-aliasing Filter.
MIC	I		Mono Microphone Input.
POWER AND GROUND			
VDD			5V Digital Power
VSS			Digital Ground
AVDD			5V Analog Power
AVSS			Analog Ground

3.3 PIN LISTS

Table 3-2 lists all pins alphabetically. The pin number(s) corresponding to each package type are given in the appropriate column. Table 3-3 lists all pins in numerical order. The corresponding pin name/pin number is given in the appropriate package type column.

Table 3-2. Alphabetical Pin Listing

	PIN(S)	
Name	**160-pin Package**	**176-pin Package**
AD[31:0]	2-8,10,13,14,16,18,21-24,35-40,43,44,	2-6,9,10,12,15,16,19,22,25-28,42-47,
	46-49,51-53,56	50,51,53-56,58-60,63
AVDD	75,77,83,91,99	83,85,91,92,101,102,111,112
AVSS	60,76,78,84,92,100,140	67,68,84,86,93,94,103,104,113,114,
		154,155
C/BE[3:0]	11,25,33,45	13, 29,39,52
CLK	158	174
DEVSEL	30	34
DOWN	63	71
FRAME	26	30
GA[21:0]	110-119,122-128,130-134	121-130,135-141,144-148
GD[7:0]	139,142-146,148,149	153,157-161,163,164
GNT	159	175
IDSEL	12	14
INTA	154	170
IRDY	28	32
JSD[7:0]	67-74	75-82
LAUX[1:2]	101,103	115,117
LCD	105	119
LFILT	106	120
LLINE	96	108
LOUT	90	100
LSRSOUT	82	90
MIC	97	109
NO CONNECT	57,59,61,85, 151,153,157	64,66,69,95,167-169,173
OE	137	151
PAR	32	38
RAUX[1:2]	98,102	110,116
RCD	104	118
REQ	160	176
RFILT	88	98
RLINE	95	107
ROMEN	135	149
ROUT	89	99
RSRSOUT	81	89
RST	156	172
RXD	65	73

Table 3-2. Alphabetical Pin Listing (Continued)

	PIN(S)	
Name	**160-pin Package**	**176-pin Package**
SRS[1:0]	86-87	96-97
$\overline{\text{STOP}}$	31	37
$\overline{\text{TESTEN}}$	62	70
$\overline{\text{TRDY}}$	29	33
TXD	66	74
$\overline{\text{UP}}$	64	72
VDD	9,19,20,27,41,54,58,107,120,138,	11,23,24,31,48,61,65,131,132,152,156,171
	141,155	
VREFADC	94	106
VREFDAC	93	105
VSS	1,15,17,34,42,50,55,108,109,121,	1,7,8,17,18,20,21,35,36,40,41,49,57,
	129,147,150	62,133,134,142,143,162,165,166
$\overline{\text{WE}}$	136	150
XIN	80	88
XOUT	79	87

Table 3-3. Numerical Pin Listing

	Name	
Number	**160-pin Package**	**176-pin Package**
1	VSS	VSS
2	AD31	AD31
3	AD30	AD30
4	AD29	AD29
5	AD28	AD28
6	AD27	AD27
7	AD26	VSS
8	AD25	VSS
9	VDD	AD26
10	AD24	AD25
11	$\overline{\text{C/BE3}}$	VDD
12	IDSEL	AD24
13	AD23	$\overline{\text{C/BE3}}$
14	AD22	IDSEL
15	VSS	AD23
16	AD21	AD22
17	VSS	VSS
18	AD20	VSS
19	VDD	AD21
20	VDD	VSS
21	AD19	VSS
22	AD18	AD20
23	AD17	VDD
24	AD16	VDD
25	$\overline{\text{C/BE2}}$	AD19
26	$\overline{\text{FRAME}}$	AD18
27	VDD	AD17
28	$\overline{\text{IRDY}}$	AD16
29	$\overline{\text{TRDY}}$	$\overline{\text{C/BE2}}$
30	$\overline{\text{DEVSEL}}$	$\overline{\text{FRAME}}$
31	$\overline{\text{STOP}}$	VDD
32	PAR	$\overline{\text{IRDY}}$
33	$\overline{\text{C/BE1}}$	$\overline{\text{TRDY}}$
34	VSS	$\overline{\text{DEVSEL}}$
35	AD15	VSS
36	AD14	VSS
37	AD13	$\overline{\text{STOP}}$
38	AD12	PAR
39	AD11	$\overline{\text{C/BE1}}$
40	AD10	VSS
41	VDD	VSS
42	VSS	AD15

Table 3-3. Numerical Pin Listing (Continued)

	Name	
Number	**160-pin Package**	**176-pin Package**
43	AD9	AD14
44	AD8	AD13
45	$\overline{\text{C/BE0}}$	AD12
46	AD7	AD11
47	AD6	AD10
48	AD5	VDD
49	AD4	VSS
50	VSS	AD9
51	AD3	AD8
52	AD2	$\overline{\text{C/BE0}}$
53	AD1	AD7
54	VDD	AD6
55	VSS	AD5
56	AD0	AD4
57	NO CONNECT	VSS
58	VDD	AD3
59	NO CONNECT	AD2
60	AVSS	AD1
61	NO CONNECT	VDD
62	$\overline{\text{TESTEN}}$	VSS
63	$\overline{\text{DOWN}}$	AD0
64	$\overline{\text{UP}}$	NO CONNECT
65	RXD	VDD
66	TXD	NO CONNECT
67	JSD7	AVSS
68	JSD6	AVSS
69	JSD5	NO CONNECT
70	JSD4	$\overline{\text{TESTEN}}$
71	JSD3	$\overline{\text{DOWN}}$
72	JSD2	$\overline{\text{UP}}$
73	JSD1	RXD
74	JSD0	TXD
75	AVDD	JSD7
76	AVSS	JSD6
77	AVDD	JSD5
78	AVSS	JSD4
79	XOUT	JSD3
80	XIN	JSD2
81	RSRSOUT	JSD1
82	LSRSOUT	JSD0
83	AVDD	AVDD
84	AVSS	AVSS

Table 3-3. Numerical Pin Listing (Continued)

	Name	
Number	**160-pin Package**	**176-pin Package**
85	NO CONNECT	AVDD
86	SRS1	AVSS
87	SRS0	XOUT
88	RFILTER	XIN
89	ROUT	RSRSOUT
90	LOUT	LSRSOUT
91	AVDD	AVDD
92	AVSS	AVDD
93	VREFDAC	AVSS
94	VREFADC	AVSS
95	RLINE	NO CONNECT
96	LLINE	SRS1
97	MIC	SRS0
98	RAUX1	RFILT
99	AVDD	ROUT
100	AVSS	LOUT
101	LAUX1	AVDD
102	RAUX2	AVDD
103	LAUX2	AVSS
104	RCD	AVSS
105	LCD	VREFDAC
106	LFILTER	VREFADC
107	VDD	RLINE
108	VSS	LLINE
109	VSS	MIC
110	GA21	RAUX1
111	GA20	AVDD
112	GA19	AVDD
113	GA18	AVSS
114	GA17	AVSS
115	GA16	LAUX1
116	GA15	RAUX2
117	GA14	LAUX2
118	GA13	RCD
119	GA12	LCD
120	VDD	LFILT
121	VSS	GA21
122	GA11	GA20
123	GA10	GA19
124	GA9	GA18
125	GA8	GA17
126	GA7	GA16

Table 3-3. Numerical Pin Listing (Continued)

	Name	
Number	**160-pin Package**	**176-pin Package**
127	GA6	GA15
128	GA5	GA14
129	VSS	GA13
130	GA4	GA12
131	GA3	VDD
132	GA2	VDD
133	GA1	VSS
134	GA0	VSS
135	$\overline{\text{ROMEN}}$	GA11
136	$\overline{\text{WE}}$	GA10
137	$\overline{\text{OE}}$	GA9
138	VDD	GA8
139	GD7	GA7
140	AVSS	GA6
141	VDD	GA5
142	GD6	VSS
143	GD5	VSS
144	GD4	GA4
145	GD3	GA3
146	GD2	GA2
147	VSS	GA1
148	GD1	GA0
149	GD0	ROMEN
150	VSS	WE
151	NO CONNECT	$\overline{\text{OE}}$
152	NO CONNECT	VDD
153	NO CONNECT	GD7
154	$\overline{\text{INTA}}$	AVSS
155	VDD	AVSS
156	$\overline{\text{RST}}$	VDD
157	NO CONNECT	GD6
158	CLK	GD5
159	$\overline{\text{GNT}}$	GD4
160	$\overline{\text{REQ}}$	GD3
161	N/A	GD2
162	N/A	VSS
163	N/A	GD1
164	N/A	GD0
165	N/A	VSS
166	N/A	VSS
167	N/A	NO CONNECT

Table 3-3. Numerical Pin Listing (Continued)

	Name	
Number	**160-pin Package**	**176-pin Package**
168	N/A	NO CONNECT
169	N/A	NO CONNECT
170	N/A	$\overline{\text{INTA}}$
171	N/A	VDD
172	N/A	$\overline{\text{RST}}$
173	N/A	NO CONNECT
174	N/A	CLK
175	N/A	$\overline{\text{GNT}}$
176	N/A	$\overline{\text{REQ}}$

Section 4: Electrical Characteristics

4.1 MAXIMUM RATINGS

Table 4-1. Maximum Ratings

Ambient Temperature	-40° C to 85° C
Storage Temperature	-65° C to 150° C
Operating Temperature	0° C to 70° C
DC Supply Voltage (analog and digital)	7.0 V
I/O Pin Voltage	GND - 0.5 V to VDD + 0.5 V
Power Dissipation	2 W

Warning: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

4.2 POWER DISSIPATION

Table 4-2. Operational Power Dissipation

Parameter	Typ	Unit	Note
Power dissipation (analog and digital)	1.5	W	All features turned on

4.3 DC CHARACTERISTICS

Conditions: 5V ± 5%, full-scale output sine wave at 1 kHz, resistive loading = 10 kΩ

Table 4-3. Analog Input DC Characteristics

Parameter	Min	Typ	Max	Unit
ADC Information				
Resolution		16 bits		
Maximum Accuracy				
Integral Linearity Error		± 1 LSB		
Differential Linearity Error		± 1 LSB		
Monotonicity		Guaranteed		
VREFADC	2.0	2.2	2.4	V
Analog Input Capacitance			15	pF
Input Offset Error			100	LSB

Table 4-4. Analog Output DC Characteristics

Parameter	Min	Typ	Max	Unit
DAC Information				
Resolution		16 bits		
Maximum Accuracy				
Integral Linearity Error		± 1 LSB		
Differential Linearity Error		± 1 LSB		
Monotonicity		Guaranteed		
Power Supply Current (measured at pin)		10		mA
VREFDAC	2.0	2.2	2.4	V
Output Offset Voltage		20		mV
Power Supply Rejection Ratio on AVDD		40		dB

Table 4-5. Digital DC Characteristics (Operating at RoomTemperature)

Symbol	Parameter	Min	Typ.	Max	Unit	Notes
VIL	Supply Low Voltage	- 0.5		0.8	V	
VIH	Supply High Voltage	2.0		VDD+0.5	V	
IIN	Supply Leakage Current	-10		10	µA	@VI = VDD or VSS
VOL	Output Low Voltage			0.4	V	@rated output current
VOH	Output High Voltage				V	@rated output current
IOL	Output Low Current				mA	1
IOH	Output High Current				mA	2
IDD	Digital Power Supply Current				mA	fs = 48 kHz, 1k Hz sine wave
CIN	Input Capacitance			7	pF	

1. The IOL values (drives) for outputs are given in Table 3-1.

2.The IOH value for each output = -(IOL/2).

4.4 AC CHARACTERISTICS

Conditions: 5V ± 5%, full-scale output sine wave at 1 kHz, resistive loading = 10 kΩ, bandwidth 20 Hz to 20 kHz.

Table 4-6. Analog Input AC Characteristics

Parameter	Min	Typ	Max	Unit
Signal to Noise Ratio		85		dB
Dynamic Range	80	85		dB
Total Harmonic Distortion (THD)		0.02		%
Interchannel Isolation		80		dB
Interchannel Gain Mismatch			1	dB
Gain Step Size	1.3	1.5	1.7	dB
Full-scale Input Voltage	2.5	2.8	3.1	VPP
Input Resistance	20			kΩ
Input Capacitance			15	pF

Table 4-7. Analog Output AC Characteristics

Parameter	Min	Typ	Max	Unit
Signal to Noise Ratio		85		dB
Dynamic Range	80	85		dB
Total Harmonic Distortion (THD)		0.02		%
Interchannel Isolation		80		dB
Interchannel Gain Mismatch			1	dB
Attenuation Step Size	1.3	1.5	1.7	dB
Mute Attenuation	80			dB
Frequency Response		± 0.5		dB
Full-scale Output Voltage	2.5	2.8	3.1	VPP
Out of Band Energy (22 kHz to 100 kHz)			-45	dB
Capacitive Load			100	pF
Output Load Resistance	10			kΩ

Table 4-8. Digital AC Characteristics

Parameter	Min	Typ	Max	Unit
Crystal Frequency (Default = 24.576 MHz)	-0.01		0.01	%
Input Clock Frequency (XIN)	24	24.576	25	MHz
Input Clock Duty Cycle (XIN)	40	50	60	%
Frequency Change Lock Time			500	µs
Cycle to Cycle Jitter		100	250	ps
Group Delay (ADC)		23/fs		s
Group Delay (DAC)		31/fs		s

4.5 AC TIMING

4.5.1 Clock Waveform Timing

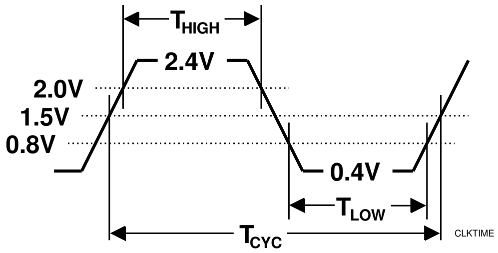

Figure 4-1. Clock Waveform Timing

Table 4-9. Clock Waveform Timing

Symbol	Parameter	Min	Typ	Max	Units	Notes
T_{CYC}	CLK Cycle Time	20		125	ns	
T_{HIGH}	CLK High Time	8		80	ns	
T_{LOW}	CLK Low Time	8		80	ns	
	CLK Slew Rate	1		4	V/ns	

4.5.2 Input Timing

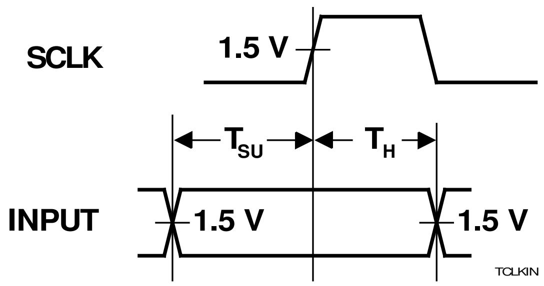

Figure 4-2. Input Timing

Table 4-10. CLK-Referenced Input Timing

PCI Bus			
Symbol	**Parameter**	**Min**	**Units**
T_{SU}	AD[31:0], $\overline{\text{C/BE}}$[3:0], $\overline{\text{FRAME}}$, $\overline{\text{IRDY}}$, IDSEL setup	7	ns
T_H	AD[31:0] hold	1	ns
T_H	$\overline{\text{C/BE}}$[3:0], $\overline{\text{FRAME}}$, $\overline{\text{IRDY}}$, IDSEL hold	1	ns
T_{SU}	$\overline{\text{GNT}}$ setup	10	ns
T_H	$\overline{\text{GNT}}$ hold	0	ns

4.5.3 Output Timing

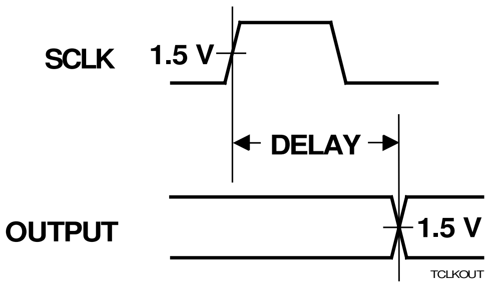

Figure 4-3. Output Timing

The minimum delay is the minimum time after the clock edge that the valid signal state from the previous cycle will begin transition to the next state (become invalid).

The maximum delay is the maximum time after the clock edge that the signal state is valid for the next cycle.

All output delays are based on an 80 pF test load.

Table 4-11. CLK-Referenced Output Timing

PCI Bus				
Parameter	**Min**	**Max**	**Units**	**Notes**
AD[31:0] valid delay	2	16	ns	1
$\overline{\text{DEVSEL}}$, PAR delay	2	11	ns	2
$\overline{\text{STOP}}$ delay	2	11	ns	
$\overline{\text{TRDY}}$ delay	2	11	ns	
$\overline{\text{INTA}}$ delay	2	11	ns	
$\overline{\text{REQ}}$ delay	2	10	ns	

Note

1. Due to the timing for $\overline{\text{TRDY}}$ for read cycles, data is not sampled on the clock edge immediately following its becoming valid. This guarantees the PCI 2.1 specification time of 11 ns.
2. Medium $\overline{\text{DEVSEL}}$ timing used.

Section 5: Hardware Interfaces

SonicVibes provides a PCI bus interface and also has several optional memory type interfaces.

5.1 POWER-ON STRAPPING

Certain functions are selected/configured at power-on reset via external strapping of designated pins. Each of the pins that functions in this manner has an internal 200 kΩ (typical) pull-up resistor. Therefore, if the desired result is obtained from a logic 1 being present on a pin during reset, no external pull-up resistor is required. If the desired result require that a logic 0 be present on a pin during reset, this requires a 10 kΩ resistor tied to ground.

Table 5-1. Power-on Strapping Settings

Pin #	Register Bit Where Latched	Description
111	CM00_2	Reverb Enable 0 = Reverb function enabled 1 = Reverb function disabled Enabling the reverb function requires that external SRAM is connected.
146, 148, 149	N/A	External Wavetable ROM Wait State Control Pin 146 is MSB, Pin 149 is LSB 101 = 5 wait states (100 ns ROM) 110 = 6 wait states (120 ns ROM) 111 = 7 wait states (150 ns ROM) - Default - leave floating Attach 10kΩ pull-down to appropriate pin for 0 value.
142	N/A	External SRAM Wait State Control 0 = No wait state (10 ns SRAM) - requires 10kΩ pull-down 1 = 1 wait state (12 - 25 ns SRAM) - Default - leave floating
112	CMX2E_0 (with reversed polarity from strap)	Wavetable Sample Source Select (register value) 0 = Use on-board ROM 1 = Use PCI bus (system memory)

5.2 PCI BUS INTERFACE

SonicVibes provides a complete bus master PCI interface. The pinout and other specifications are in conformance with Revision 2.1 of the PCI specification. No glue logic is required.

5.2.1 PCI Configuration

The Vendor ID register (Index 00H) in the PCI Configuration space is hardwired to 5333H to specify S3 Incorporated as the vendor. The Device ID register is hardwired to CA00H. The Revision ID will vary by stepping. Subvendor ID is implemented. The information must be stored in the wavetable ROM (if available) or in the BIOS for motherboard implementations. The BIOS is responsible for writing the subvendor ID information to PCI2C during initialization.

Bits 10-9 of the Status register (Index 06H) are hardwired to 01b to specify medium $\overline{\text{DEVSEL}}$ timing. The Class Code register (Index 08H) is hardwired to 040100xxH to specify that the SonicVibes is a multimedia audio device. There are 5 Base Address registers corresponding to the 5 logic devices defined for ISA PnP. Bit 0 of each register is hardwired to 1 to indicate that the register resides in I/O space and responds only to I/O accesses (no MMIO).

5.2.2 PCI External Memory Interfaces

For PCI configurations, SonicVibes provides complete interfaces to two types of optional external memory:

- Wavetable ROM
- SRAM (reverb support)

5.2.2.1 ROM Interface

SonicVibes supports up to 4 external ROM chips for storage and retrieval of wavetable data. The maximum memory size is 2 MBytes for 512Kx8 ROMs and 4 MBytes for 1Mx8, 2Mx8 or 4Mx8 ROMs. Normally, wavetable data is stored in system memory for PCI configurations and external ROM is not used. If it is, CMX2E_0 = 0 selects ROM as the wavetable data source, with CMX2E_0 = 1 selecting the PCI bus as the source. This selection can be made via power-on strapping of pin 112. The state of this pin during reset is latched in CMX2E_30 and can be reprogrammed after reset. With external ROM present, CMX2E_1 can be set to 1 to enable both the ROM and the PCI bus to be wavetable data sources. A diagram of the ROM interface for 1 chip is shown in Figure 5-1. A two chip configuration is shown in Figure 5-2.

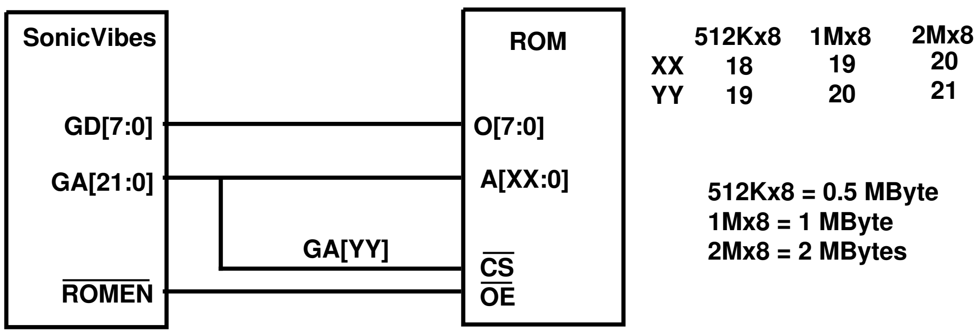

Figure 5-1. Single Chip ROM Configurations

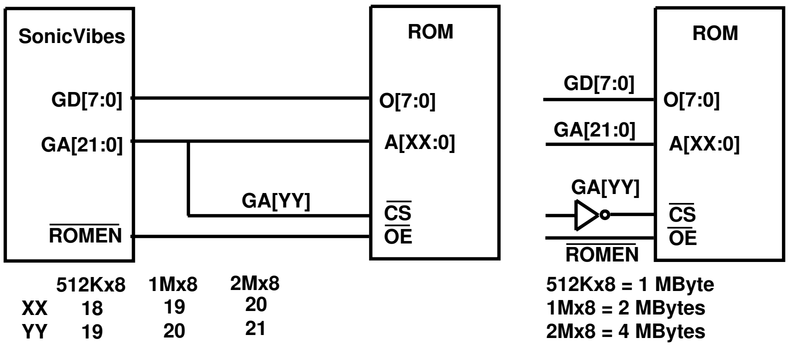

Figure 5-2. Two Chip ROM Configurations

Figure 5-3 shows the timing for this interface. The clock is internal and is generated by the synthesizer PLL. The number of wait states is defined by power-on strapping of GD[2:0]. Since these pins have internal pull-ups, the default is 7, resulting in 8 wait states. (Wait states = strapping value + 1). The appropriate number of wait states depends on the speed of the ROM chosen.

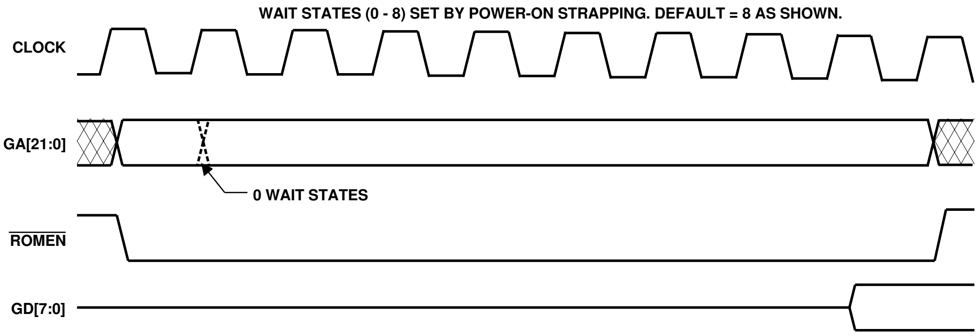

Figure 5-3. ROM Read Functional Timing

5.2.2.2 SRAM Interface

SonicVibes supports one external 32Kx8 SRAM to provide reverb capability during wavetable synthesis. This interface is shown in Figure 5-4. If SRAM is connected, pin 111 must be pulled down by an external resistor during reset to enable the SRAM interface. The state of this pin during reset is latched in CM00_2. The reverb function is controlled through system exclusive MIDI commands. This is described in a separate document.

Figure 5-5 shows the read timing for this interface and Figure 5-6 shows the write timing. The clock is internal and is generated by the synthesizer PLL. The number of wait states is defined by power-on

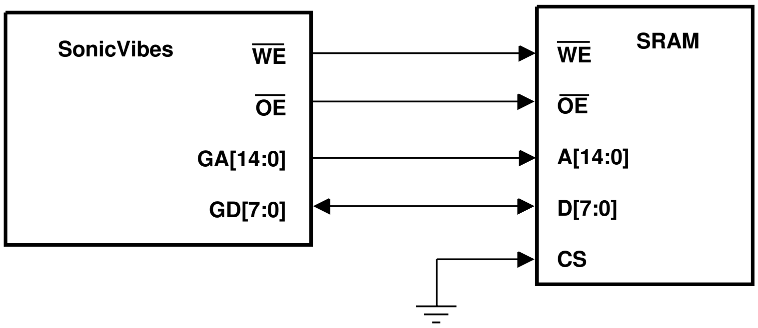

Figure 5-4. SRAM Interface

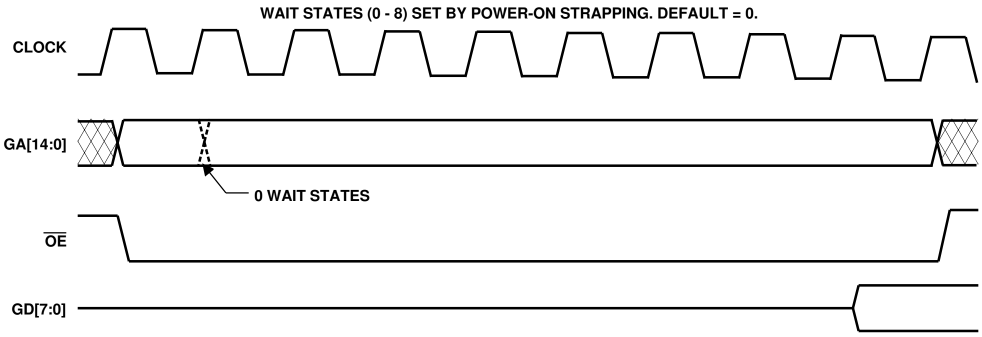

Figure 5-5. SRAM Read Functional Timing

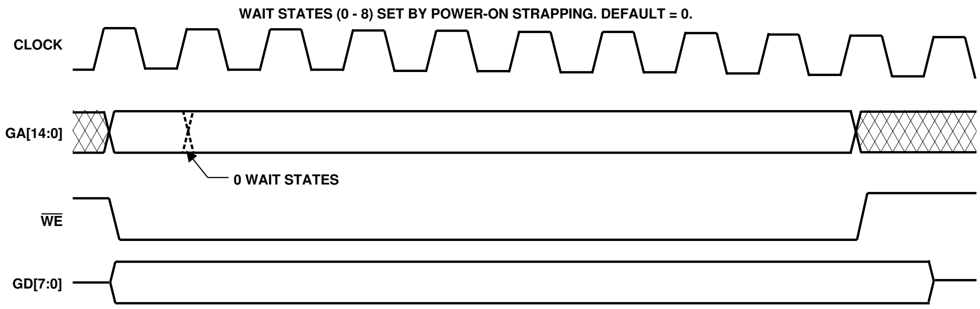

Figure 5-6. SRAM Write Functional Timing

strapping of GD[6:3]. Since these pins have internal pull-ups, the default is FH. This results in 0 wait states. If GD6 is pulled down at reset, the number of wait states = GD[5:3] value + 1). The range is thus from 1 to 8. The appropriate number of wait states depends on the speed of the SRAM chosen.

5.2.3 Distributed DMA Support

SonicVibes supports distributed DMA (DDMA) to provide support for legacy audio applications. This support requires that the SonicVibes be located on the PCI system motherboard with core logic and a system BIOS that supports DDMA.

DDMA is supported for the playback DMA channel (DMA_A) used by games compatible software. PCI40 provides the channel enable and configuration information for this support. The following 8237-compatible DMA registers are provided for this channel.

Table 5-2. Compatible DMA Registers for DMA_A

Offset From Base	Type	Description
00	W/R	Base/Current address (7-0)
01	W/R	Base/Current address (15-8)
02	W/R	Base/Current address (23-16)
03	W/R	Base/Current address (31-24)
04	W/R	Base/Current byte count (7-0)
05	W/R	Base/Current byte count (15-8)
06	W/R	Base/Current byte count (23-16)
08	W/R	Command/Status (bits 7-4, Channel Request - return 0000 or 1111; bits 3-0, Channel terminal count - return 0000 or 1111)
09		Reserved
0B	W	Bits 3-2 - 01 = IOR, 10 = IOW Bits 4 - 0 = auto init disabled, 1 = auto init enabled
0D	W	Master clear
0F	W	Bit 0 - 0 = Clear mask bit, 1 = Set mask bit

In game compatible mode, only DMA_A is used. In enhance mode, DMA_A is used for playback and DMA_C is used for record. The latter is a 16-bit channel. It is handled in a manner similar to DMA_A except that since it has no legacy support functions, the compatible DMA register requirements are reduced. PCI48 provides the channel enable and I/O base address. The channel registers are given in the following table.

Table 5-3. Compatible DMA Registers for DMA_C

Offset From Base	Type	Description
00	W/R	Base/Current address (7-0)
01	W/R	Base/Current address (15-8)
02	W/R	Base/Current address (23-16)
03	W/R	Base/Current address (31-24)
04	W/R	Base/Current word count (7-0)
05	W/R	Base/Current word count (15-8)
06	W/R	Base/Current word count (23-16)
0B	W	Bits 3-2 - 01 = IOR, 10 = IOW Bits 4 - 0 = auto init disabled, 1 = auto init enabled
0D	W	Master clear

5.2.4 PCI PnP Issues

Most legacy software expects to find the games compatible registers, the MIDI UART registers and the game port registers each at a fixed I/O address. Therefore, the system BIOS needs to be aware of this requirement and always assign the following base addresses during its Plug and Play routine.

Games Compatible (PCI10) - 220H
FM Synthesis (PCI18) - 388H
MIDI UART (PCI1C) - 330H
Game Port (PCI20) - 200H

The enhanced registers (PCI14) can be relocated anywhere in I/O space if legacy support is not a consideration.

5.3 AUDIO CONTROL INTERFACES

This section describes the analog audio control interfaces, the hardware master volume control interface, the MIDI UART interface and the joystick interface (game port). See Figure 5-7. The electrical specifications for these interfaces are provided in Section 4.

5.3.1 Analog Audio Control Interfaces

Table 5-4 lists the analog audio control interfaces.

Table 5-4. Analog Audio Control Interfaces

Pin #	Pin Name	Description
101, 103	LAUX[1:2]	Left channel auxiliary analog inputs 1 and 2
98, 102	RAUX[1:2]	Right channel auxiliary analog inputs 1 and 2
96	LLINE	Left line analog input
95	RLINE	Right line analog input
105	LCD	Left CD analog input
104	RCD	Right CD analog input
97	MIC	Microphone mono analog input
90	LOUT	Left channel analog output
89	ROUT	Right channel analog output
82	LSRSOUT	Left channel SRS 3D enhanced analog output
81	RSRSOUT	Right channel SRS 3D enhanced analog output

5.3.2 Hardware Master Volume Control Interface (Up/Down Button Support)

The output volume is indirectly controlled by software based on the input states of the digital $\overline{\text{UP}}$ and $\overline{\text{DOWN}}$ inputs. These inputs will typically be connected to end-user controlled up and down volume buttons in such a way that they are driven low when the corresponding button is pressed. When one of these inputs is asserted, an interrupt is generated unless it is masked via CM01_6. The interrupt status is reported by CM02_6. For each 0.1 second the pin is asserted, a counter is incremented. The value of this counter reported in CMX14_5-0. CMX14_6 reports whether the $\overline{\text{UP}}$ (= 1) or $\overline{\text{DOWN}}$ (= 0) pin was asserted. If both pins are asserted, this requests muting and is indicated by CMX14_7 = 1. The interrupt service routine reads CMX14 and uses this information to program CMX10 and CMX11 to change the output volume appropriately.

5.3.3 MPU-401-COMPATIBLE MIDI UART Interface

This interface is compatible with the MPU-401 standard. It takes serial MIDI input on the RXD pin, converts it to 8-bit parallel data and stores it in a 16-deep FIFO for retrieval by the host. If also stores 8-bit data from the host in an 8-deep FIFO and converts it to serial data for output on the TXD pin. The interface operates at a fixed 31.25 kbs.

5.3.3.1 MIDI UART Registers

The base address for these registers is that defined by the MIDI Base Address register.

Table 5-5. MIDI UART Registers

Address (Hex)	Description
Base + 0	MIDI UART Data (R/W)
Base + 1	MIDI UART Command (W), Status (R)

MIDI UART Data Register

Read/Write Address: Base + 0H
Power-On Default: 00H

7	6	5	4	3	2	1	0
DATA [7:0]							

Bits 7–0 DATA [7:0]

Value = MIDI data written to the FIFO or to be read from the FIFO or status information generated by the previous command

MIDI UART Status

Read Only Address: Base + 1H
Power-On Default: 40H

7	6	5	4	3	2	1	0
RBS	TBS	R	R	R	R	R	R

Bits 5–0 Reserved

These bits will read the 6 LSB's of the last command written to this address.

Bit 6 TBS - Transmit Buffer Status
0 = Transmit buffer not full
1 = Transmit buffer full

Bit 7 RBS - Receive Buffer Status
0 = Receive buffer not empty
1 = Receive buffer empty

MIDI UART Command

Write Only Address: Base + 1H
Power-On Default: 00H

7	6	5	4	3	2	1	0
COMMAND							

Bits 7–0 COMMAND

Value = Command byte

5.3.3.2 MIDI UART Operation

The MIDI UART interface powers up in non-UART mode. The RXD input and TXD output are shorted together internally as indicated by the dashed line in Figure 5-7 so that data input on the RXD pin comes out on the TXD pin. Switches S1 and S3 are closed and S2 is open by default. S2 open and the fact that all writes to the data register are ignored mean that the synthesizer is totally isolated after a power-on reset.

In non-UART mode, all reads of the data register (base + 0) return the last data received in the receive FIFO. The FIFO read pointer is not incremented. Two legal commands are available for the host to send to the command register (base + 1, W):

FFH = reset

3FH = UART Mode

A reset command causes an ACK byte (FEH) to be written to the data register. This generates an interrupt and clears bit 7 of the status register to 0 to indicate the receive FIFO is not empty. The interrupt is cleared by a read of the data register. PCI configurations provide only 1 interrupt pin for all interrupts, so CM02 must be read to determine the interrupt source. CM02_7 = 1 specifies a MIDI interrupt. Reading CM02 clears all bits in this register, but not the interrupt, which is cleared by reading the MIDI data register. Generation of this interrupt can be masked via CM01_7. Note that this interrupt information is valid for both non-UART mode and UART mode.

Writing 3FH to the command register initializes UART mode. 3FH is written to the data register and an interrupt is generated.

In UART mode, the connection between the RXD and TXD pins is broken. All writes to the data register are latched in the transmit FIFO. All FIFO data is serialized and clocked out to the TXD pin at a rate of

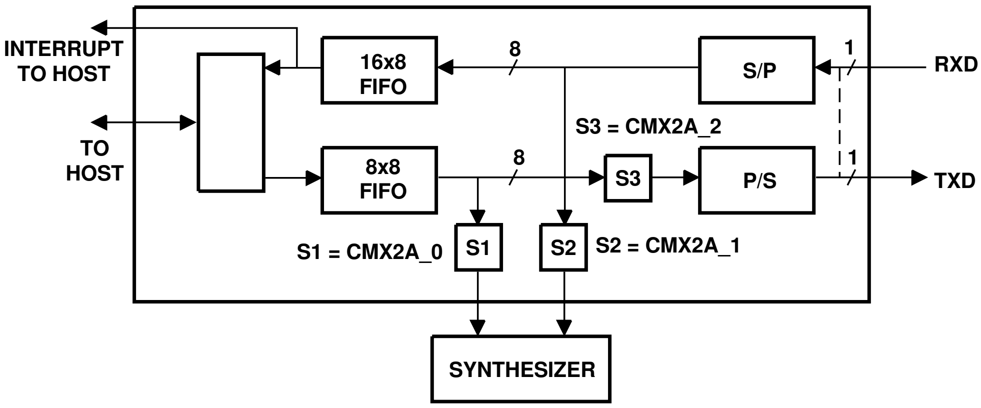

Figure 5-7. MIDI UART Block Diagram

31.25 kbs. Bit 6 of the status register is updated to reflect the current transmit FIFO status. The same data is also sent to the synthesizer because switch S1 is closed.

In UART mode, any serial data input on the RXD pin is converted to parallel and latched in the 16-deep receive FIFO. This generates an interrupt. If the FIFO is full, the last byte is overwritten. The host reads the data register to obtain the next byte in the receive FIFO and clear the interrupt. The status of the receive FIFO register is updated via bit 7 of the status register whenever the data register is read or written.

Only the reset command (FFH) is valid in UART mode. This causes a return to non-UART mode. No ACK byte is written and no interrupt is generated. The receive FIFO pointer is reset, meaning that any data in the FIFO cannot be retrieved. Any data pending in the transmit FIFO is sent. When the transmit FIFO is empty, the RXD and TXD pins are connected again. The switch states are not changed by this reset.

The S3, S2 and S1 switches are controlled via CMX2A_2-0 respectively. Setting a bit to 1 closes the corresponding switch. By default, S1 and S3 are closed and S2 is open. These can be reconfigured by software for special purposes. For example, closing S1 and opening S2 allows a MIDI device to send data directly to the synthesizer as well as the host. Closing S3 stops TXD output without affecting input to the synthesizer.

5.3.4 Game Port/Joystick Timer Interface

This interface conforms to industry standards with a speed compensation extension. Eight input pins (JSD[7:0] connect to a standard game port connector, which in turn connects to one or two joysticks. The inputs are latched in a single 8-bit register accessible at any of 8 consecutive byte addresses. The base address for these registers is that defined by the Game Port Base Address register. This base is normally at 200H.

5.3.4.1 Game Port Register

Table 5-6. Game Port Register

Address (Hex)	Description
Base + 0 to Base + 7	Game Port Register

Game Port Register

Read/Write Address: Base + 0H through 07H
Power-On Default: 00H

Accesses to any address in the address range are made to the same register.

7	6	5	4	3	2	1	0
BF2	BF1	AF2	AF1	BY	BX	AY	AX

Bit 0 AX - Joystick A, X Coordinate

Bit 1 AY - Joystick A, Y Coordinate

Bit 2 BX - Joystick B, X Coordinate

Bit 3 BY - Joystick B, Y Coordinate

Bit 4 AF1 - Joystick A, Fire Button 1

Bit 5 AF2 - Joystick A, Fire Button 2

Bit 6 BF1 - Joystick B, Fire Button 1

Bit 7 BF2 - Joystick B, Fire Button 2

5.3.4.2 Game Port Speed Compensation

The analog coordinate inputs from the joystick are converted to digital values to be latched in the game port register on the basis of comparison with an internal voltage reference. Speed compensation is accomplished by changing the voltage reference. CMX09_4-1 specify the voltage reference (threshold) in 16 steps from 0.1 VDD to 0.85 VDD.

Section 6: Audio Control

SonicVibes provides “legacy” audio control through Sound Blaster Pro games compatibility and emulation of AdLib® OPL3™ FM synthesis operation. To take full advantage of the advanced features of SonicVibes, enhanced mode operation must be used. Each of these three audio control modes is explained below.

6.1 SOUND BLASTER PRO GAMES COMPATIBILITY

Software written for applications assuming the presence of a Sound Blaster or Sound Blaster Pro audio card will operate unchanged (and as expected) on a SonicVibes-based system. Therefore, register and programming details are not provided, as they are available elsewhere. Software written for SonicVibes will typically not use these registers.

6.1.1 Games Compatible Registers

The base address for these registers is that defined by the Games Compatible Base Address register.

Table 6-1. Games Compatible Direct Access Registers

Address (Hex)	Description
Base + 0	Left FM Port: Address (W), Status (R)
Base + 1	Left FM Data Port (W)
Base + 2	Right FM Port: Address (W), Status (R)
Base + 3	Right FM Data Port (W)
Base + 4	Mixer Register Index (W)
Base + 5	Mixer Register Data (R/W)
Base + 6	Reset (W)
Base + 8	FM Status Port (R)
Base + 9	FM Register Port (W)
Base + A	Input Data (R)
Base + C	Write Data/Command (W), Write Buffer Status (R)
Base + E	Read (Output) Buffer Status (R)

Table 6-2. Games Compatible Mixer (Indexed) Registers

<table>
<tr><th rowspan="2">Index (Hex)</th><th rowspan="2">Default (Hex)</th><th colspan="8">Description</th></tr>
<tr><th>Bit 7</th><th>Bit 6</th><th>Bit 5</th><th>Bit 4</th><th>Bit 3</th><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th></tr>
<tr><td>00</td><td>xx</td><td colspan="8">Reset</td></tr>
<tr><td>04</td><td>99</td><td colspan="4">PCM Volume Left</td><td colspan="4">PCM Volume Right</td></tr>
<tr><td>0A</td><td>11</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td colspan="2">MIC</td><td>R</td></tr>
<tr><td>0C</td><td>11</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td colspan="2">ADC Input Select</td><td>R</td></tr>
<tr><td>0E</td><td>11</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td>VSTC</td><td>R</td></tr>
<tr><td>22</td><td>99</td><td colspan="4">Master Volume Left</td><td colspan="4">Master Volume Right</td></tr>
<tr><td>26</td><td>99</td><td colspan="4">FM Volume Left</td><td colspan="4">FM Volume Right</td></tr>
<tr><td>28</td><td>11</td><td colspan="4">CD Volume Left</td><td colspan="4">CD Volume Right</td></tr>
<tr><td>2E</td><td>11</td><td colspan="4">Line Volume Left</td><td colspan="4">Line Volume Right</td></tr>
</table>

6.1.2 Games Compatibility Issues

Sound Blaster Pro games compatibility is enabled when CM00_0 = 0. This is the power-on default. Mixer input naming conventions are not the same for games compatible registers and SonicVibes. This is shown by Table 6-3. The analog inputs must be connected correctly to maintain compatibility, e.g., what would be the Line input for games compatible registers must be connected to the AUX1 input for the SonicVibes. The SonicVibes automatically maps the games compatible registers to the correct SonicVibes registers.

Table 6-3. Mixer Input Naming Conventions

Sound Blaster Name	SonicVibes Name
Line	AUX1
N/A	AUX2
FM	Synthesizer (internal)
CD	CD
N/A	LINE
MIC	MIC
PCM	PCM (Internal)

6.2 S3FM SYNTHESIS

S3FM synthesis can be used in either Sound Blaster emulation mode or enhanced mode (which is described in Section 6.3 below). This provides legacy games-compatible FM synthesis via AdLib OPL3 emulation. The registers are listed in Table 6-4

The base address for these registers is that defined by the FM Base Address register if accessed in enhanced mode or by the Sound Blaster Base address register in Sound Blaster Pro emulation mode.

Table 6-4. S3FM Registers

I/O Address (Hex)	Sound Blaster Address	Default (Hex)	Description
388	Base + 0	00 (Read)	Left FM Port: Address (W), Status (R) - OPL3
389	Base + 1	xx	Left FM Data Port (W) - OPL3
38A	Base + 2	xx	Right FM Port: Address (W), Status (R) - OPL3
38B	Base + 3	x	Right FM Data Port (W) - OPL3
388	Base + 8	xx	FM Status Port (R) - OPL2
389	Base + 9	xx	FM Register Port (W) - OPL2

6.3 ENHANCED MODE

Enhanced mode operation provides features such as down-loadable wavetable samples, SRS 3D audio enhancement, complex mixer and signal paths, with higher sampling rates than previous industry standards. It is enabled by setting CM00_0 to 1. The registers associated with enhanced mode operation are found in Section 7. Note that the directly accessed CODEC/Mixer registers are referenced as CMxx registers (address = base + xx), while the indirectly accessed CODEC/Mixer registers are referenced as CMXxx registers. (write xx to base + 4).

6.3.1 Wavetable Synthesis

The wavetable synthesizer is based on S3S™ sample playback technology. It is 32-voice, 16-multi-timbral and 16-bit resolution, with a maximum output sample rate of 32 kHz. It is both General MIDI and Downloadable Sample Level 1 compliant. The integrated digital effects processor produces high quality reverb and chorus effects. The integrated hardware MIDI interpreter requires no host CPU overhead and eliminates problems with TSR-based emulation.

The synthesizer can address 4 MBytes of ROM and 16 MBytes of host system memory for instrument storage. It supports 8-bit, 16-bit and 8-bit S3 proprietary compression sample data formats. With it's ability for PCI configurations to store sounds in system memory, S3S technology has an unlimited sound palette for musical instrument and special effects. DirectMusic and DirectSound hardware acceleration are supported.

6.3.2 PCM Playback and Record

PCM playback and record are always done via DMA transfers. In games compatible mode, only the DMA_A 8-bit channel is used. Both playback and record are provided for enhanced mode operation. DDMA is used as explained on page 5-5 for hardware games compatibility.

SonicVibes allows playback at one sampling rate (specified via CMX1E and CMX1F) and recording simultaneously at a different sampling rate (specified via CMX22 or CMX23). Loopback is not available in this case, as the loopback input and the PCM playback input must be the same sampling frequency.

6.3.3 CODEC/Mixer Operation

CODEC/Mixer operation is illustrated by Figure 6-1. The register bits used to control each left channel function are shown in conjunction with the function. Parallel right channel bits are also available and are described in Section 7.

The digital mixer always operates at 48 kHz. The sampling rate for wavetable input is programmable, but normally will always be the default level of 32 kHz. The synthesizer performs both FM and wave table synthesis, so only one can be operational at a time.

One analog signal can be selected for mixing with the PCM input. If this capability is enabled (CMX16_0 = 1), the sampling frequencies of the PCM input and the ADC must be exactly the same.

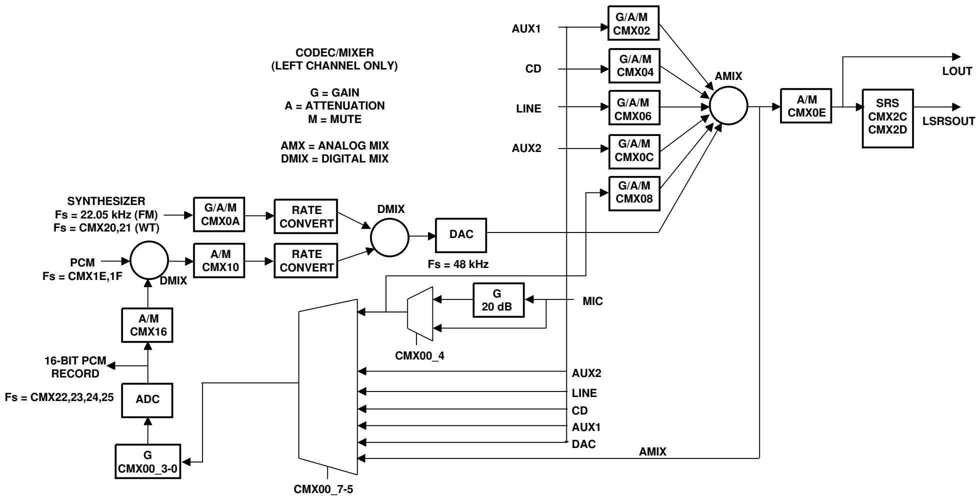

Figure 6-1. CODEC/Mixer Operation

6.3.4 SRS 3D Audio Enhancement

This function is enabled when CMX2C_7 = 0 (default). If CMX2C_7 is set to 1, the SRS function is bypassed. CMX2C_2-0 provide control of the SRS “space” effect. CMX2D_2-0 provide control of the SRS “center” effect.

Section 7: Enhanced Mode Registers

The base address for these registers is that specified by the Enhanced Mode Base Address register (PCI14).

7.1 DIRECT ACCESS CODEC/MIXER REGISTER DESCRIPTIONS

The registers described in this section are accessed directly at an offset from the base address assigned by the BIOS.

Table 7-1. Direct Access CODEC/Mixer Registers

Address (Hex)	Default (Hex)	Description
CODEC/Mixer Registers		
Base + 0	20	CODEC/Mixer Control
Base + 1	48	CODEC/Mixer Interrupt Mask
Base + 2	00	CODEC/Mixer Status (Read Only)
Base + 3		Reserved
Base + 4	40	CODEC/Mixer Index Address
Base + 5	C0	CODEC/Mixer Index Data
Base + 6		Reserved
Base + 7		Reserved

CODEC/Mixer Control Register (CM00)

Read/Write Address: Base + 00H
Power-On Default: 20H

7	6	5	4	3	2	1	0
RST	R	INTA	R	FWS	MD1	R = 0	AMS

Bit 0 AMS - Audio Mode Select
0 = Sound Blaster/Sound Blaster Pro-compatible mode
1 = Enhanced audio mode

Bit 1 TST - Test

This is an S3 test bit and must never be set to 1 in operation use.

Bit 2 MD1 - Reverb Enable
0 = Reverb disabled
1 = Reverb enabled

This bit is initially programmed by power-on strapping of GA20 (pin 111). It should only be set to 1 if external SRAM is connected.

Bit 3 FWS - FM/WT Status
0 = Music input to the DAC is FM
1 = Music input to the DAC is wavetable

This bit is programmed by the hardware based on detection of an FM I/O access or a MIDI I/O access. If FM input is programmed, the DAC sampling rate is automatically set. If wavetable input is programmed (for MIDI), the sampling frequency is specified via the Wavetable Output Sampling Rate registers (CMX20 and CMX21).

Bit 4 Reserved

Bit 5 INTA - INTA Driving
0 = Disable INTA
1 = $\overline{\text{INTA}}$ pin is driven when an interrupt is generated (default)

This bit should always be left at its default value of 1.

Bit 6 Reserved

Bit 7 RST - Reset
0 = No effect
1 = Reset chip (same as power-on reset)

CODEC/Mixer Interrupt Mask Register (CM01)

Read/Write Address: Base + 01H
Power-On Default: 48H

7	6	5	4	3	2	1	0
MIDM	UDM	R	R	SMSK	CMSK	R	AMSK

Bit 0 AMSK - DMA_A Interrupt Mask
0 = Hardware interrupt not masked
1 = Hardware interrupt masked

Bit 1 Reserved

Bit 2 CMSK - DMA_C Interrupt Mask
0 = Hardware interrupt not masked
1 = Hardware interrupt masked

Bit 3 SMSK - Special Interrupt Mask
0 = Interrupts not masked
1 = Interrupts masked (default)

This should always be left masked.

Bits 5-4 Reserved

Bit 6 UDM - Up/Down Button Interrupt Mask
0 = Hardware interrupt not masked
1 = Hardware interrupt masked

Bit 7 MIDM - MIDI Interrupt Mask
0 = Hardware interrupt not masked
1 = Hardware interrupt masked

CODEC/Mixer Status Register (CM02)

Read Only Address: Base + 02H
Power-On Default: 00H

This register is cleared to 00H when read. This also clears the all interrupts except for the MIDI interrupt, which is cleared when MIDI data register is read.

7	6	5	4	3	2	1	0
MI	UDI	R	R	SINT	CINT	R	AINT

Bit 0 AINT - DMA_A Interrupt Status
0 = No DMA_A interrupt generated
1 = Interrupt generated

An interrupt is automatically generated when the DMA_A counter reaches zero regardless of the state of CM01_0.

Bit 1 Reserved

Bit 2 CINT - DMA_C Interrupt Status
0 = No interrupt generated
1 = Interrupt generated

An interrupt is automatically generated when the DMA_C counter reaches zero regardless of the state of CM01_2.

Bit 3 SINT - Special Interrupt Status
0 = No interrupt generated
1 = Interrupt generated if not masked

This interrupt should always be masked, so this bit should always read 0.

Bits 5-4 Reserved

Bit 6 UDI - Up/Down Button Interrupt Status
0 = No interrupt generated
1 = Interrupt generated

An interrupt is automatically generated when either the $\overline{\text{UP}}$ or $\overline{\text{DOWN}}$ input is asserted regardless of the state of CM01_6.

Bit 7 MI - MIDI Interrupt Status
0 = No interrupt generated
1 = Interrupt generated

CODEC/Mixer Index Address Register (CM04)

Read/Write Address: Base + 04H
Power-On Default: 40H

7	6	5	4	3	2	1	0
TRD	MCE	CODEC/MIXER INDEX[5:0]					

Bits 5–0 CODEC/MIXER INDEX

Value = Index (in hex) of the indexed CODEC/Mixer register to be accessed.

Bit 6 MCE - Mode Change Enable
0 = Normal operation
1 = Enable mode change

This bit must be set to 1 before programming the DMA Data Format register (CMX13). The DAC is muted when this bit is set.

Bit 7 TRD - DMA Transfer Request Disabled
0 = Allow DMA transfer
1 = Disable DMA transfer

CODEC/Mixer Index Data Register (CM05)

Read/Write Address: Base + 05H
Power-On Default: C0H

7	6	5	4	3	2	1	0
CODEC/MIXER DATA[7:0]							

Bits 7–0 CODEC/MIXER DATA

Value = Data written to or data read from the CODEC/Mixer register at the index location specified in the CODEC/Mixer Index Address register (CM04).

7.2 INDEXED CODEC/MIXER REGISTER DESCRIPTIONS

The following registers are accessed by writing the index to the CODEC/Mixer Index Address register (CM04) and then data is written to or read from the CODEC/Mixer Index Data register (CM05).

Table 7-2. Indexed CODEC/Mixer Registers

Index (Hex)	Default (Hex)	Description	Page
00	C0	Left ADC Input Control	8
01	C0	Right ADC Input Control	9
02	80	Left AUX1 Input Control	10
03	80	Right AUX1 Input Control	10
04	80	Left CD Input Control	11
05	80	Right CD Input Control	11
06	80	Left Line Input Control	12
07	80	Right Line Input Control	12
08	88	MIC Input Line Control	13
09	10	Game Port Control	13
0A	0F	Left Synthesizer Input Control	14
0B	0F	Right Synthesizer Input Control	14
0C	80	Left AUX2 Input Control	15
0D	80	Right AUX2 Input Control	15
0E	07	Left Analog Mixer Output Control	16
0F	07	Right Analog Mixer Output Control	16
10	80	Left PCM Input Control	17
11	80	Right PCM Input Control	17
12	00	DMA Data Format	18
13	00	Playback/Capture Enable Register	18
14	00	Up/Down Button Register	19
15	01	Revision	20
16	00	ADC Output Control	20
18	00	DMA_A Upper Base Count	21
19	00	DMA_A Lower Base Count	21
1C	00	DMA_C Upper Base Count	22
1D	00	DMA_C Lower Base Count	22
1E	75	PCM Sampling Rate Low Byte	23
1F	99	PCM Sampling Rate High Byte	23
20	AA	Synthesizer Sampling Rate Low Byte	24
21	AA	Synthesizer Sampling Rate High Byte	24
22	00	ADC Clock Source Selection	25
23	40	ADC Alternative Sampling Rate Selection	25
24	09	ADC PLL M Register	26
25	61	ADC PLL N Register	26
26	0A	Synthesizer PLL M Register	27

Index (Hex)	Default (Hex)	Description	Page
27	21	Synthesizer PLL N Register	27
2A	05	MPU-401 UART Operation	28
2B	00	Drive Control	29
2C	00	SRS Space Control	29
2D	00	SRS Center Control	30
2E	00	Wavetable Sample Source Select	30
30	00	Analog Power Down Control	31
31	00	Digital Power Down Control	32

Left ADC Input Control Register (CMX00)

Read/Write Index: 00H
Power-On Default: C0H

7	6	5	4	3	2	1	0
ADC LEFT INPUT			MGE	ADC LEFT INPUT GAIN			

Bits 3–0 ADC LEFT INPUT GAIN

Value (integer) = (dB gain/1.5)

0000 = 0 dB (default)
0001 = 1.5 dB
0010 = 3 dB
0011 = 4.5 dB
0100 = 6 dB
0101 = 7.5 dB
0110 = 9 dB
0111 = 10.5
1000 = 12 dB
1001 = 13.5 dB
1010 = 15 dB
1011 = 16.5 dB
1100 = 18 dB
1101 = 19.5 dB
1110 = 21 dB
1111 = 22.5 dB

Bit 4 MGE - MIC Gain Enable
0 = No gain for MIC input (default)
1 = Additional 20 dB gain for MIC input

This gain is applied before the gain specified by bits 3-0 of this register.

Bits 7-5 ADC LEFT INPUT SELECTOR
000 = Reserved
001 = Left CD
010 = Left DAC
011 = Left AUX2
100 = Left Line
101 = Left AUX1
110 = MIC (default)
111 = Left Mixer Out

Right ADC Input Control Register (CMX01)

Read/Write Index: 01H
Power-On Default: C0H

7	6	5	4	3	2	1	0
ADC RIGHT INPUT			R	ADC RIGHT INPUT GAIN			

Bits 3–0 ADC RIGHT INPUT GAIN

Value (integer) = (dB gain/1.5)

0000 = 0 dB (default)
0001 = 1.5 dB
0010 = 3 dB
0011 = 4.5 dB
0100 = 6 dB
0101 = 7.5 dB
0110 = 9 dB
0111 = 10.5
1000 = 12 dB
1001 = 13.5 dB
1010 = 15 dB
1011 = 16.5 dB
1100 = 18 dB
1101 = 19.5 dB
1110 = 21 dB
1111 = 22.5 dB

Bit 4 Reserved

Bits 7-5 ADC RIGHT INPUT SELECTOR
000 = Reserved
001 = Right CD
010 = Right DAC
011 = Right AUX2
100 = Right Line
101 = Right AUX1
110 = MIC (default)
111 = Right Mixer Out

Left AUX1 Input Control Register (CMX02)

Read/Write Index: 02H
Power-On Default: 80H

7	6	5	4	3	2	1	0
LA1M	R	R	LEFT AUX1 INPUT LEVEL				

Bits 4–0 LEFT AUX1 INPUT LEVEL

Value = IL = integer such that:

dB = 12 - 1.5 IL

The default value (00000b) corresponds to a gain of 12 dB when the input is not muted (bit 7 = 0). All values greater than 8 result in -dB levels (attenuation). This is the input level to the analog mixer.

Bits 6-5 Reserved

Bit 7 LAIM - Left AUX1 Input Mute
0 = Input not muted
1 = Input muted (default)

Right AUX1 Input Control Register (CMX03)

Read/Write Index: 03H
Power-On Default: 80H

7	6	5	4	3	2	1	0
RA1M	R	R	RIGHT AUX1 INPUT LEVEL				

Bits 4–0 RIGHT AUX1 INPUT LEVEL

Value = IL = integer such that:

dB = 12 - 1.5 IL

The default value (00000b) corresponds to a gain of 12 dB when the input is not muted (bit 7 = 0). All values greater than 8 result in -dB levels (attenuation). This is the input level to the analog mixer.

Bits 6-5 Reserved

Bit 7 RAIM - Right AUX1 Input Mute
0 = Input not muted
1 = Input muted (default)

Left CD Input Control Register (CMX04)

Read/Write Index: 04H
Power-On Default: 80H

7	6	5	4	3	2	1	0
LCDM	R	R	LEFT CD INPUT LEVEL				

Bits 4–0 LEFT CD INPUT LEVEL

Value = IL = integer such that:

dB = 12 - 1.5 IL

The default value (00000b) corresponds to a gain of 12 dB when the input is not muted (bit 7 = 0). All values greater than 8 result in -dB levels (attenuation). This is the input level to the analog mixer.

Bits 6-5 Reserved

Bit 7 LCDM - Left CD Input Mute
0 = Input not muted
1 = Input muted (default)

Right CD Input Control Register (CMX05)

Read/Write Index: 05H
Power-On Default: 80H

7	6	5	4	3	2	1	0
RCDM	R	R	RIGHT CD INPUT LEVEL				

Bits 4–0 RIGHT CD INPUT LEVEL

Value = IL = integer such that:

dB = 12 - 1.5 IL

The default value (00000b) corresponds to a gain of 12 dB when the input is not muted (bit 7 = 0). All values greater than 8 result in -dB levels (attenuation). This is the input level to the analog mixer.

Bits 6-5 Reserved

Bit 7 RCDM - Right CD Input Mute
0 = Input not muted
1 = Input muted (default)

Left Line Input Control Register (CMX06)

Read/Write Index: 06H
Power-On Default: 80H

7	6	5	4	3	2	1	0
LLM	R	R	LEFT LINE INPUT LEVEL				

Bits 4–0 LEFT LINE INPUT LEVEL

Value = IL = integer such that:

dB = 12 - 1.5 IL

The default value (00000b) corresponds to a gain of 12 dB when the input is not muted (bit 7 = 0). All values greater than 8 result in -dB levels (attenuation). This is the input level to the analog mixer.

Bits 6-5 Reserved

Bit 7 LLM - Left Line Input Mute
0 = Input not muted
1 = Input muted (default)

Right Line Input Control Register (CMX07)

Read/Write Index: 07H
Power-On Default: 80H

7	6	5	4	3	2	1	0
RLM	R	R	RIGHT LINE INPUT LEVEL				

Bits 4–0 RIGHT LINE INPUT LEVEL

Value = IL = integer such that:

dB = 12 - 1.5 IL

The default value (00000b) corresponds to a gain of 12 dB when the input is not muted (bit 7 = 0). All values greater than 8 result in -dB levels (attenuation). This is the input level to the analog mixer.

Bits 6-5 Reserved

Bit 7 RLM - Right Line Input Mute
0 = Input not muted
1 = Input muted (default)

MIC Input Control Register (CMX08)

Read/Write Index: 08H
Power-On Default: 88H

7	6	5	4	3	2	1	0
MICM	R	R	R	MIC INPUT LEVEL			

Bits 3–0 MIC INPUT LEVEL

Value = IL = integer such that:

dB = 12 - 1.5 IL

The default value (0000b) corresponds to a gain of 12 dB when the input is not muted (bit 7 = 0). All values greater than 8 result in -dB levels (attenuation). This is the input level to the analog mixer.

Bits 6-4 Reserved

Bit 7 MICM - MIC Input Mute
0 = Input not muted
1 = Input muted (default)

Game Port Control Register (CMX09)

Read/Write Index: 09H
Power-On Default: 10H

7	6	5	4	3	2	1	0
R	R	R	GP SPEED COMP				R

Bits 3–0 GP SPEED COMP
0000 = Threshold voltage is 0.1 VDD
0001 = Threshold voltage is 0.15 VDD
0010 = Threshold voltage is 0.2 VDD
.
.
1000 = Threshold voltage is 0.5 VDD (default)
.
.
1111 = Threshold voltage is 0.85 VDD

The general formula is TV = [(0.1 +0.05xGP)]xVDD, where TV is the threshold voltage used for speed compensation and GP is the value in bits 4-1.

Left Synthesizer Input Control Register (CMX0A)

Read/Write Index: 0AH
Power-On Default: 0FH

This is the digital wavetable or FM input as indicated by CM00_3.

7	6	5	4	3	2	1	0
LSM	R	R	LEFT SYNTHESIZER INPUT LEVEL				

Bits 4–0 LEFT SYNTHESIZER INPUT LEVEL

Value = IL = integer such that:

dB = 12 - 1.5 IL

The default corresponds to -10.5 dB. All values greater than 8 result in -dB levels (attenuation). This is an input to the digital mixer.

Bits 6-5 Reserved

Bit 7 LSM - Left Synthesizer Input Mute
0 = Input not muted (default)
1 = Input muted

Right Synthesizer Input Control Register (CMX0B)

Read/Write Index: 0BH
Power-On Default: 0FH

This is the digital wavetable or FM input as indicated by CM00_3.

7	6	5	4	3	2	1	0
RSM	R	R	RIGHT SYNTHESIZER INPUT LEVEL				

Bits 4–0 RIGHT SYNTHESIZER INPUT LEVEL

Value = IL = integer such that:

dB = 12 - 1.5 IL

The default corresponds to -10.5 dB. All values greater than 8 result in -dB levels (attenuation). This is the input to the digital mixer.

Bits 6-5 Reserved

Bit 7 RSM - Right Synthesizer Input Mute
0 = Input not muted (default)
1 = Input muted

Left AUX2 Input Control Register (CMX0C)

Read/Write Index: 0CH
Power-On Default: 80H

7	6	5	4	3	2	1	0
LA2M	R	R	LEFT AUX2 INPUT LEVEL				

Bits 4–0 LEFT AUX2 INPUT LEVEL

Value = IL = integer such that:

dB = 12 - 1.5 IL

The default value (00000b) corresponds to a gain of 12 dB when the input is not muted (bit 7 = 0). All values greater than 8 result in -dB levels (attenuation). This is the input level to the analog mixer.

Bits 6-5 Reserved

Bit 7 LA2M - Left AUX2 Input Mute
0 = Input not muted
1 = Input muted (default)

Right AUX2 Input Control Register (CMX0D)

Read/Write Index: 0DH
Power-On Default: 80H

7	6	5	4	3	2	1	0
RA2M	R	R	RIGHT AUX2 INPUT LEVEL				

Bits 4–0 RIGHT AUX2 INPUT LEVEL

Value = IL = integer such that:

dB = 12 - 1.5 IL

The default value (00000b) corresponds to a gain of 12 dB when the input is not muted (bit 7 = 0). All values greater than 8 result in -dB levels (attenuation). This is the input level to the analog mixer.

Bits 6-5 Reserved

Bit 7 RA2M - Right AUX2 Input Mute
0 = Input not muted
1 = Input muted (default)

Left Analog Mixer Output Control Register (CMX0E)

Read/Write Index: 0EH
Power-On Default: 07H

7	6	5	4	3	2	1	0
LMM	R	R	LEFT MIXER OUTPUT LEVEL				

Bits 4–0 LEFT MIXER OUTPUT LEVEL

Value = OL = integer such that:

-dB = 1.5 OL

The default value (7) corresponds to -10.5 dB.

Bits 6-5 Reserved

Bit 7 LMM - Left Mixer Output Mute
0 = Output not muted (default)
1 = Output muted

Right Analog Mixer Output Control Register (CMX0F)

Read/Write Index: 0FH
Power-On Default: 07H

7	6	5	4	3	2	1	0
RMM	R	R	RIGHT MIXER OUTPUT LEVEL				

Bits 4–0 RIGHT MIXER OUTPUT LEVEL

Value = OL = integer such that:

-dB = 1.5 OL

The default value (7) corresponds to-10.5 dB.

Bits 6-5 Reserved

Bit 7 RMM - Right Mixer Output Mute
0 = Output not muted (default)
1 = Output muted

Left PCM Input Control Register (CMX10)

Read/Write Index: 10H
Power-On Default: 80H

7	6	5	4	3	2	1	0
LPM	R	LEFT PCM INPUT LEVEL					

Bits 5–0 LEFT PCM INPUT LEVEL

Value = IL = integer such that:

-dB = 1.5 IL

The default value (000000b) corresponds to an attenuation of 0 dB. The maximum attenuation is 94.5 dB. This is an input to the digital mixer.

Bit 6 Reserved

Bit 7 LPM - Left PCM Mute
0 = Input not muted
1 = Input muted (default)

Right PCM Input Control Register (CMX11)

Read/Write Index: 11H
Power-On Default: 80H

7	6	5	4	3	2	1	0
RPM	R	RIGHT PCM INPUT LEVEL					

Bits 4–0 RIGHT PCM INPUT LEVEL

Value = IL = integer such that:

-dB = 1.5 IL

The default value (000000b) corresponds to an attenuation of 0 dB. The maximum attenuation is 94.5 dB. This is an input to the digital mixer.

Bits 6-5 Reserved

Bit 7 RPM - Right PCM Mute
0 = Input not muted
1 = Input muted (default)

DMA Data Format Register (CMX12)

Read/Write Index: 12H
Power-On Default: 00H

Bit 6 of CM04 must be set to 1 whenever the data format is changed.

7	6	5	4	3	2	1	0
R	R	CF	CS/M	R	R	AF	AS/M

Bit 0 AS/M - DMA_A Stereo/Mono Select
0 = Mono
1 = Stereo

Bit 1 AF - DMA_A Data Format
0 = 8-bit unsigned PCM data
1 = 16-bit 2's complement PCM data

Bits 3-2 Reserved

Bit 4 CS/M - DMA_C Stereo/Mono Select
0 = Mono
1 = Stereo

Bit 5 CF - DMA_C Data Format
0 = 8-bit unsigned PCM data
1 = 16-bit 2's complement PCM data

Bits 7-6 Reserved

Playback/Record Enable Register (CMX13)

Read/Write Index: 13H
Power-On Default: 08H

7	6	5	4	3	2	1	0
R	R	R	R	R	PPE	RE	PE

Bit 0 PE - Playback Enable
0 = Playback disabled
1 = Playback enabled

Bit 1 RE - Record Enable
0 = Record disabled
1 = Record enabled

Bit 2 PPE - Playback Pause Enable
0 = Pause disabled
1 = Pause enabled

Bits 7–3 Reserved

Up/Down Button Register (CMX14)

Read Only Index: 14H
Power-On Default: 00H

An interrupt is generated when either the $\overline{\text{UP}}$ or $\overline{\text{DOWN}}$ pin is asserted (unless masked via CM01_6 = 1). An up/down counter is incremented or decremented each 10 Hz rising clock edge as long as the input is asserted (up to the maximum counter value of 31). Muting is signaled when both the $\overline{\text{UP}}$ and $\overline{\text{DOWN}}$ pins are asserted at the same time. Software reads this register to determine what action to take (mute or change volume).

This register is cleared to 00H upon being read.

7	6	5	4	3	2	1	0
MUTE	U/D	UP/DOWN COUNTER					

Bits 5–0 UP/DOWN COUNTER

Value = # of 10 Hz clock rising edges either the $\overline{\text{UP}}$ or $\overline{\text{DOWN}}$ pin has been asserted

Bit 6 U/D - Up/Down Input
0 = $\overline{\text{DOWN}}$ pin asserted
1 = $\overline{\text{UP}}$ pin asserted

Bit 7 MUTE
0 = No muting requested
1 = Muting input ($\overline{\text{UP}}$ and $\overline{\text{DOWN}}$ both asserted)

Revision Level Register (CMX15)

Read Only Index: 15H
Power-On Default: xxH

7	6	5	4	3	2	1	0
REVISION LEVEL							

Bits 7–0 REVISION LEVEL

This value will change with different revisions of the chip.

Digital Loopback Control Register (CMX16)

Read/Write Index: 16H
Power-On Default: 00H

7	6	5	4	3	2	1	0
LOOPBACK INPUT LEVEL						R	DLE

Bit 0 DLE - Digital Loopback Enable
0 = Output of ADC and attenuator is not input to the digital mixer
1 = Output of ADC and attenuator is input to the digital mixer

The ADC output (before attenuation) is always available for recording.

Bit 1 Reserved

Bits 7-2 LOOPBACK INPUT LEVEL

Value = IL = integer such that:

-dB = 1.5 IL

The default value (0) corresponds to an attenuation of 0 dB. The maximum attenuation is 94.5 dB. This is the loopback input from the ADC to the digital mixer if enabled via bit 0 of this register and an analog source is enabled for loopback.

DMA_A Upper Base Count Register (CMX18)

Read/Write Index: 18H
Power-On Default: 00H

7	6	5	4	3	2	1	0
DMA_A UPPER BASE COUNT							

Bits 7–0 DMA_A UPPER BASE COUNT

16-bit Value = # of bytes to be transferred -1

When this value is loaded, an internal counter decrements from this value until it reaches 0. An interrupt is generated at this time unless it is masked via CM01_0. The lower byte of this value is in CMX19.

DMA_A Lower Base Count Register (CMX19)

Read/Write Index: 19H
Power-On Default: 00H

7	6	5	4	3	2	1	0
DMA_A LOWER BASE COUNT							

Bits 7–0 DMA_A LOWER BASE COUNT

16-bit Value = # of bytes to be transferred -1

When this value is loaded, an internal counter decrements from this value until it reaches 0. An interrupt is generated at this time unless it is masked via CM01_0. The upper byte of this value is in CMX18.

DMA_C Upper Base Count Register (CMX1C)

Read/Write Index: 1CH
Power-On Default: 00H

7	6	5	4	3	2	1	0
DMA_C UPPER BASE COUNT							

Bits 7–0 DMA_C UPPER BASE COUNT

16-bit Value = # of words to be transferred -1

When this value is loaded, an internal counter decrements from this value until it reaches 0. An interrupt is generated at this time unless it is masked via CM01_2. The lower byte of this value is in CMX1D.

DMA_C Lower Base Count Register (CMX1D)

Read/Write Index: 1DH
Power-On Default: 00H

7	6	5	4	3	2	1	0
DMA_C LOWER BASE COUNT							

Bits 7–0 DMA_C LOWER BASE COUNT

16-bit Value = # of words to be transferred -1

When this value is loaded, an internal counter decrements from this value until it reaches 0. An interrupt is generated at this time unless it is masked via CM01_2. The upper byte of this value is in CMX1C.

PCM Sampling Rate Low Byte Register (CMX1E)

Read/Write Index: 1EH
Power-On Default: 99H

7	6	5	4	3	2	1	0
PCM SAMPLING RATE LOW BYTE							

Bits 7–0 PCM SAMPLING RATE FACTOR LOW BYTE

16-bit Value = PCM = integer such that:

SR = 48*PCM/65536

where SR is the sampling rate in kHz for the PCM data being transferred to the digital mixer. The default value corresponds to a sampling rate of 22.05 kHz. The maximum value (FFH) corresponds to a sampling rate of 47.99927 kHz. The high byte of this value is in CMX1F.

If digital loopback is enabled (CMX16_0 = 1), the PCM sampling rate must be the same as the ADC sampling rate.

PCM Sampling Rate High Byte Register (CMX1F)

Read/Write Index: 1FH
Power-On Default: 75H

7	6	5	4	3	2	1	0
PCM SAMPLING RATE HIGH BYTE							

Bits 7–0 PCM SAMPLING RATE HIGH BYTE

16-bit Value = PCM = integer such that:

SR = 48*PCM/65536

where SR is the sampling rate in kHz for the PCM data being transferred to the digital mixer. The default value corresponds to a sampling rate of 22.05 kHz. The maximum value (FFH) corresponds to a sampling rate of 47.99927 kHz. The low byte of this value is in CMX1E.

If digital loopback is enabled (CMX16_0 = 1), the PCM sampling rate must be the same as the ADC sampling rate.

Synthesizer Sampling Rate Low Byte Register (CMX20)

Read/Write Index: 20H
Power-On Default: AAH

7	6	5	4	3	2	1	0
SYNTHESIZER SAMPLING RATE LOW BYTE							

Bits 7–0 SYNTHESIZER SAMPLING RATE LOW BYTE

16-bit Value = SYN = integer such that:

SR = 48*SYN/65536

where SR is the sampling rate in kHz of data generated by the synthesizer. The default value corresponds to a sampling rate of 32 kHz. The maximum value (FFH) corresponds to a sampling rate of 47.99927 kHz. The high byte of this value is in CMX21.

This register should normally never be reprogrammed. If it is, changes must also be made to the synthesizer firmware. The 32 kHz default is appropriate for wavetable data (as indicated by CM00_3 = 1). If the synthesizer data is FM (as indicated by CM00_3 = 0), the sampling rate is automatically changed to 22.05 kHz. Reprogramming this register during FM operation can cause serious problems. Note that CM00_3 is programmed by the hardware based on its detection of FM or MIDI (wavetable) accesses.

Synthesizer Sampling Rate High Byte Register (CMX21)

Read/Write Index: 21H
Power-On Default: AAH

7	6	5	4	3	2	1	0
SYNTHESIZER SAMPLING RATE HIGH BYTE							

Bits 7–0 SYNTHESIZER SAMPLING RATE HIGH BYTE

16-bit Value = SYN = integer such that:

SR = 48 SYN/65536

where SR is the sampling rate in kHz of data generated by the synthesizer. The default value corresponds to a sampling rate of 32 kHz. The maximum value (FFH) corresponds to a sampling rate of 47.99927 kHz. The low byte of this value is in CMX20.

This register should normally never be reprogrammed. If it is, changes must also be made to the synthesizer firmware. The 32 kHz default is appropriate for wavetable data (as indicated by CM00_3 = 1). If the synthesizer data is FM (as indicated by CM00_3 = 0), the sampling rate is automatically changed to 22.05 kHz. Reprogramming this register during FM operation can cause serious problems. Note that CM00_3 is programmed by the hardware based on its detection of FM or MIDI (wavetable) accesses.

ADC Clock Source Register (CMX22)

Read/Write Index: 22H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	ADCS	R	R	R	R

Bits 3-0 Reserved

Bit 4 ADCS - ADC Clock Source Selection
0 = Use ADC PLL as the ADC clock source (CMX24, CMX25)
1 = Use alternate sampling rate (CMX23_7-4) for the ADC clock

In either case, if ADC loopback data is to be mixed with PCM data, the same sampling rate must be used to generate both types of data.

Bits 7-5 Reserved

ADC Alternate Sampling Rate Register (CMX23)

Read/Write Index: 23H
Power-On Default: 40H

7	6	5	4	3	2	1	0
ASR				R	R	R	R

Bits 3–0 Reserved

Bits 7-4 ASR - ADC Alternate Sampling Rate Parameter

Value = ASR = integer such that:

SR = 48/(ASR + 1)

where SR is the ADC sampling rate in kHz to be used if CMX22_4 = 1. The maximum sampling rate is 48 kHz (ASR = 0). The default value of 4 selects a 9.6 kHz sampling rate.

ADC PLL M Register (CMX24)

Read/Write Index: 24H
Power-On Default: 09H

7	6	5	4	3	2	1	0
ADC PLL M VALUE							

Bits 7–0 ADC PLL M VALUE

These bits contain the binary equivalent of the integer (1-127) divider used in the feedback loop of the ADC PLL. See Appendix A for details. The ADC PLL is used to generate the ADC sampling frequency when CMX22_4 = 0. The defaults for CMX24 and CMX25 produce a frequency of 11.2896 MHz. The sampling frequency is 1/512 of this, or 22.05 kHz. See Appendix A for details.

ADC PLL N Register (CMX25)

Read/Write Index: 25H
Power-On Default: 61H

See CMX24 for more information.

7	6	5	4	3	2	1	0
ADC PLL R VALUE			ADC PLL N VALUE				

Bits 4–0 ADC PLL N VALUE

These bits contain the binary equivalent of the integer (1-31) divider used to scale the input of the ADC PLL. See Appendix A for details.

Bits 7-5 ADC PLL R VALUE

These bits contain the binary equivalent of the integer (1-7) range value used to scale the output of the ADC PLL. See Appendix A for details.

Synthesizer PLL M Register (CMX 26)

Read/Write Index: 26H
Power-On Default: 0AH

7	6	5	4	3	2	1	0
SYNTHESIZER PLL M VALUE							

Bits 7–0 SYNTHESIZER PLL M VALUE

These bits contain the binary equivalent of the integer (1-127) divider used in the feed-back loop of the synthesizer PLL. See Appendix A for details. The defaults for CMX26 and CMX27 produce a frequency of 50 MHz. This frequency should not be changed under normal circumstances. See Appendix A for details.

Synthesizer PLL N Register (CMX27)

Read/Write Index: 27H
Power-On Default: 21H

See CMX26 for more information.

7	6	5	4	3	2	1	0
SYN PLL R VALUE			SYN PLL N VALUE				

Bits 4–0 SYN PLL N VALUE

These bits contain the binary equivalent of the integer (1-31) divider used to scale the input of the synthesizer PLL. See Section Appendix A for details.

Bits 7-5 SYN PLL R VALUE

These bits contain the binary equivalent of the integer (1-7) range value used to scale the output of the synthesizer PLL. See Appendix A for details.

MPU-401 UART Operation Register (CMX2A)

Read/Write Index: 2AH
Power-On Default: 05H

7	6	5	4	3	2	1	0
EXSC	EXAC	R	R	R	S3	S2	S1

Bit 0 S1 - UART Internal Switch 1
0 = Switch off
1 = Switch on (default)

With this switch on, host MIDI data can be sent to the synthesizer.

Bit 1 S2 - UART Internal Switch 2
0 = Switch off (default)
1 = Switch on

With this switch on, external MIDI data (incoming from RXD pin) can be sent to the synthesizer.

Bits 2 S3 - UART Internal Switch 3
0 = Switch off
1 = Switch on (default)

With this switch on, host MIDI data can be output on the TXD pin.

Bits 5-3 Reserved

Bit 6 EXAC - External ADC Clock
0 = Internal ADC PLL is ADC clock source
1 = ADC clock source is input on pin 68

An external clock source is used only for S3 testing. This function is available only when the $\overline{\text{TESTEN}}$ pin is pulled low.

Bit 7 EXSC - External Synthesizer Clock
0 = Internal synthesizer PLL is synthesizer clock source
1 = Synthesizer clock source is input on pin 67

An external clock source is used only for S3 testing. This function is available only when the $\overline{\text{TESTEN}}$ pin is pulled low.

Drive Control Register (CMX2B)

Read/Write Index: 2BH
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	ODC	R	R	R	R	R	R

Bits 5–0 Reserved for S3 testing

Bit 6 ODC - Output Drive Control
0 = 16/8 mA drive outputs configured for 16 mA
1 = 16/8 mA drive outputs configured for 8 mA

Bit 7 Reserved

SRS Space Control Register (CMX2C)

Read/Write Index: 2CH
Power-On Default: 00H

7	6	5	4	3	2	1	0
SOFF	R	R	R	R	SRS SPACE		

Bits 2–0 SRS SPACE
000 = 100%
001 = 75 %
010 = 50 %
011 = 25%
1xx = 0%

Bits 6-3 Reserved

Bit 7 SOFF - SRS Off
0 = SRS function enabled
1 = SRS function bypassed (no stereo expansion)

SRS Center Control Register (CMX2D)

Read/Write Index: 2DH
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	R	R	SRS CENTER		

Bits 2–0 SRS CENTER
000 = 100%
001 = 75 %
010 = 50 %
011 = 25%
1xx = 0%

Bits 7-3 Reserved

Wavetable Sample Source Select Register (CMX2E)

Read/Write Index: 2EH
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	R	R	R	WT1	WT0

Bit 0 WT0 - Wavetable Sample Source Select 0
0 = Wavetable samples provided by on-board ROM
1 = Wavetable samples provided via PCI interface

This bit is initially programmed at power-on reset via strapping of pin 112. Note that the polarity of this bit is reversed from that of the strapping.

Bit 1 WT1 - Wavetable Sample Source Select 1
0 = Wavetable sample source defined by bit 0 of this register
1 = Both ROM and PCI used as wavetable sample source

Bits 7-2 Reserved

Analog Power Down Control Register (CMX30)

Read/Write Index: 30H
Power-On Default: 00H

7	6	5	4	3	2	1	0
APLL	SPLL	SRS	AMIX	ADC	R	R	DAC

Bit 0 DAC
0 = DAC block powered up
1 = DAC block powered down

Note: Software must mute both the synthesizer and PCM inputs and the mixer output before this bit is set to avoid audible clicks.

Bits 2-1 Reserved

Bit 3 ADC
0 = ADC block powered up
1 = ADC block powered down

Bit 4 AMIX
0 = Analog mixer block powered up
1 = Analog mixer block powered down

Note: Software must mute the mixer output before this bit is set to avoid audible clicks.

Bit 5 SRS
0 = SRS block powered up
1 = SRS block powered down

Note: Software must mute the mixer output before this bit is set to avoid audible clicks.

Bit 6 SPLL
0 = Synthesizer PLL block powered up
1 = Synthesizer PLL block powered down

Bit 7 APLL
0 = ADC PLL block powered up
1 = ADC PLL block powered down

Digital Power Down Control Register (CMX31)

Read/Write Index: 31H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	R	BI	GP	MU	SYN

Bit 0 SYN
0 = Synthesizer block powered up
1 = Synthesizer block powered down

Bit 1 MU
0 = MPU-401 UART block powered up
1 = MPU-401 UART block powered down

Bit 2 GP
0 = Game port block powered up
1 = Game port block powered down

Bit 3 BI
0 = Bus interface block powered up
1 = Bus interface block powered down

Games compatible registers are reset. Programmed I/O can still be performed after the bus interface block is powered down.

Bits 7-4 Reserved

Section 8: PCI Registers

The configuration register space occupies 256 bytes. When a configuration read or write command is issued, the AD[7:0] lines contain the address of the register in this space to be accessed. The SonicVibes supports or returns 0 for the first 64 bytes of this space. Beyond this point, it supports user defined functions.

In the following register descriptions, 'R' stands for reserved (write = 0, read = undefined). See Appendix A for a table listing each of the registers in this section and its page number.

Table 8-1. Supported PCI Registers

Byte 3	Byte 2	Byte 1	Byte 0	Offset (Hex)
Device ID		Vendor ID		00
Status		Command		04
Class	Sub-Class		Revision ID	08
		Latency Timer		0C
Games-compatible Base Address				10
Enhanced Mode Base Address				14
FM Synthesis Base Address				18
MIDI Base Address				1C
Game Port Base Address				20
Subsystem ID		Subsystem Vendor ID		2C
Max Latency	Min Grant	Interrupt Pin	Interrupt Line	3C
DMA_A Configuration				40
DMA_C Configuration				48
Reserved				50
Wavetable Memory Base Address				60

Vendor ID Register

Read Only Address: 00H
Power-On Default: 5333H

This read-only register identifies the device manufacturer.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Vendor ID															

Bits 15–0 Vendor ID

This is hardwired to 5333H to identify S3 Incorporated.

Device ID Register

Read Only Address: 02H
Power-On Default: CA00H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Device ID															

Bits 15–0 Device ID

value = CA00H (hardwired)

Command Register

Read/Write Address: 04H
Power-On Default: 0000H

This register controls which types of PCI cycles the SonicVibes can generate and respond to.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	R	PCE	R	R	R	BME	R	I/O

Bit 0 I/O - Enable Response to I/O Accesses
0 = Response to I/O space accesses is disabled
1 = Response to I/O space accesses enabled

Bit 1 Reserved

Bit 2 BME - Bus Master Operation Enable
0 = Bus master operation disabled
1 = Bus master operation enabled

Bits 5-3 Reserved

Bit 6 PCE - Parity Checking Enable
0 = Parity checking disabled
1 = Parity checking disabled

Bits 15–7 Reserved

Status Register

Read/Write Address: 06H
Power-On Default: 0240H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	DEVSEL		R	R	UDF	R	R	R	R	R	R

Bits 5–0 Reserved

Bit 6 UDF - User Definable Features

value = 1 (user selectable configuration items implemented)

Bits 7-8 Reserved

Bits 10–9 DEVSEL - Device Select Timing

value = 01 (medium $\overline{\text{DEVSEL}}$ timing) (hardwired)

Bits 15–11 Reserved

Class Code

Read Only Address: 08H
Power-On Default: 040100xxH

This register is hardwired to 040100xxH to specify an audio multimedia device. The xx will change with each revision.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								REVISION ID							
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASE CLASS CODE								SUB-CLASS							

Latency Timer

Read/Write Address: 0DH
Power-On Default: 00H

7	6	5	4	3	2	1	0
BM LATENCY TIMER					0	0	0

Bits 2-0 Reserved = 0

These are the 3 lsb's of the latency timer value, providing 8 clocks granularity.

Bits 7-3 BM LATENCY TIMER - Bus Master Latency Timer

Value = number of PCI clocks the SonicVibes can keep its bus master grant without having it removed

These are the 5 msb's of this value. The three lsb's are 000b. This value is normally programmed by the system BIOS based in part on the requested value in bits 15-8 of 3EH.

Games Compatible Base Address Register

See Bit Descriptions Address: 12H (high) 10H (low)
Power-On Default: 0000 0001H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GAMES COMPATIBLE BASE ADDRESS												R=0	R = 0	R = 0	I=1
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
GAMES COMPATIBLE BASE ADDRESS															

Bit 0 I - I/O Space Indicator (Read Only)

value = 1 (base registers map into I/O space) (hardwired)

Bits 3–1 Reserved = 0 (Read Only)

These bits are hardwired to 0 to specify that the games compatible registers require 16 bytes of I/O space.

Bits 31–4 GAMES COMPATIBLE BASE ADDRESS

Value = upper 28 bits of the I/O base address for accessing games compatible registers

To maintain backwards compatibility, this should be programmed according to the Sound Blaster Pro *de facto* standard.

Enhanced Mode Base Address Register

See Bit Descriptions Address: 16H (high) 14H (low)
Power-On Default: 0000 0001H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENHANCED MODE BASE ADDRESS												R=0	R = 0	R = 0	I=1
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ENHANCED MODE BASE ADDRESS															

Bit 0 I - I/O Space Indicator (Read Only)

value = 1 (base registers map into I/O space) (hardwired)

Bits 2–1 Reserved = 0 (Read Only)

These bits are hardwired to 0 to specify that the enhanced mode registers require 16 bytes of I/O space.

Bits 31–4 ENHANCED MODE BASE ADDRESS

Value = upper 28 bits of the I/O base address for accessing enhanced mode registers

FM Synthesis Base Address Register

See Bit Descriptions Address: 1AH (high) 18H (low)
Power-On Default: 0000 0001H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FM SYNTHESIZER BASE ADDRESS														R=0	I=1
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FM SYNTHESIZER BASE ADDRESS															

Bit 0 I - I/O Space Indicator (Read Only)

value = 1 (base registers map into I/O space) (hardwired)

Bit 1 Reserved = 0 (Read Only)

This bit is hardwired to 0 to specify that the FM synthesis registers require 4 bytes of I/O space.

Bits 31–2 FM SYNTHESIS BASE ADDRESS

Value = upper 30 bits of the I/O base address for accessing FM synthesis registers

To maintain backwards compatibility, this should be programmed according to the AdLib *de facto* standard.

MIDI Base Address Register

See Bit Descriptions Address: 1EH (high) 1CH (low)
Power-On Default: 0000 0001H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIDI BASE ADDRESS														R=0	I=1
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MIDI BASE ADDRESS															

Bit 0 I - I/O Space Indicator (Read Only)

value = 1 (base registers map into I/O space) (hardwired)

Bit 1 Reserved = 0 (Read Only)

This bit is hardwired to 0 to specify that the MIDI registers require 4 bytes of I/O space.

Bits 31–2 MIDI BASE ADDRESS

Value = upper 30 bits of the I/O base address for accessing MIDI registers

To maintain backwards compatibility with applications directly accessing the MPU-401, this should be programmed according to that *de facto* standard.

Game Port Base Address Register

See Bit Descriptions Address: 22H (high) 20H (low)
Power-On Default: 0000 0001H

15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GAME PORT BASE ADDRESS													R=0	R=0	I=1
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
GAME PORT BASE ADDRESS															

Bit 0 I - I/O Space Indicator (Read Only)

value = 1 (base registers map into I/O space) (hardwired)

Bits 2-1 Reserved = 0 (Read Only)

These bits are hardwired to 0 to specify that the game port registers require 8 bytes of I/O space.

Bits 31–3 GAME PORT BASE ADDRESS

Value = upper 29 bits of the I/O base address for accessing game port registers

To maintain backwards compatibility with applications directly accessing the Game Port, this should be programmed according to that *de facto* standard.

PCI Configuration Space Subsystem ID

Read/Write Address: 2CH
Power-On Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUBSYSTEM VENDOR ID															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SUBSYSTEM ID															

Bits 15-0 SUBSYSTEM VENDOR ID

Bits 31-16 SUBSYSTEM ID

Interrupt Line Register

Read/Write Address: 3CH
Power-On Default: 00H

This register contains interrupt line routing information written by the POST program during power-on initialization.

7	6	5	4	3	2	1	0
INTERRUPT LINE							

Bits 7–0 INTERRUPT LINE

Interrupt Pin Register

Read Only Address: 3DH
Power-On Default: 01H

This register specifies that $\overline{\text{INTA}}$ is the interrupt pin used.

7	6	5	4	3	2	1	0
INTERRUPT PIN							

Bits 7–0 INTERRUPT PIN
value = 01H (hardwired)

Latency/Grant

Read Only Address: 3EH
Power-On Default: 0000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAXIMUM LATENCY								MINIMUM GRANT							

Bits 7–0 MINIMUM GRANT

Value = Length of burst period required in units of 250 ns (33 MHz clock)

Bits 15–8 MAXIMUM LATENCY

Value = Maximum latency of PCI access in units of 250 ns (33 MHz clock)

DMA_A Configuration Register

See Bit Descriptions Address: 42H (high) 40H (low)
Power-On Default: 0000 0000H

This playback DMA channel provides full ISA (legacy) compatibility.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA_A BASE ADDRESS												EA	TS		CE
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DMA_A BASE ADDRESS															

Bit 0 CE = Channel Enable
0 = Disable DMA_A
1 = Enable DMA_A

Bits 2-1 TS - Transfer Size (Read Only)

These bits are hardwired to 00b (8-bit transfers)

Bit 3 EA - Extended Addressing (non-legacy)
0 = Disabled (DMA address 31:24 = 00H; base count 23-16 = 00H)
1 = Enabled

Bits 31-4 DMA_A BASE ADDRESS

Value = I/O base address for DMA_A channel

DMA_C Configuration Register

Read/Write Address: 4AH (high) 48H (low)
Power-On Default: 0000 0000H

This record DMA channel does not provide full ISA (legacy) compatibility.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DCA_C BASE ADDRESS												R	R	R	CE
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DMA_C BASE ADDRESS															

Bit 0 CE = Channel Enable
0 = Disable DMA_A
1 = Enable DMA_A

Bits 3-1 Reserved

Bits 31-4 DMA_C BASE ADDRESS

Value = I/O base address for DMA_C channel

Reserved Register

Read/Write Address: 50H
Power-On Default: 0001 0000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R=1

Bits 31–0 Reserved

Wavetable Memory Base Address Register

Read/Write Address: 62H (high) 60H (low)
Power-On Default: 0000 0000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WT BASE															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	WT BASE			

Bits 19-0 WT BASE

Value = Base address in system memory of wavetable data

Bits 31-20 Reserved

Appendix A: Clock Synthesis and Power Management

SonicVibes contains two phase-locked loop (PLL) frequency synthesizers. These generate the clocks for the ADC and music synthesizer. The programming model is the same for both.

A.1 CLOCK SYNTHESIS

The PLL scales a single reference frequency input on the XIN pin. By placing a parallel-resonant crystal between the XOUT output pin and the XIN pin, the reference frequency is generated by the SonicVibes' internal oscillator. Alternately, a CMOS-compatible clock input can be connected to XIN to provide the reference frequency.

The frequency synthesized by the PLL is determined by the following equation:

$$f_{OUT} = \frac{(M+2)}{(N+2)\times 2^R} \times f_{REF}$$

where R = 0 to 7

Programmed PLL M and PLL N values should be consistent with the following constraints:

1. $80MHz \le \frac{(M+2)f_{REF}}{(N+2)} \le 150MHz$

2. min N $\ge$ 1

Note that values used for the parameters are the integer equivalents of the programmed value. In particular, the R value is the code, not the actual frequency divisor.

The PLL M value can be programmed with any integer value from 1 to 255. The binary equivalent of this value is programmed in bits 7-0 of CMX24 for the ADC PLL and CMX26 for the synthesizer PLL. The PLL feedback loop frequency from the voltage controlled oscillator stage is scaled by dividing that frequency by (M+2).

The PLL N value can be programmed with any integer value from 1 to 31. The binary equivalent of this value is programmed in bits 4-0 of CMX25 for the ADC PLL and CMX27 for the synthesizer PLL. The reference frequency is divided by (N+2) before being fed to the phase detector stage of the PLL.

The PLL R value is a 3-bit range value that can be programmed with any integer value from 0 to 7. The R value is programmed in bits 7-5 of CMX25 for the ADC PLL and CMX27 for the synthesizer PLL. This value codes the selection of a frequency divider for the PLL output. This is shown Table A-1.

Table A-1. PLL R Parameter Decoding

R-Range Code	Frequency Divider
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

The entire PLL block diagram is shown in Figure A-2.

The following sequence may be followed to arrive at M and N values for any mode.

1. Calculate an R which does not violate the following constrains:

$$80MHz < 2^R \times f_{OUT} \leq 150MHz$$

2. Start with N1 = 1 and calculate:

$$M = [\frac{f_{OUT} \times (N+2) \times 2^R}{f_{REF}}] - 2$$

3. Determine if the following constraint is met:

$$0.995 f_{OUT} < \frac{(M+2)\ f_{REF}}{(N+2)\ 2^R} < 1.005\ f_{OUT}$$

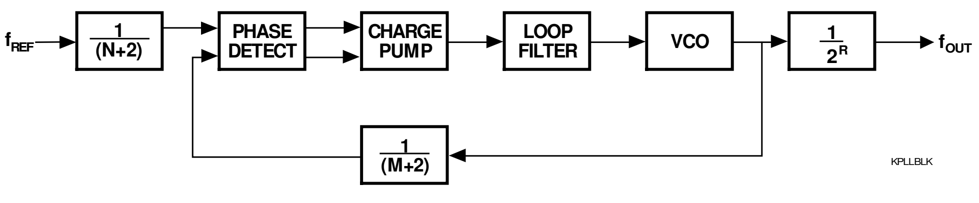

Figure A-1. PLL Block Diagram

4. If the constraint in step 3 is met, the M and N values used will generate the desired frequency (within the specified tolerance). If the constrain is not met, repeat steps 2 and 3 with N increased by 1 each time until the constraint in step 3 is met. Note that multiple combinations of M and N are possible for a given output frequency.

SonicVibes powers up with an ADC PLL frequency of 11.289 MHz. The power-on default for the synthesizer PLL is 50 MHz. If either is to be reprogrammed, the new M value must be programmed first. The N and R values must be programmed next (back to back), upon which the new M, N and R values will be updated simultaneously.

When SonicVibes is in test mode (TESTEN pin pulled down), the ADC clock is output on pin 122 and the synthesizer clock is output on pin 119.

A.2 POWER MANAGEMENT

SonicVibes provides extensive power management capabilities. CMX30 provides control over the power of six analog blocks. Several bits in this register have notes specifying that certain functions must be muted before power down to prevent audible clicks. CMX31 provide control over the power to four digital blocks.

SonicVibes Audio Accelerator

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