ARM Cortex-A8 Processor

High Performances And Low Power for Portable Applications

Architectures for Multimedia Systems
Prof. Cristina Silvano

Gianfranco Longi
Matr. 712351

ARM Partners

ARM Powered Products

Evolution of ARM architecture

- Original ARM architecture:
  - 32 bit RISC architecture
  - 16 registers (1 being the PC)
  - 4-bit condition code of most instructions (compensates for the lack of a branch predictor)
  - save and restore blocks of registers on function call/return in one cycle
  - Shift available on data processing and address generation
- Thumb Instruction was the next big step
  - Introduced in the ARMv4T architecture (ARM7TDMI)
  - Present a 16 bit instruction set alongside the 32 bit instruction set (but Thumb still processes 32-bit data)
  - Only branches can be conditional and many opcodes cannot access all CPU registers
  - Better performance in situations where memory port or bus is constrained to less than 32 bits (Game Boy Advance)
  - Not a full instruction set… ARM still essential!

ARM

Evolution of ARM architecture (2)

- ARMv5TEJ (ARM926EJ-S) introduced:
  - Better interworking between ARM and Thumb
  - additional istructions focused on DSP
  - **Jazelle-DBX** for Java bytecode interpretation in hardware

- ARMv6 (ARM1136JF-S) introduced:
  - Media processing – **SIMD** within the integer datapath
  - Enhanced exception handling
  - Revision of the memory system architecture

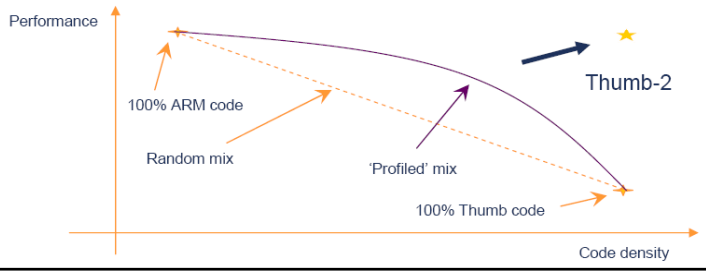
- ARMv7 introduces several important changes:
  - **Thumb-2**
  - **TrustZone**
  - **Jazelle-RCT** → Complementary to Jazelle DBX on mid-tier devices
  - **Neon**
  - ARMv7 split into 3 profiles (Portable Applications, Real time Systems and Microcontrollers)

Thumb-2

Strong limitation of Thumb: Not all ARM instructions have Thumb equivalents, so some ARM instructions must still be used even when the target is the highest code density.

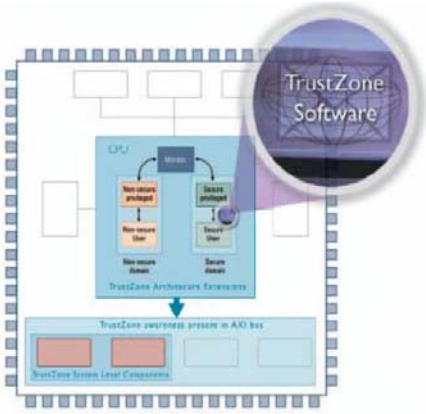
Idea: "*Thumb density at ARM performance*"… but How ???

Thumb-2 = Thumb 16 bit original instructions augmented by
• New 16-bit Thumb instructions for improved program flow
• New 32-bit Thumb instructions derived from ARM instruction equivalents
• Addition of new 32-bit ARM instructions for improved performance and data handling



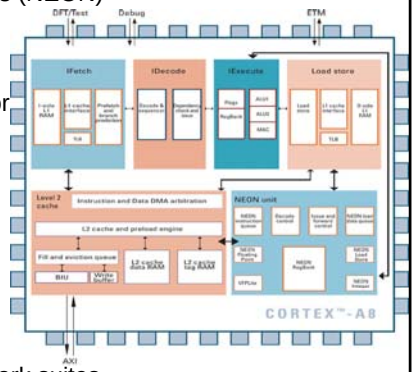
TrustZone Technology

- Architectural extensions to introduce a "Security" state
  - Orthogonal to User/Privileged split
- Effectively two virtual CPUs separated by a new mode
  - Some hardware registers duplicated to aid switching
- Memory tagged as secure and non-secure by the system
  - Only the secure CPU can access the secure memory & peripherals
  - System can include secure and non-secure peripherals

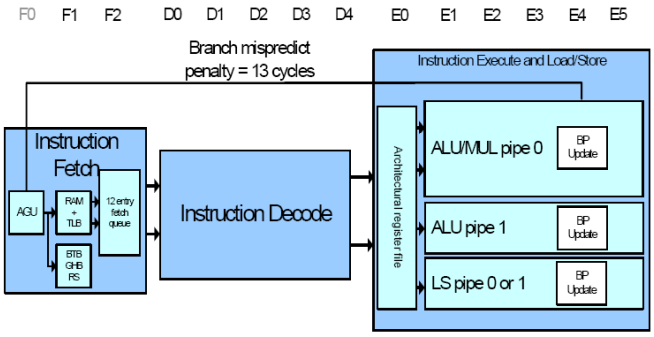


Cortex-A8 Processor Highlights

- First implementation of the ARMv7 instruction set architecture (and **all** its innovations) including the Advanced SIMD media instructions (NEON)
- In-order, dual-issue, superscalar microprocessor core
  - 13-stages integer pipeline
  - 10-stages NEON media pipeline
  - Branch prediction based on global history
- Performances
  - delivers 2000 DMIPS
  - average IPC of 0.9 across multiple benchmark suites
  - achieves 1GHz when fabricated in high-performance technologies
  - consumes less than 300mW in low-power devices
  - less than 4mm^2 at 65nm, excluding NEON, L2 cache, and Embedded Trace



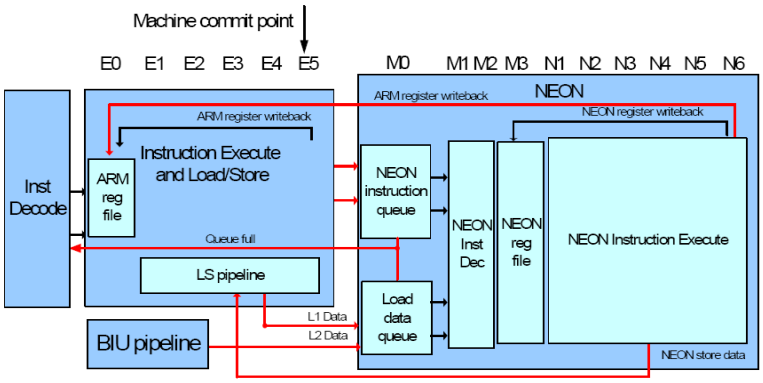
Cortex-A8 Integer Pipeline



- First ARM processor with dual integer execution pipeline
  - In-order issue to keep additional power required to a minimum. Out-of-order issue and retire can require extensive amounts of logic consuming extra power
- Dinamic branch predictor components
  - 512-entry BTB
  - 4k-2 bits saturating counter entry GHB indexed by branch history(a BHR of 10-bit) and (last 4 bits of) PC
  - All branches are resolved in single stage

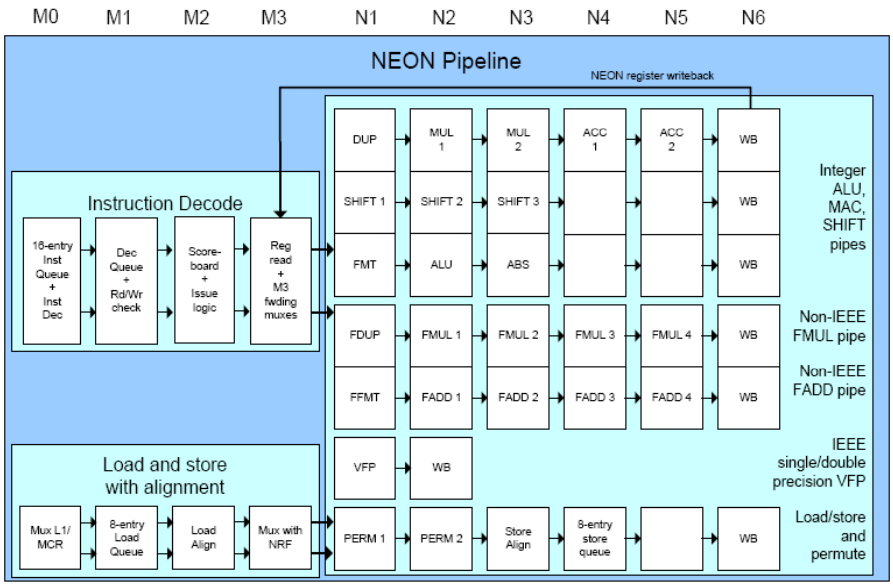
→ *High frequency design with out-of-order performance, but in-order clock frequency and power consumption*

NEON Media Engine Pipeline

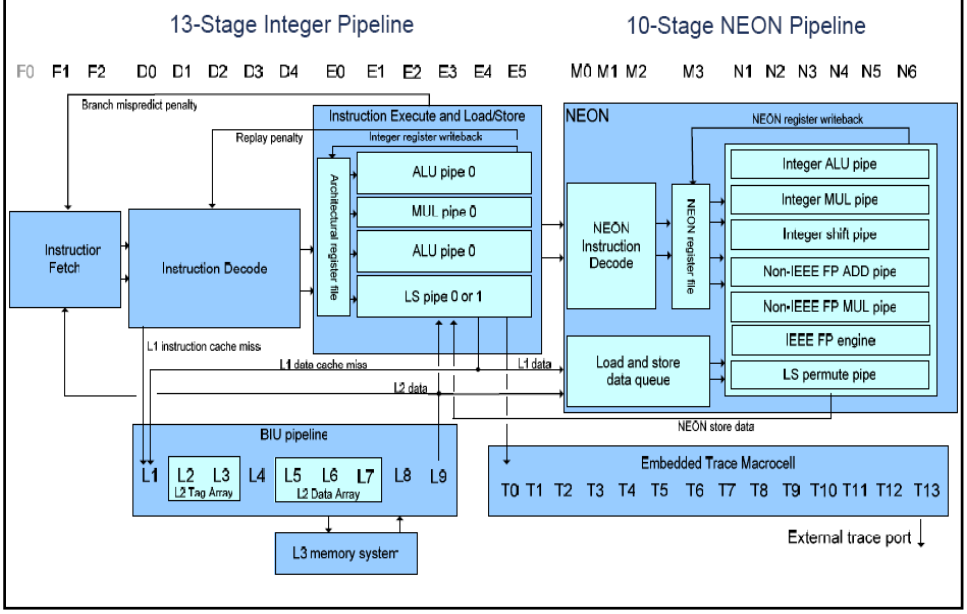


- Separate SIMD execution pipeline and register file with shared access to L1 and L2 memory
- 10-stage pipeline begins at the end of the main integer pipeline (NIQ)
- No exceptions in NEON pipeline (all mispredicts and exceptions have been resolved in the ARM integer unit)
- Zero load-use penalty for data in the L1-Cache (the integer unit generates the addresses for NEON loads and stores as they pass through the pipeline, thus allowing data to be fetched from the Level-1 cache before it is required by a NEON data processing operation)

NEON Media Engine Pipeline (2)



Full Cortex-A8 Pipeline

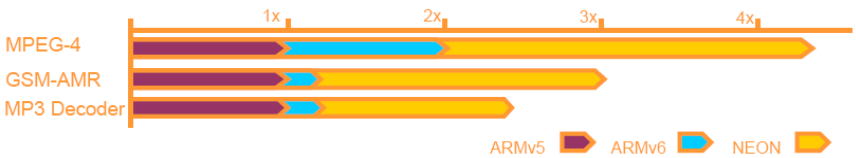


Memory System on Cortex-A8

- Single-cycle load-use penalty for fast access to the Level-1 caches
- The data and instruction Level-1 caches are configurable to 16k or 32k. Each is 4-way set associative and uses a **Hash Virtual Address Buffer (HVAB)** way prediction scheme to improve timing and reduce power consumption. Write-back with write no allocate replecement policy + write buffer for faster writes in memory
- The Level-2 cache is a unified data and instruction 8-way set associative cache, that can be configured in size from 64K to 2M.
- The tag and data RAMs of the Level-2 cache are accessed serially for power savings.
- Data caches are multilevel exclusive, whereas instruction caches are multilevel inclusive.

Conclusion

- The Cortex-A8 processor is the fastest, most power-efficient microprocessor yet developed by ARM
- Ability to decode VGA H.264 video in under 350MHz
- Provides the media processing power required for next generation products while consuming less than 300mW in 65nm technologies
- Thumb-2 instructions provide code density while maintaining the performance of standard ARM code
- Jazelle RCT technology does likewise for runtime compilers
- TrustZone technology provides security for sensitive data and DRM



Video, 30fps VGA decode	
MPEG-4 including de-ring and de-block filters, yuv2rgb[1]	275MHz
H.264 (estimated)[4]	350MHz
GSM-AMR, worst case[2]	13MHz
MP3 decode, 320kbps 48kHz, worst case[3]	9.4MHz

1) MPEG-4 Simple Profile @ 30fps 512kbps , 133MHz SDRAM 10-1-1-1-1-1-1-1 memory, includes deblocking and deringing filters
2) MP3 Decoder @ 320kbps 48kHz (worst case), 133MHz SDRAM 10-1-1-1-1-1-1-1 memory
3) GSM-AMR (worst case), 3 cycle per word memory
4) H.264 Decoder Baseline profile

References

- arm.com/pdfs/ARM-DSP.pdf
- arm.com/pdfs/ARMv6_Architecture.pdf
- arm.com/pdfs/Thumb-2%20Core%20Technology%20Whitepaper%20-%20Final4.pdf
- iee-cambridge.org.uk/arc/seminar05/slides/RichardGrisenthwaite.pdf
- arm.com/pdfs/Tiger%20Whitepaper%20Final.pdf