

# How FreeBSD Boots: a soft-core MIPS perspective

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SRI International

SCALE x13  
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# Bluespec Extensible RISC Implementation



# MIPS64-ISA Soft-core CPU

Multi-core &  
Multi-threaded



Why BERI?





spyware

spam

phishing

info

data

security

virus alert!

virus detected

Banks lose over \$300m

Sony hackers

80 million  
customer records



malware alert!

**40 million cards compromised**



**Total damage to banks and  
retailers could exceed \$18 billion.**

**— NYTimes**

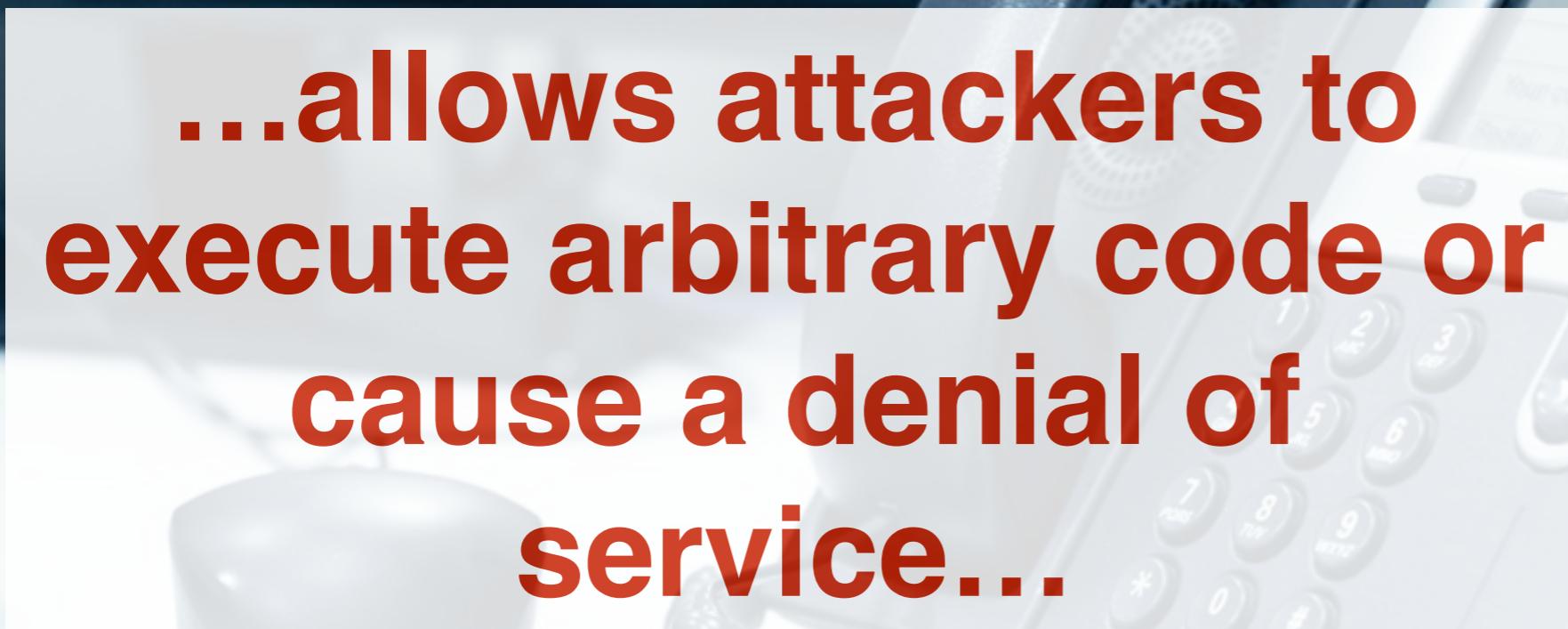




© Pete Souza | shown on platonica.com

# CVE-2012-5445:

**...allows attackers to  
execute arbitrary code or  
cause a denial of  
service...**





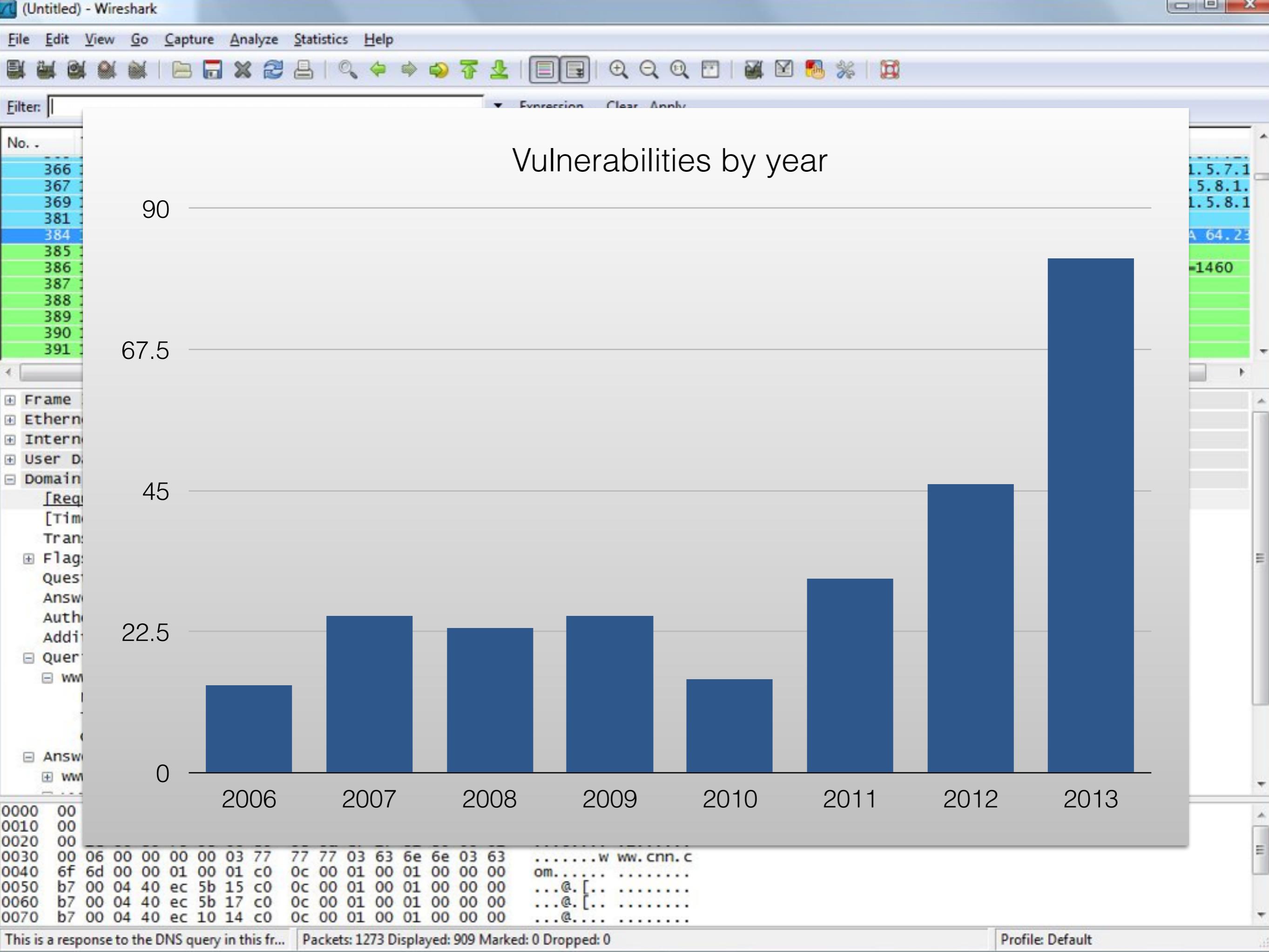
Filter:

Expression... Clear Apply

No.	Time	Source	Destination	Protocol	Info
366	11.767290	192.168.0.31	192.168.0.28	SNMP	get-response SNMPv2-SMI::enterprises.11.2.3.9.4.2.1.4.1.5.7.1
367	11.768865	192.168.0.28	192.168.0.31	SNMP	get-request SNMPv2-SMI::enterprises.11.2.3.9.4.2.1.4.1.5.8.1
369	11.775952	192.168.0.31	192.168.0.28	SNMP	get-response SNMPv2-SMI::enterprises.11.2.3.9.4.2.1.4.1.5.8.1
381	12.286091	192.168.0.28	192.168.0.1	DNS	Standard query A www.cnn.com
384	12.311862	192.168.0.1	192.168.0.28	DNS	Standard query response A 64.236.91.21 A 64.236.91.23 A 64.23
385	12.312727	192.168.0.28	64.236.91.21	TCP	56606 > http [SYN] Seq=0 Win=8192 Len=0 MSS=1460 WS=2
386	12.361495	64.236.91.21	192.168.0.28	TCP	http > 56606 [SYN, ACK] Seq=0 Ack=1 Win=8192 Len=0 MSS=1460
387	12.361583	192.168.0.28	64.236.91.21	TCP	56606 > http [ACK] Seq=1 Ack=1 Win=17520 Len=0
388	12.361805	192.168.0.28	64.236.91.21	HTTP	GET / HTTP/1.1
389	12.413166	64.236.91.21	192.168.0.28	TCP	http > 56606 [ACK] Seq=1 Ack=845 Win=6960 Len=0
390	12.413611	64.236.91.21	192.168.0.28	TCP	[TCP segment of a reassembled PDU]
391	12.414386	64.236.91.21	192.168.0.28	TCP	[TCP segment of a reassembled PDU]

+ Frame 384 (167 bytes on wire, 167 bytes captured)  
 + Ethernet II, Src: Sparklan\_04:d0:9e (00:0e:8e:04:d0:9e), Dst: HonHaiPr\_26:66:a2 (00:1c:26:26:66:a2)  
 + Internet Protocol, Src: 192.168.0.1 (192.168.0.1), Dst: 192.168.0.28 (192.168.0.28)  
 + User Datagram Protocol, Src Port: domain (53), Dst Port: 62872 (62872)  
 - Domain Name System (response)  
 [Request In: 381]  
 [Time: 0.025771000 seconds]  
 Transaction ID: 0xcf1f  
 + Flags: 0x8180 (Standard query response, No error)  
 Questions: 1  
 Answer RRs: 6  
 Authority RRs: 0  
 Additional RRs: 0  
 - Queries  
 - www.cnn.com: type A, class IN  
 Name: www.cnn.com  
 Type: A (Host address)  
 class: IN (0x0001)  
 - Answers  
 + www.cnn.com: type A, class IN, addr 64.236.91.21

0000	00 1c 26 26 66 a2 00 0e	8e 04 d0 9e 08 00 45 00	. . . & f . . . . . E .
0010	00 99 00 00 40 00 40 11	b8 e6 c0 a8 00 01 c0 a8	. . . @ . @ . . . . .
0020	00 1c 00 35 f5 98 00 85	98 5a cf 1f 81 80 00 01	. . . 5 . . . . Z . . . .
0030	00 06 00 00 00 00 03 77	77 77 03 63 6e 6e 03 63	. . . . . w w w . c n n . c
0040	6f 6d 00 00 01 00 01 c0	0c 00 01 00 01 00 00 00	o m . . . . . . . . .
0050	b7 00 04 40 ec 5b 15 c0	0c 00 01 00 01 00 00 00	. . . @ [ . . . . . . . . .
0060	b7 00 04 40 ec 5b 17 c0	0c 00 01 00 01 00 00 00	. . . @ [ . . . . . . . . .
0070	b7 00 04 40 ec 10 14 c0	0c 00 01 00 01 00 00 00	. . . @ . . . . . . . . .



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Secure  
Hosts



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Capability  
Hardware  
Enhanced  
RISC  
Instructions

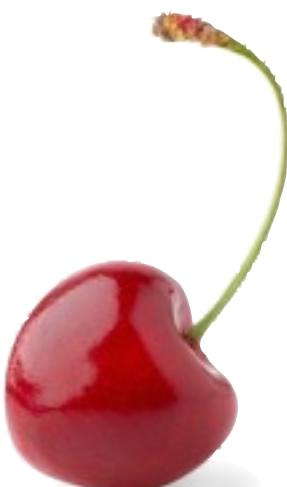


BERI

+ Memory Capabilities

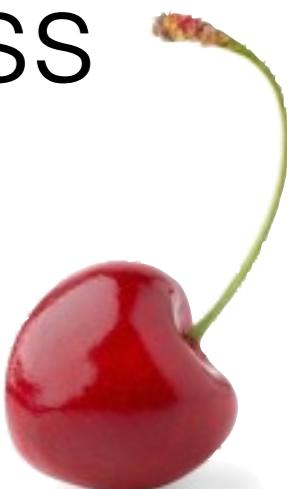
=

CHERI



# Memory Capabilities

- Unforgeable references to memory
- Implemented as a MIPS coprocessor
  - All memory access via a capability
    - Regular MIPS instructions access via a default capability



# Other **BERI** research topics

- Novel multi-threaded CPUs
- Multi-core architectures
- Tight integration of CPUs and switches
- Validation of formal models



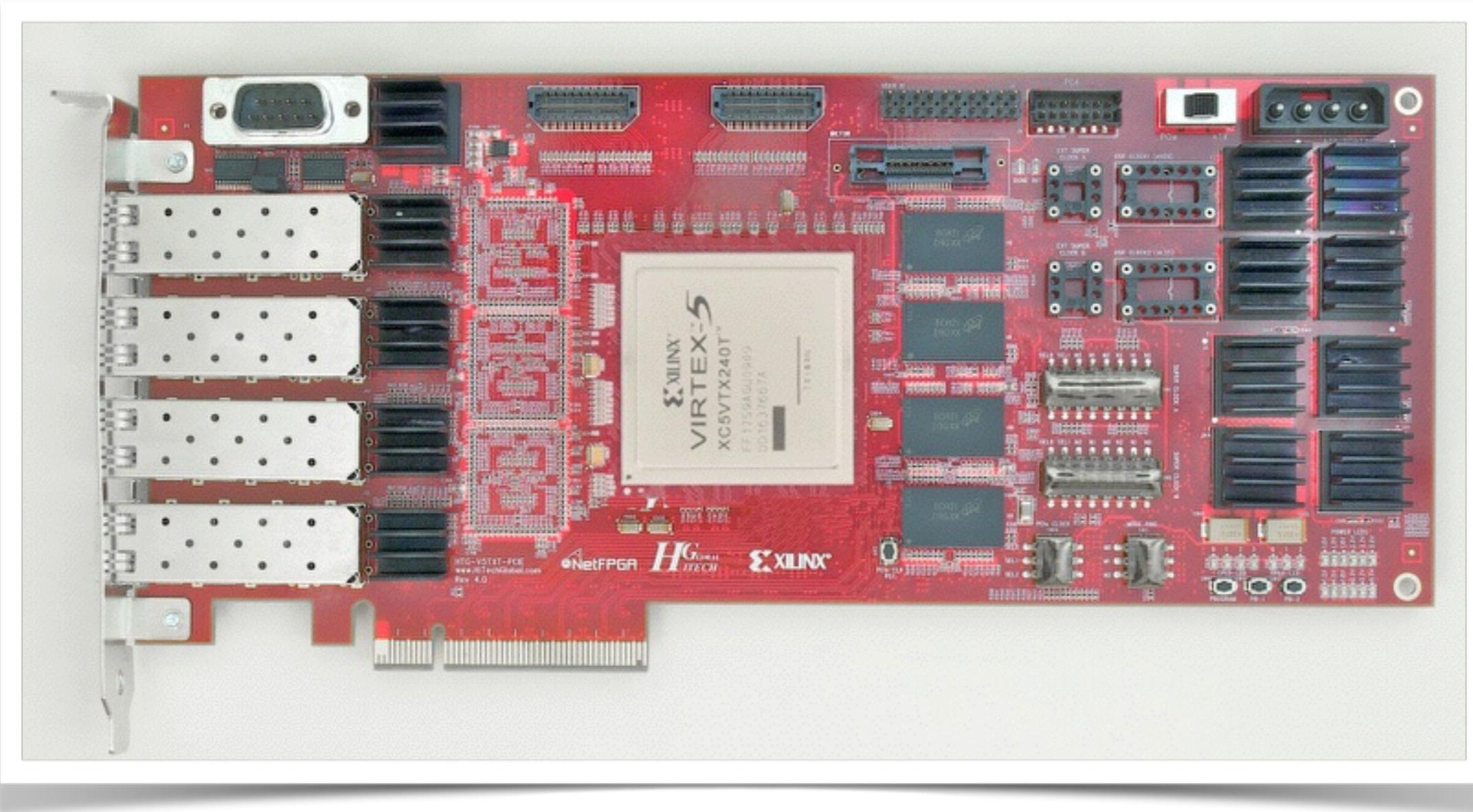
Where does BERI run?



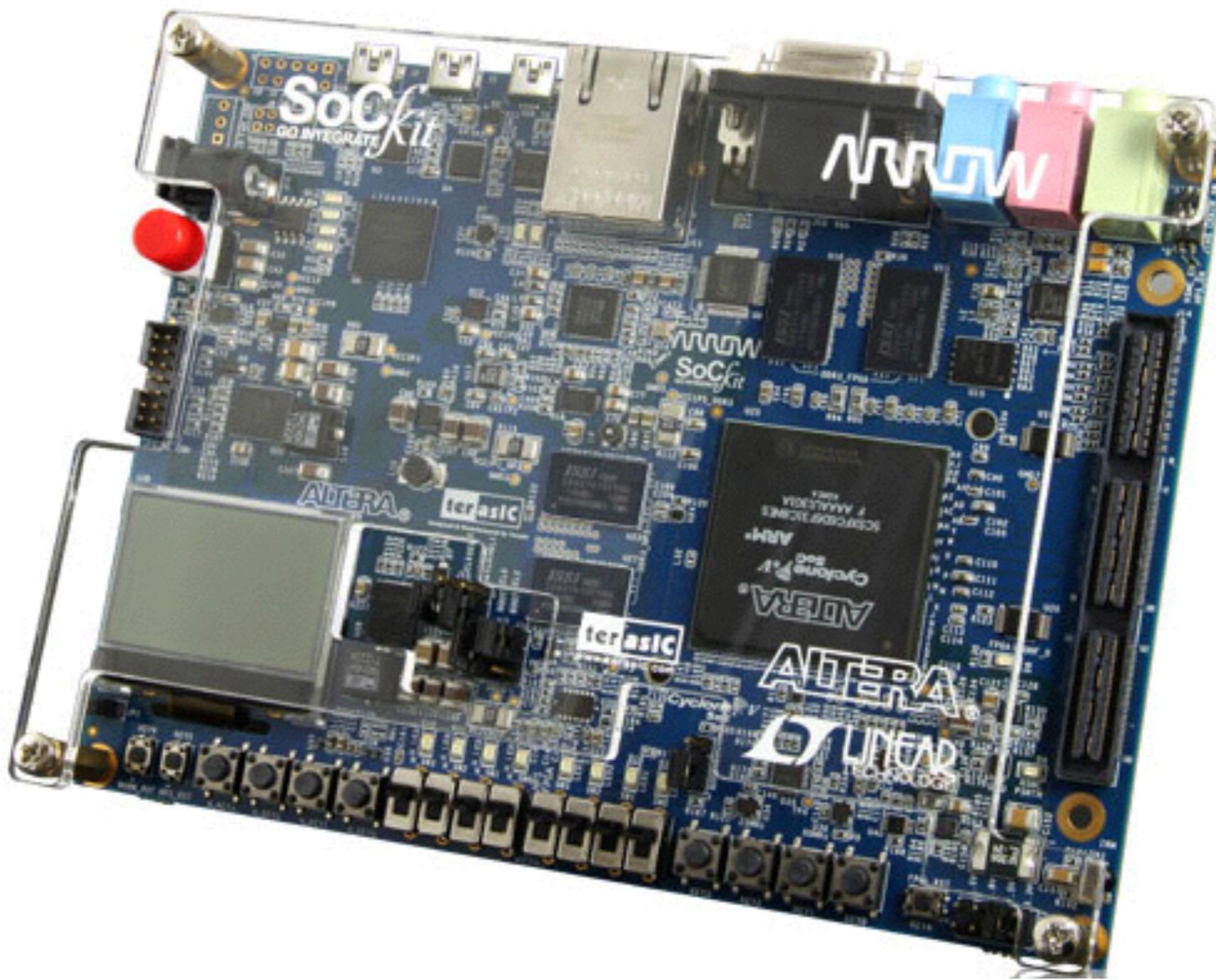
# Simulation



# NetFPGA-10G

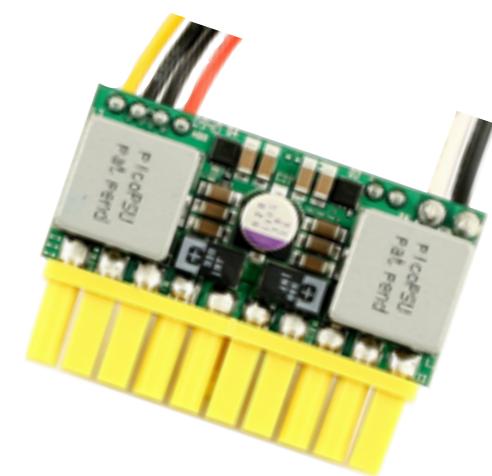


# Terasic SoCKIT



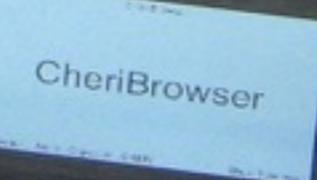
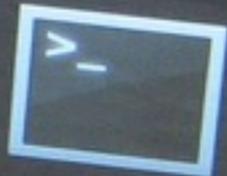
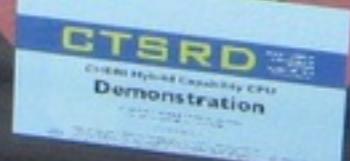
# Terasic DE4



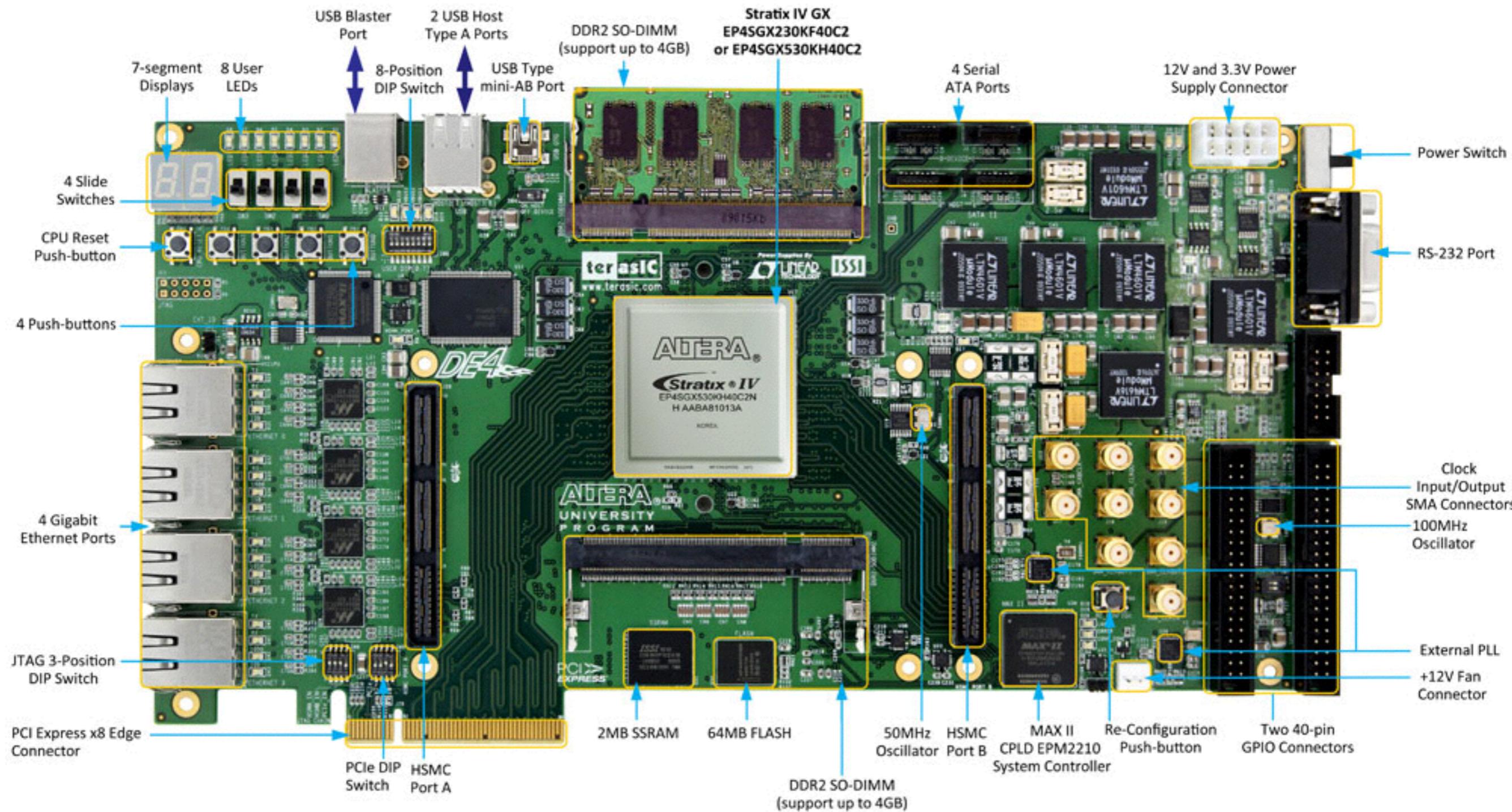


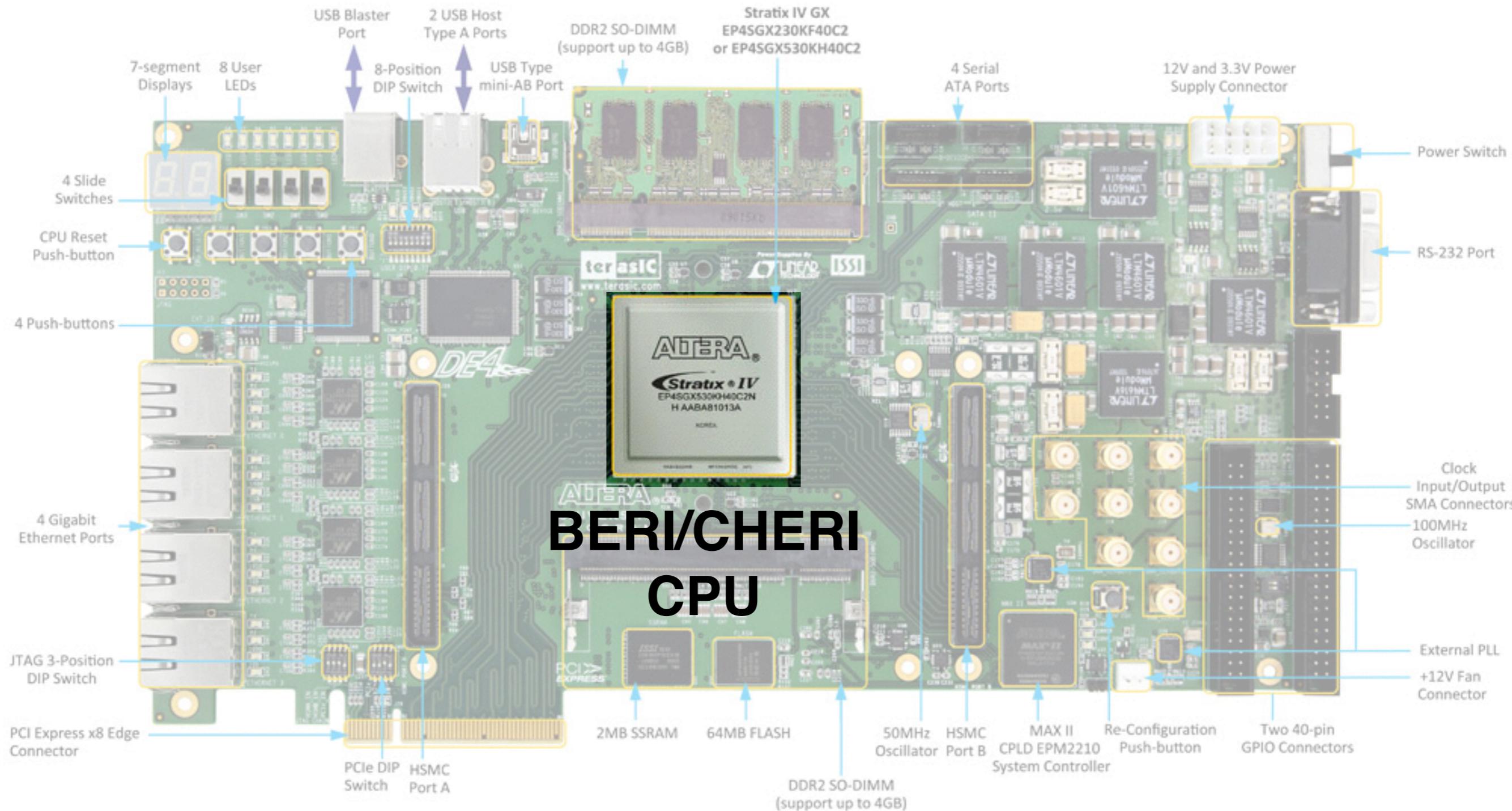


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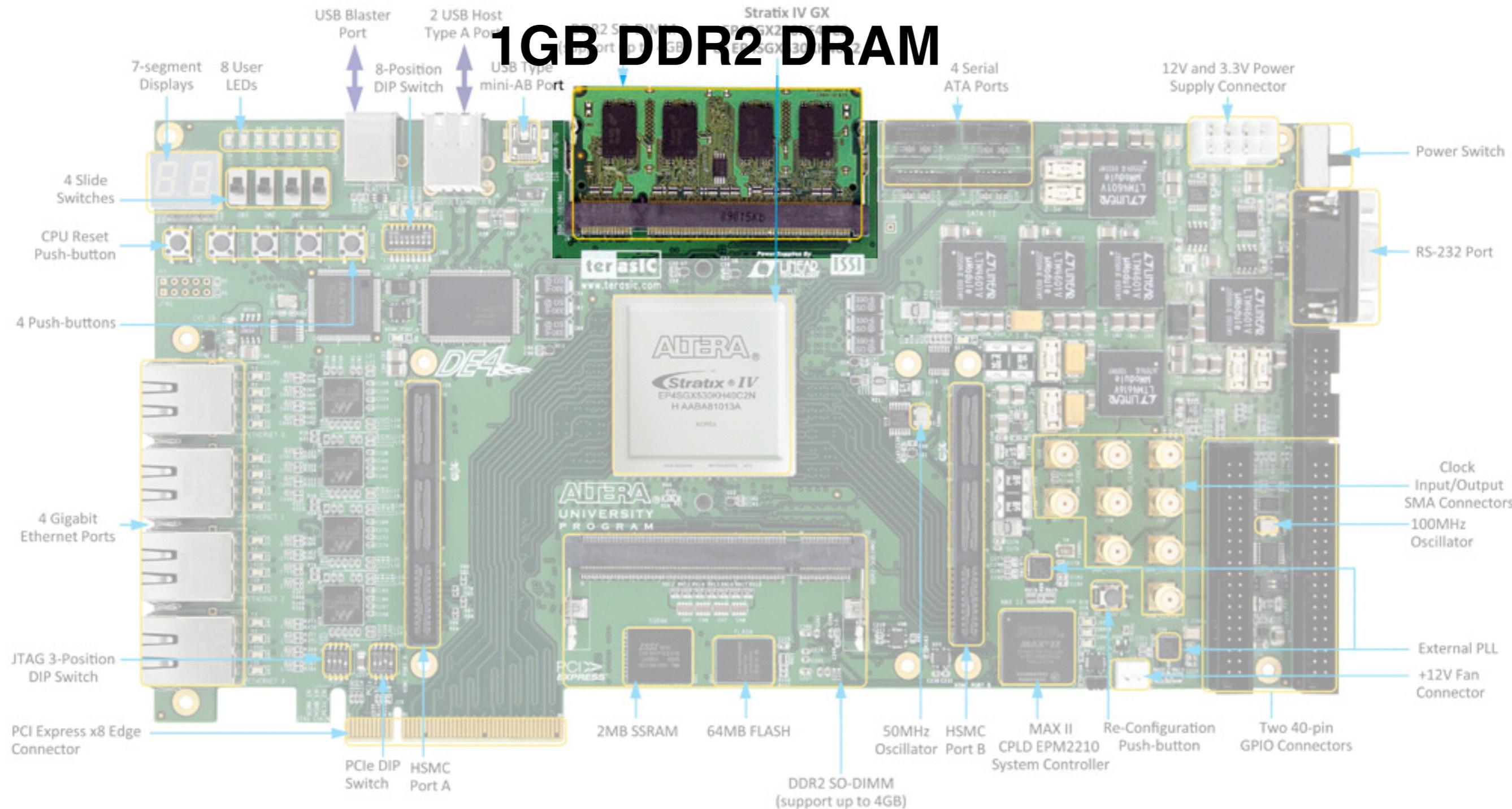


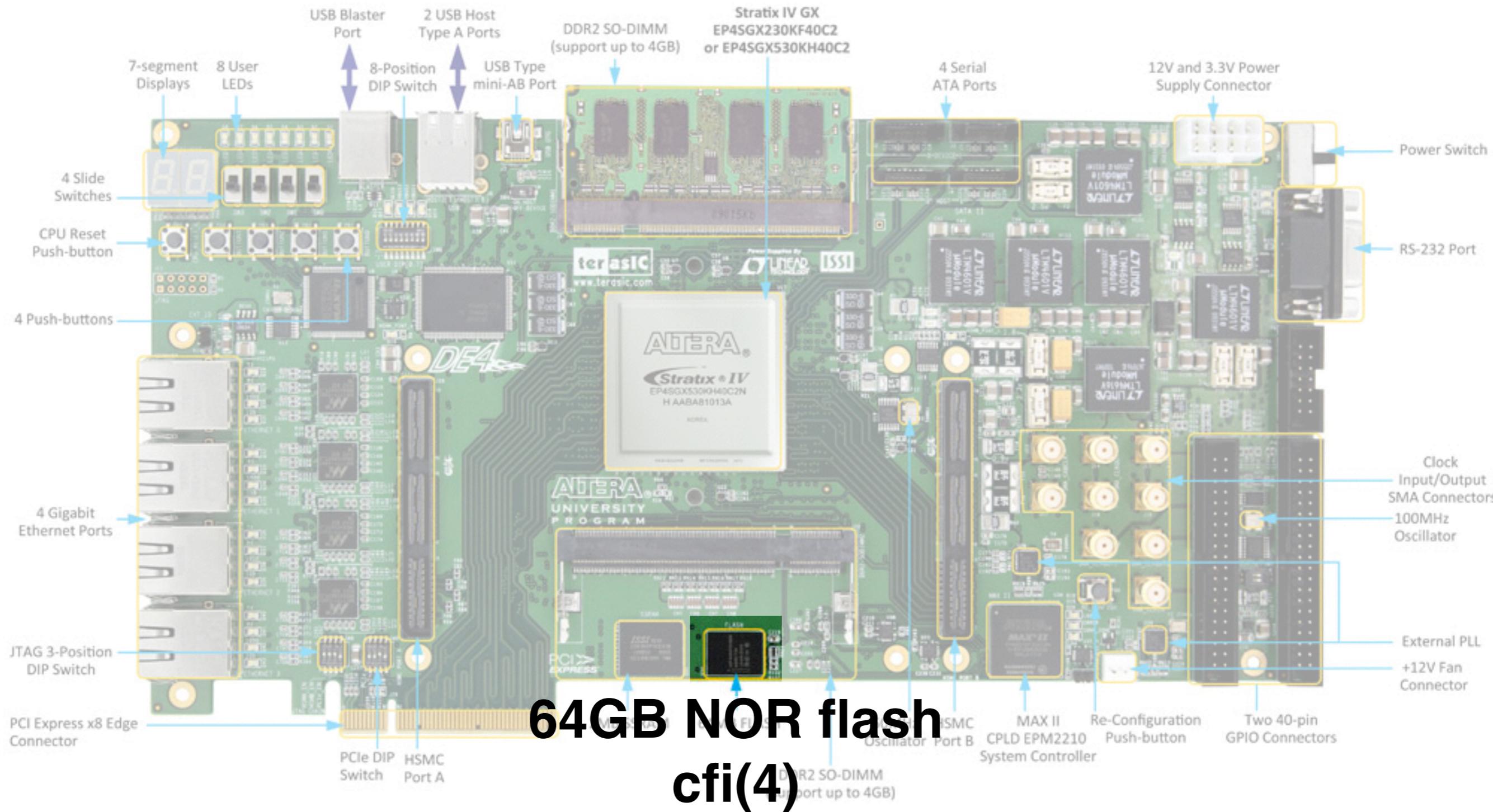
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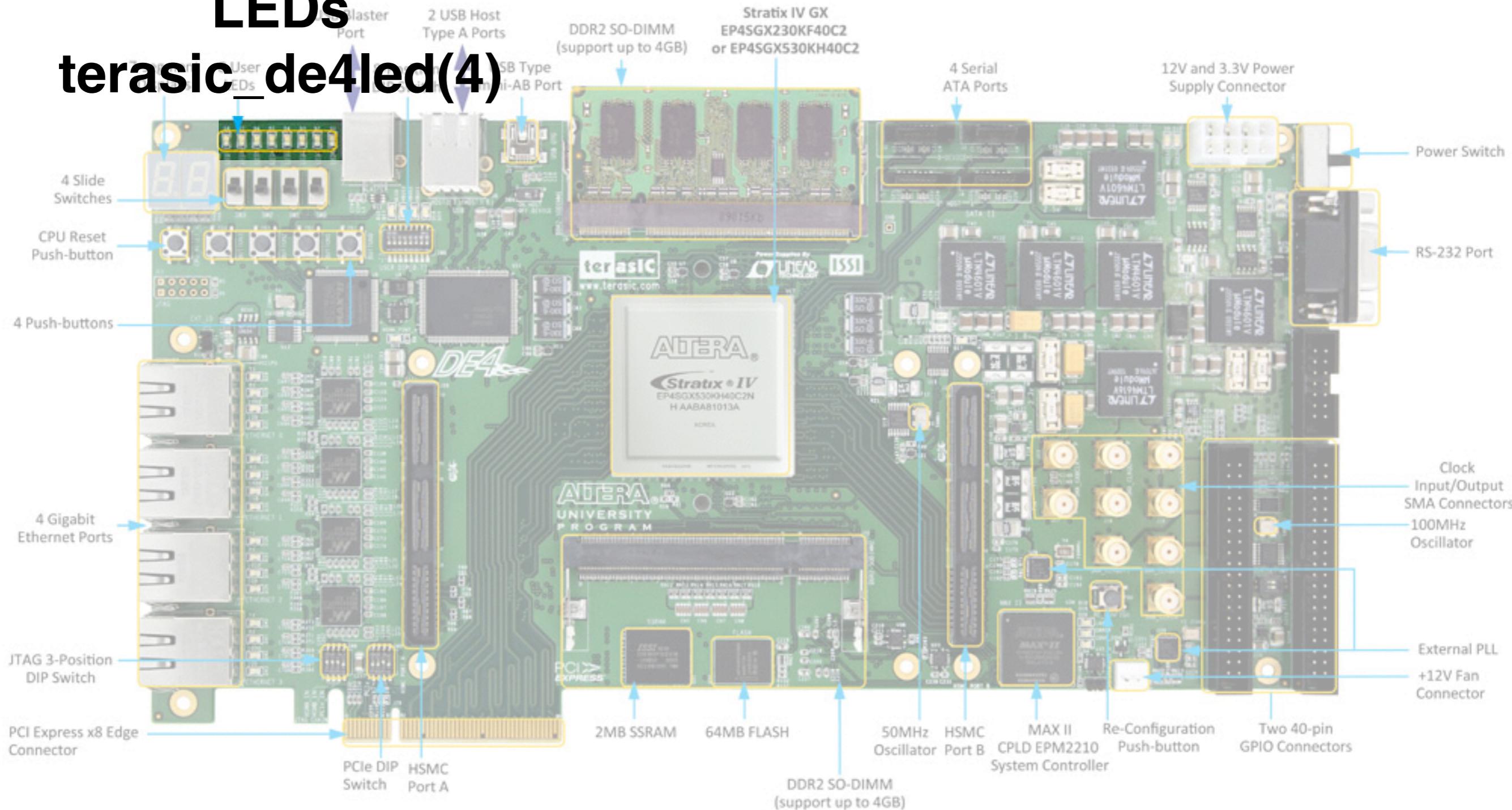


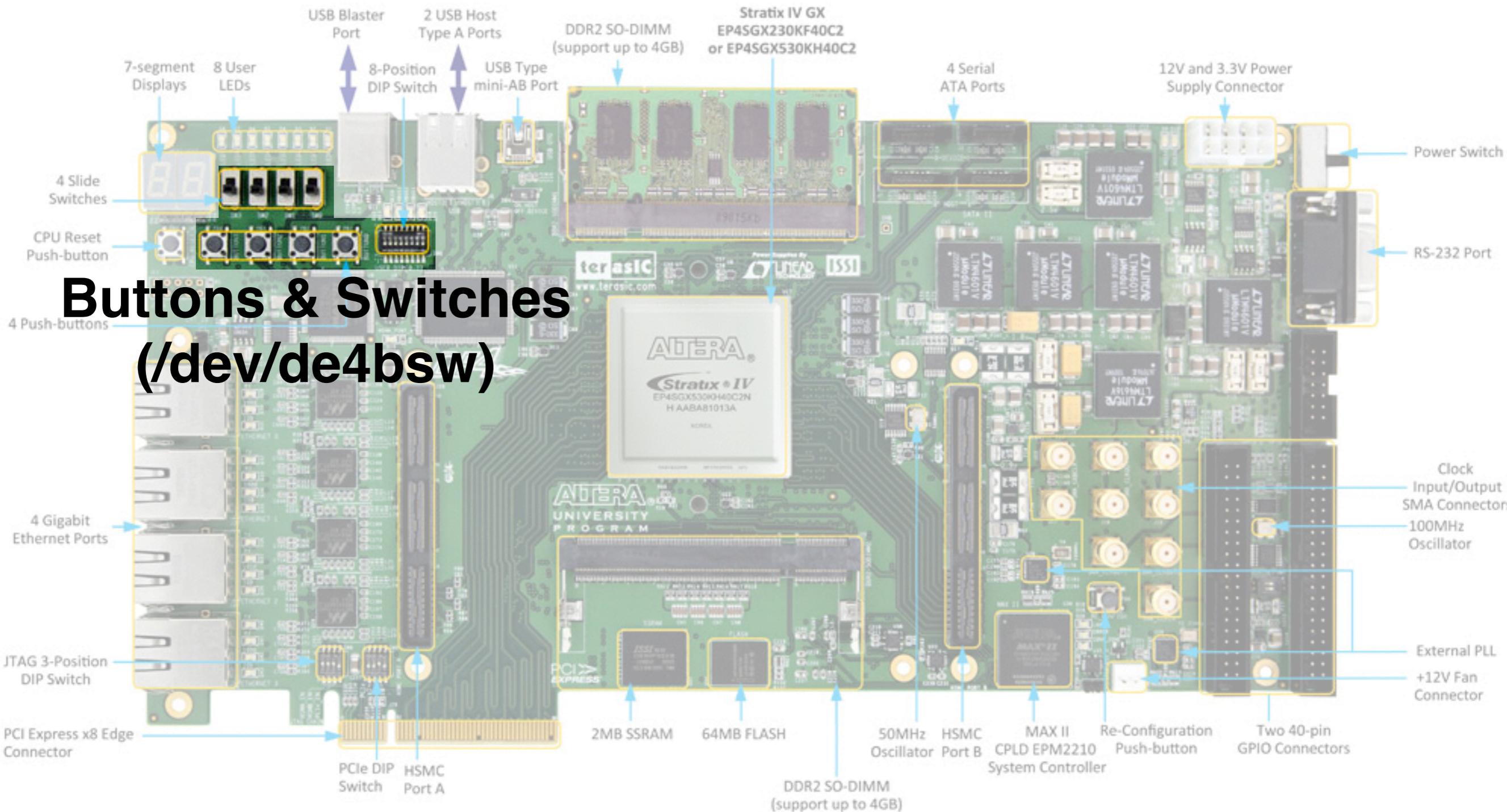
# 1GB DDR2 DRAM



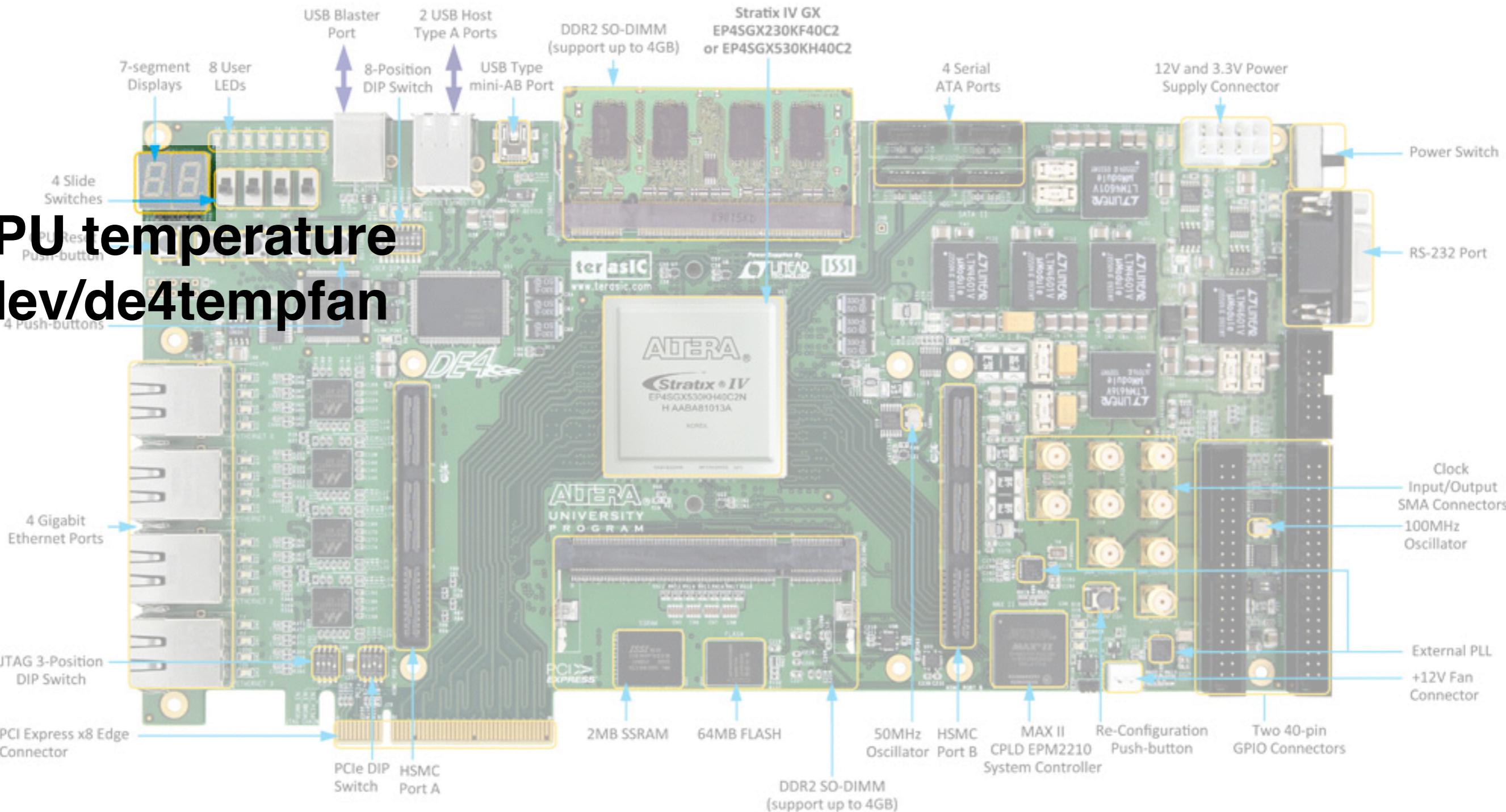


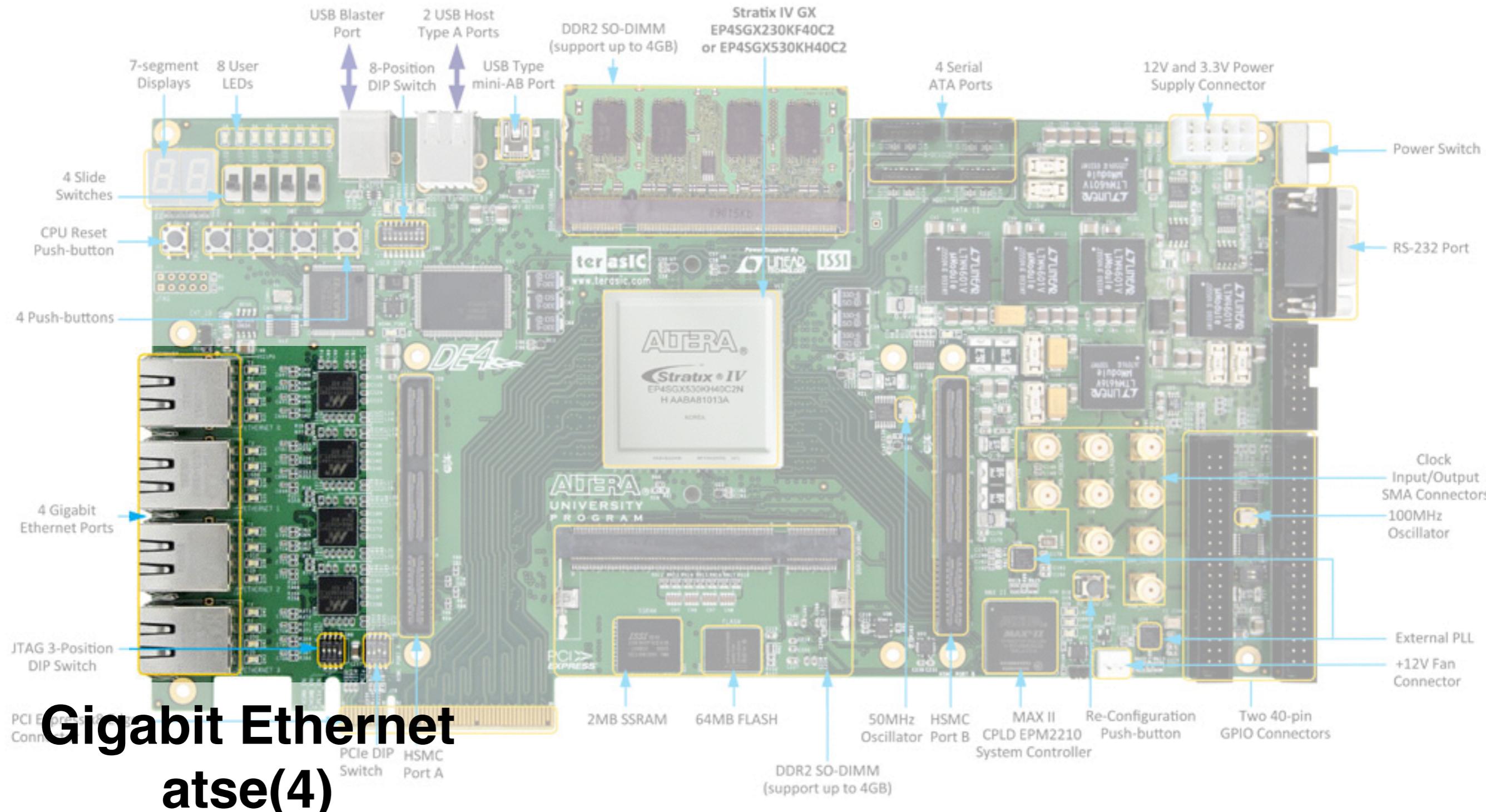
# LEDs terasic\_de4led(4)

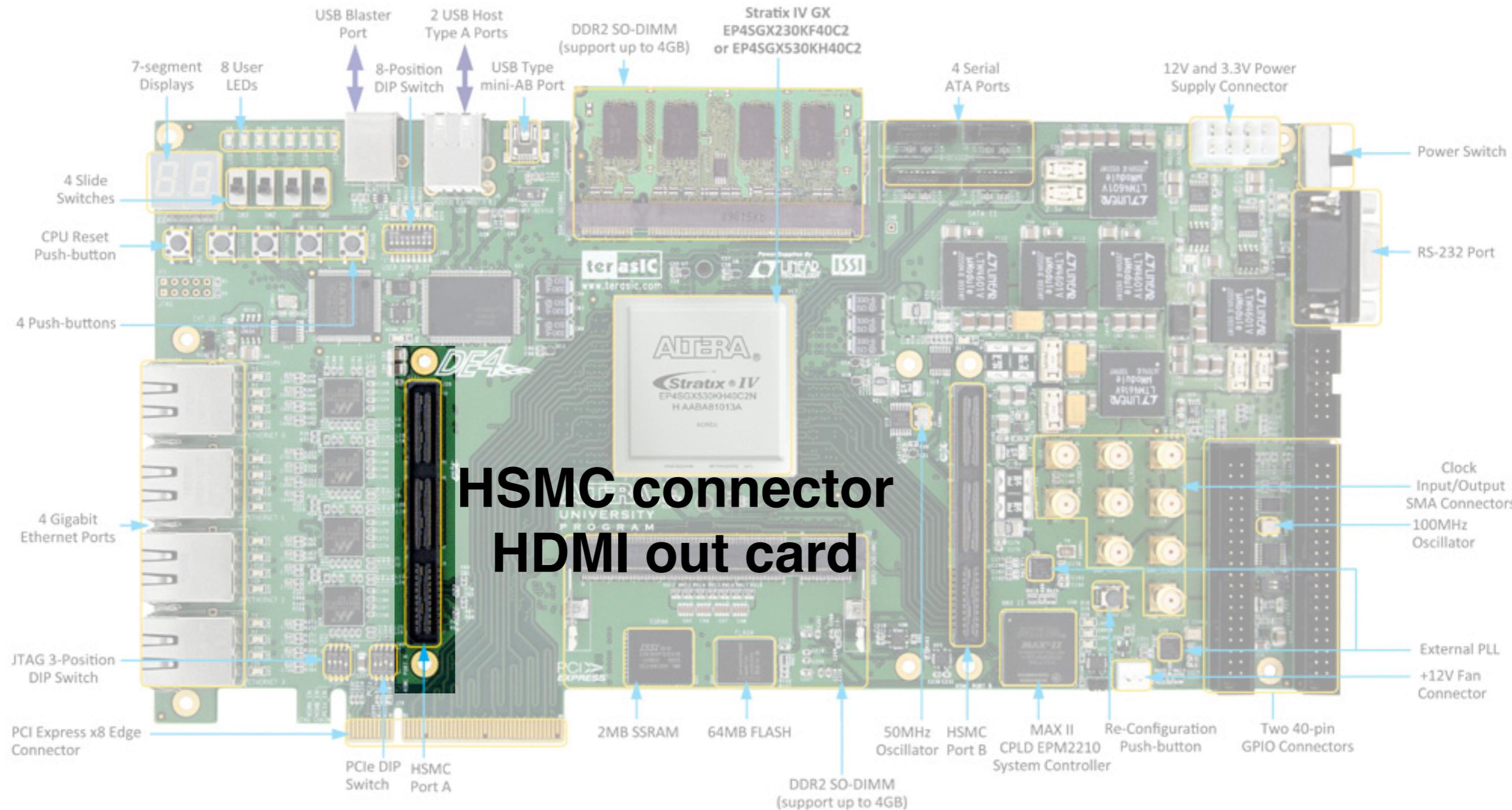


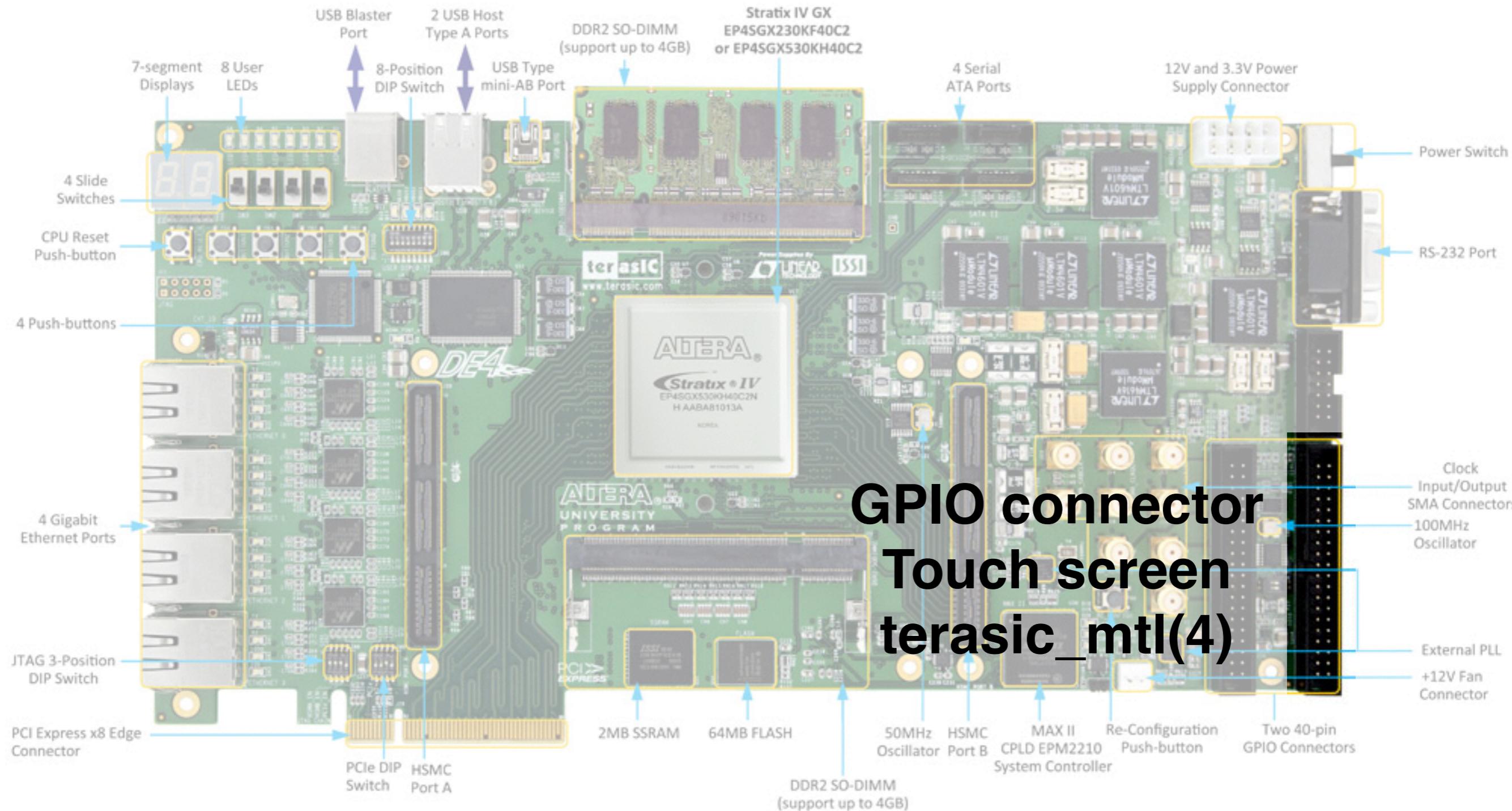


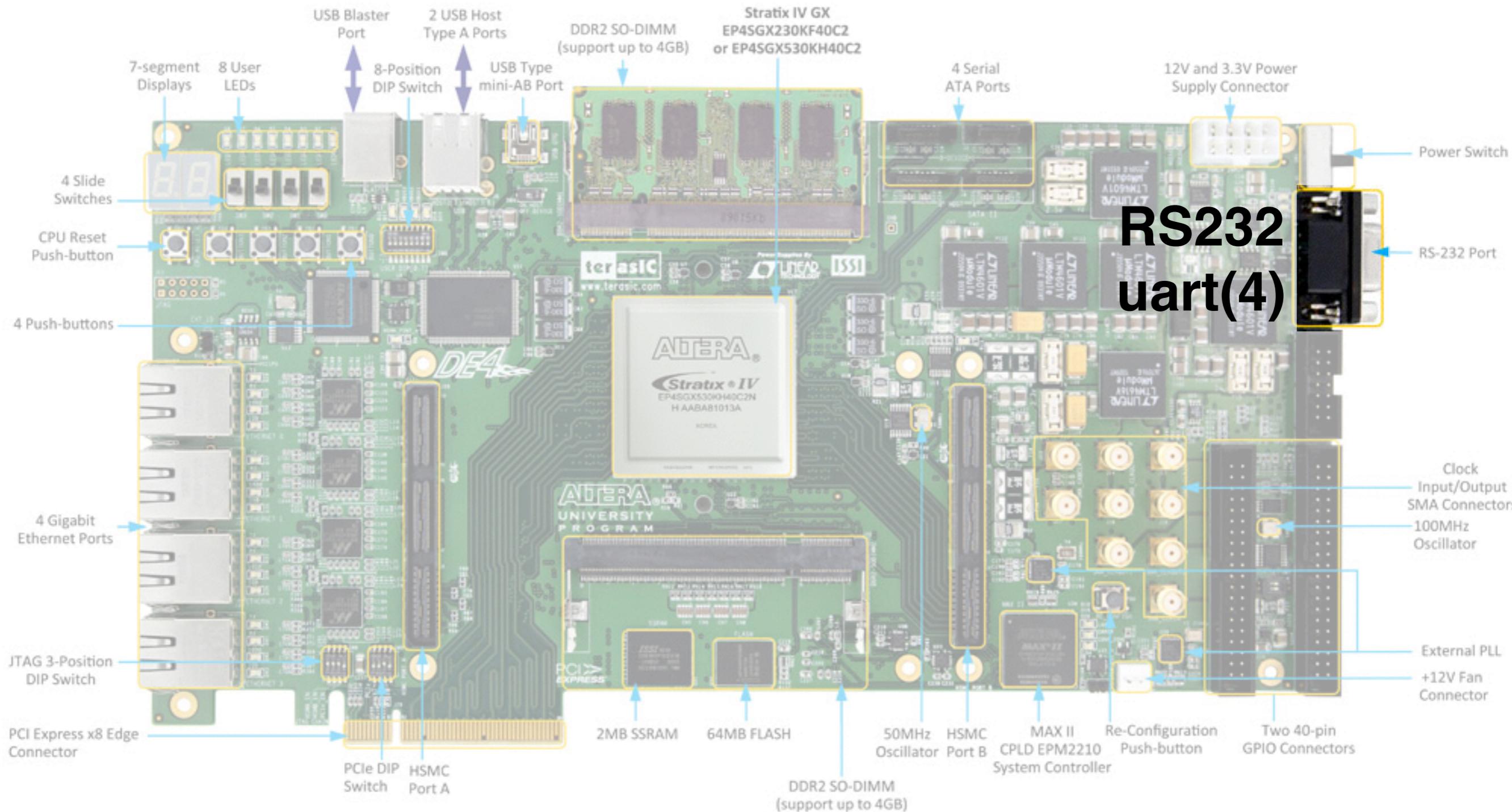
# CPU temperature `/dev/de4tempfan`

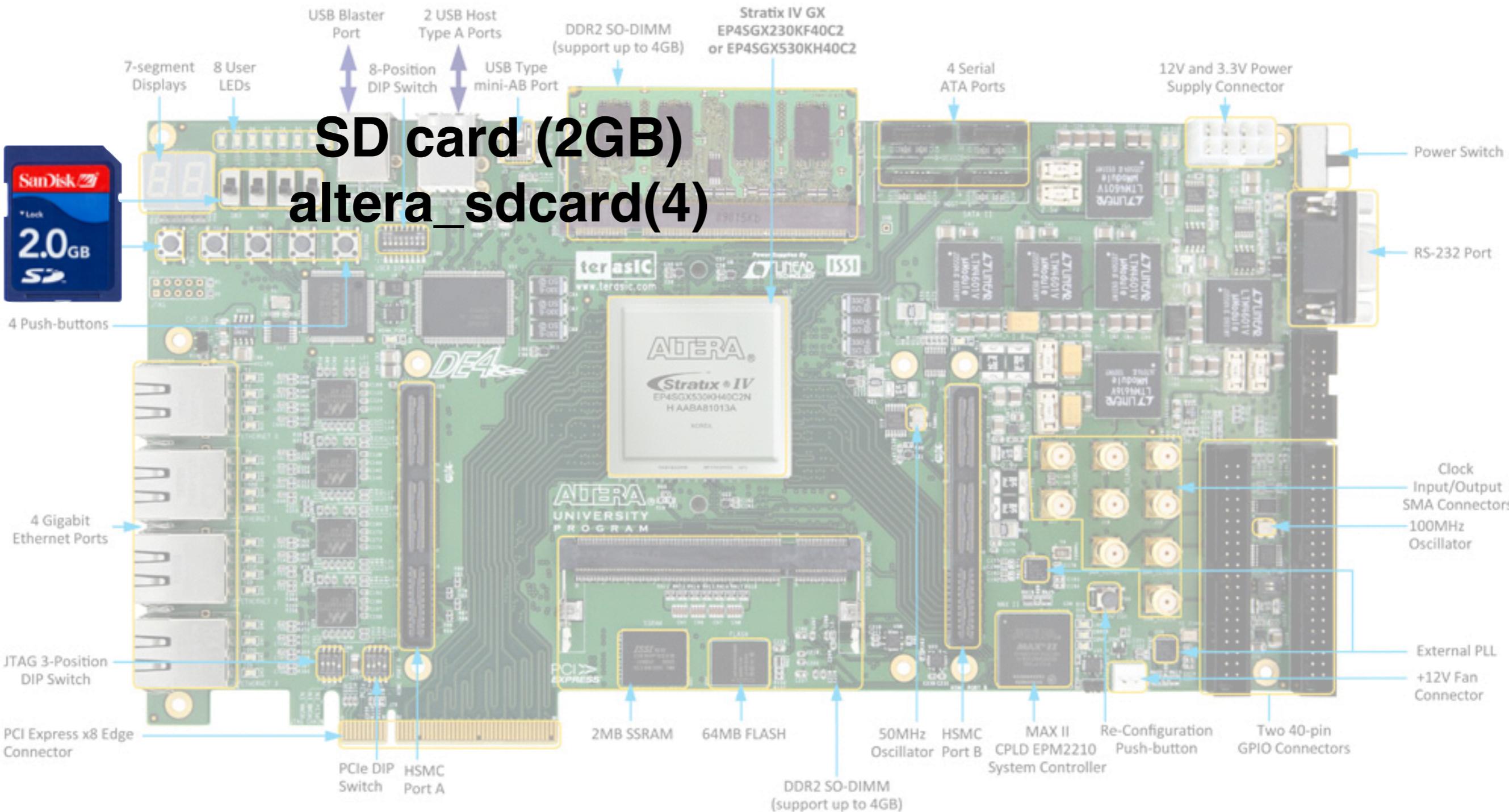


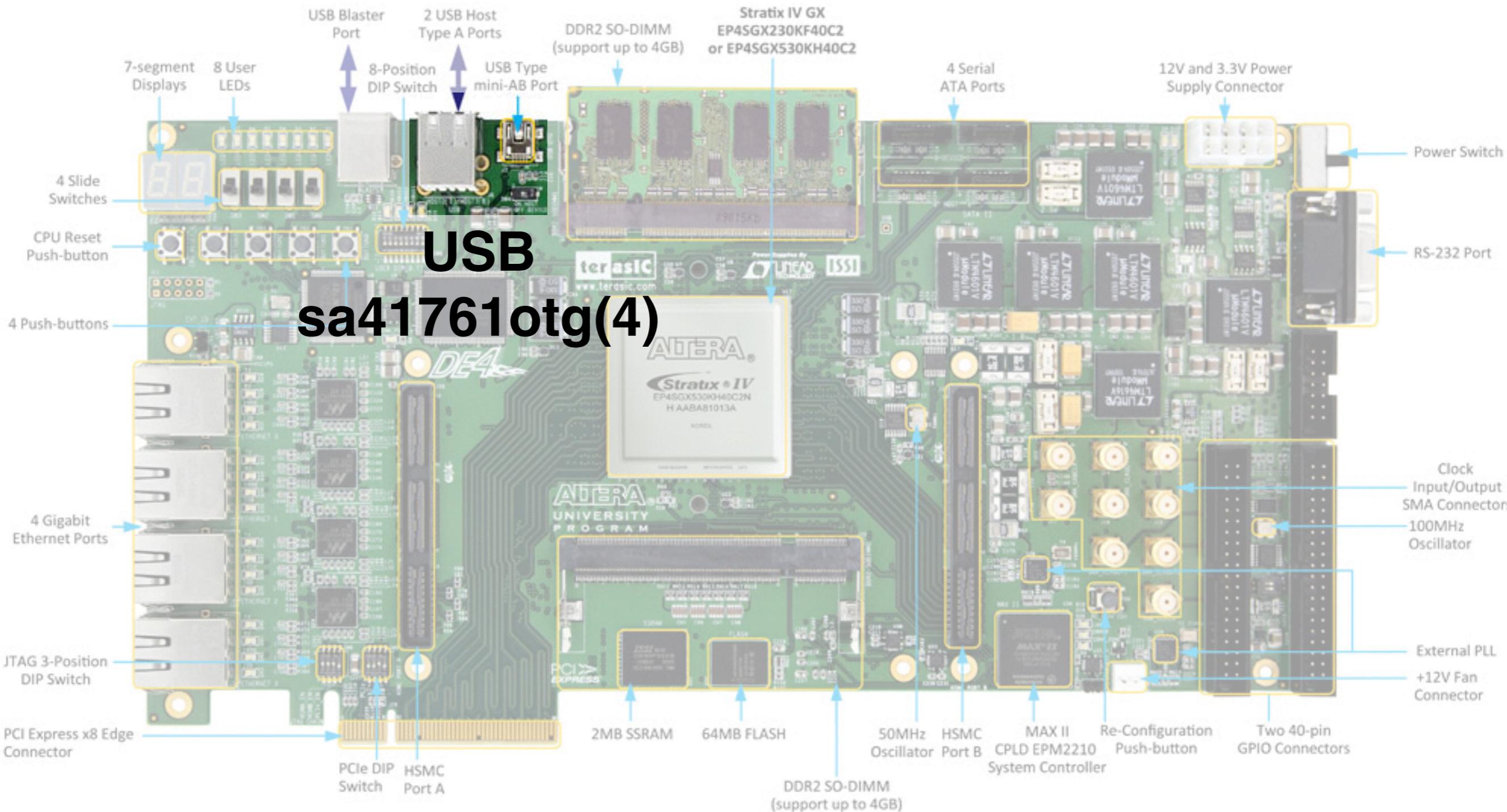












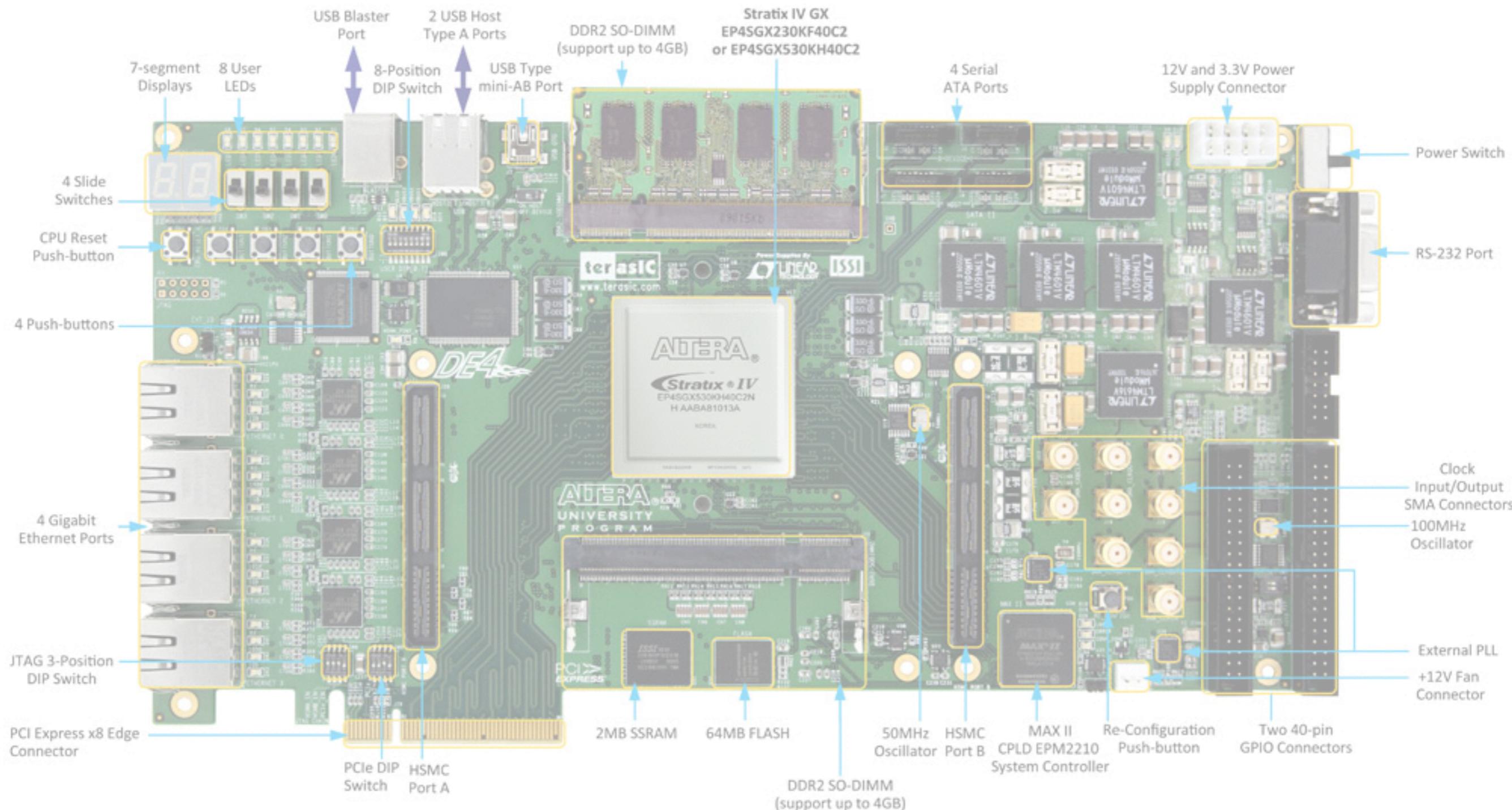
Booting CheriBSD  
Please Wait



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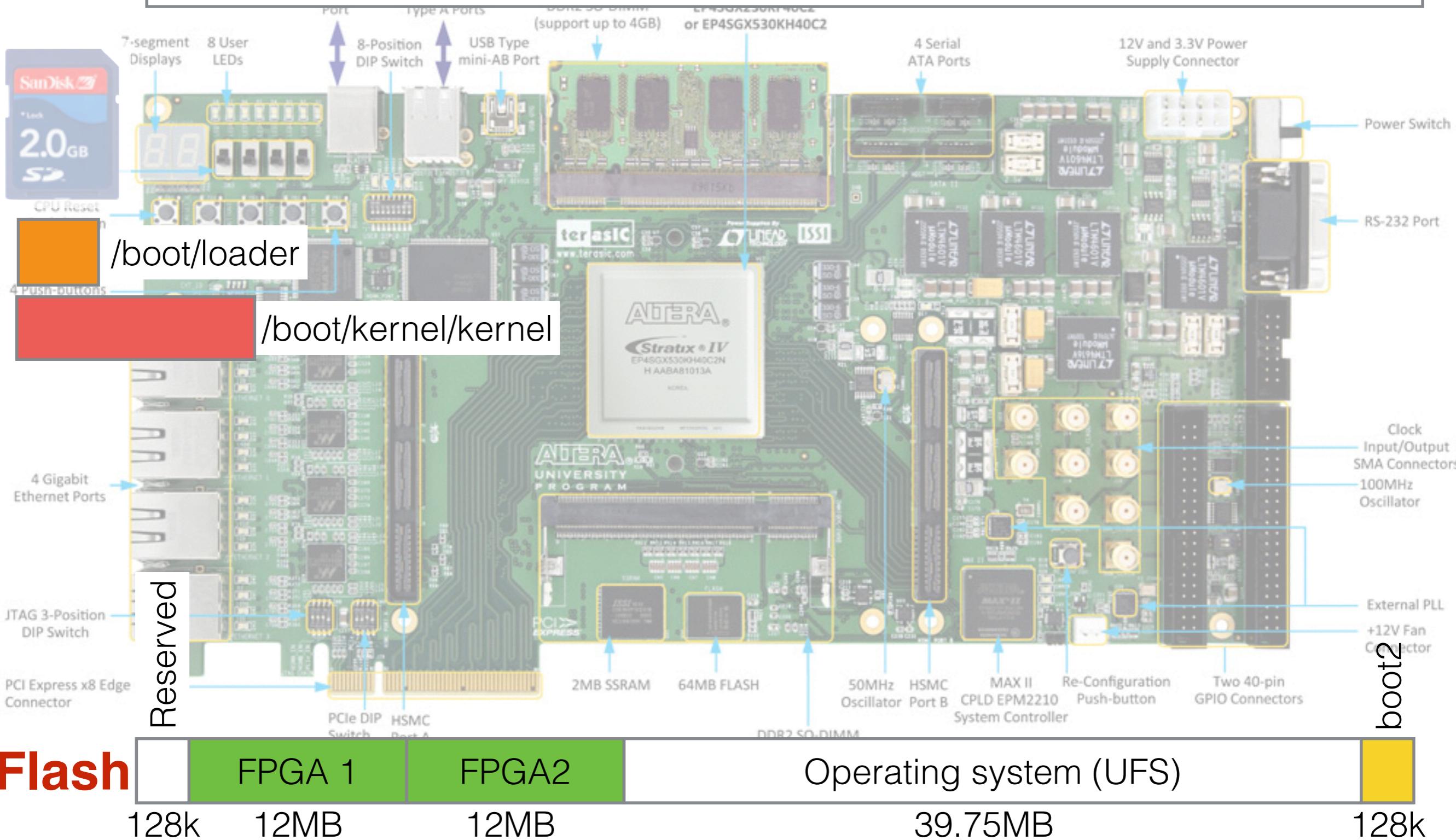
PRO VIO

# Booting the DE4



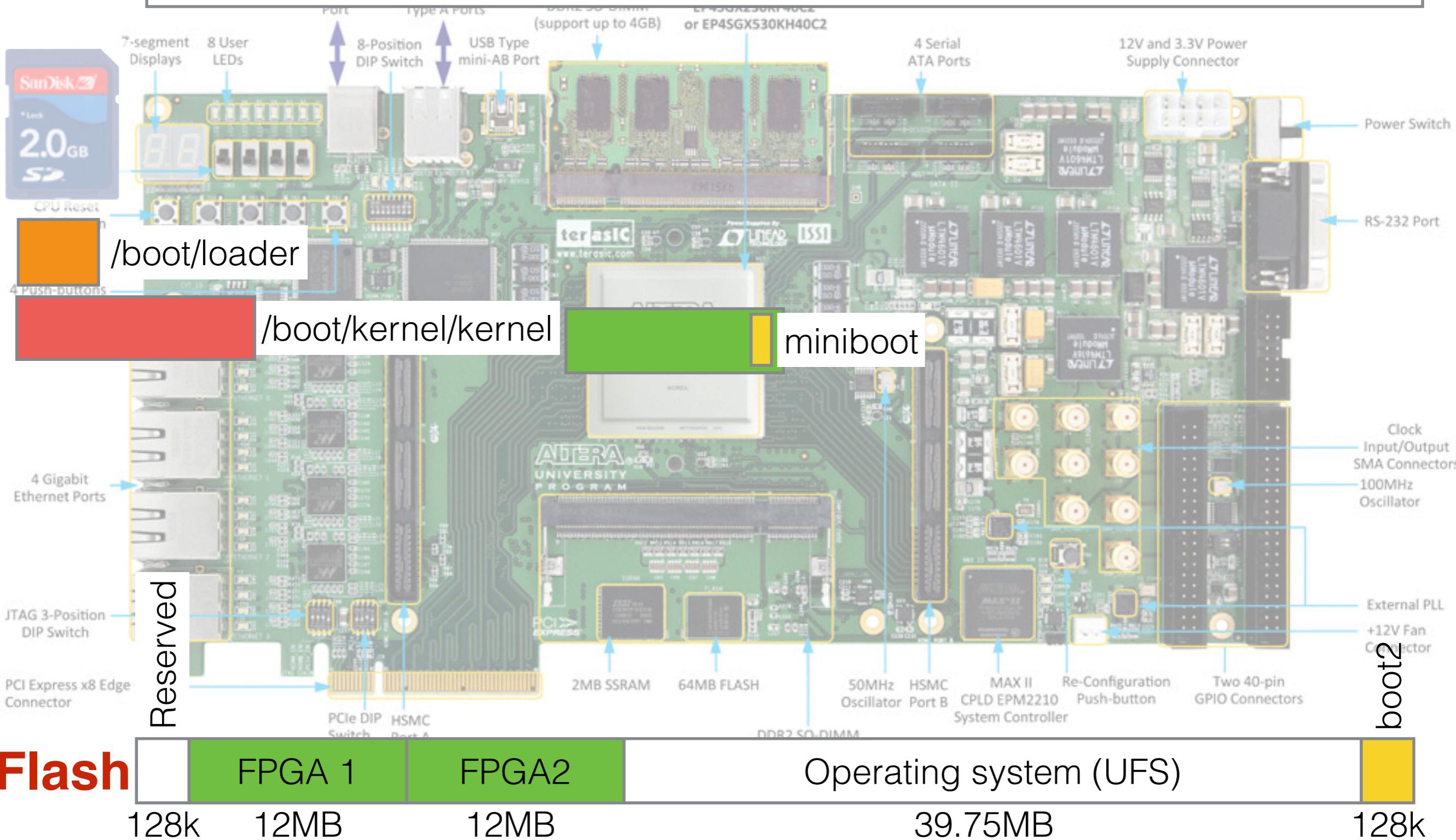
# Booting the DE4

DRAM



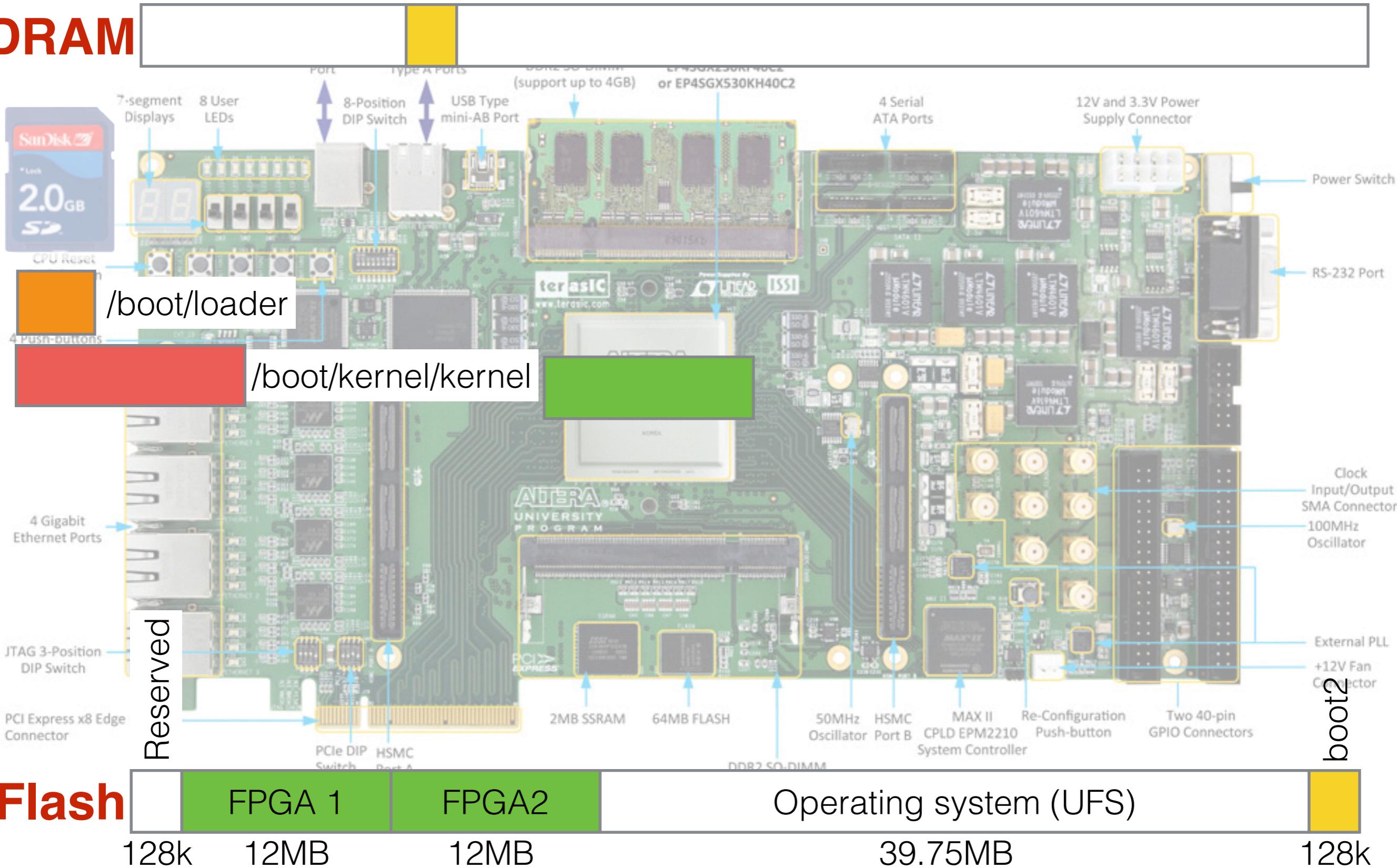
# Booting the DE4

DRAM



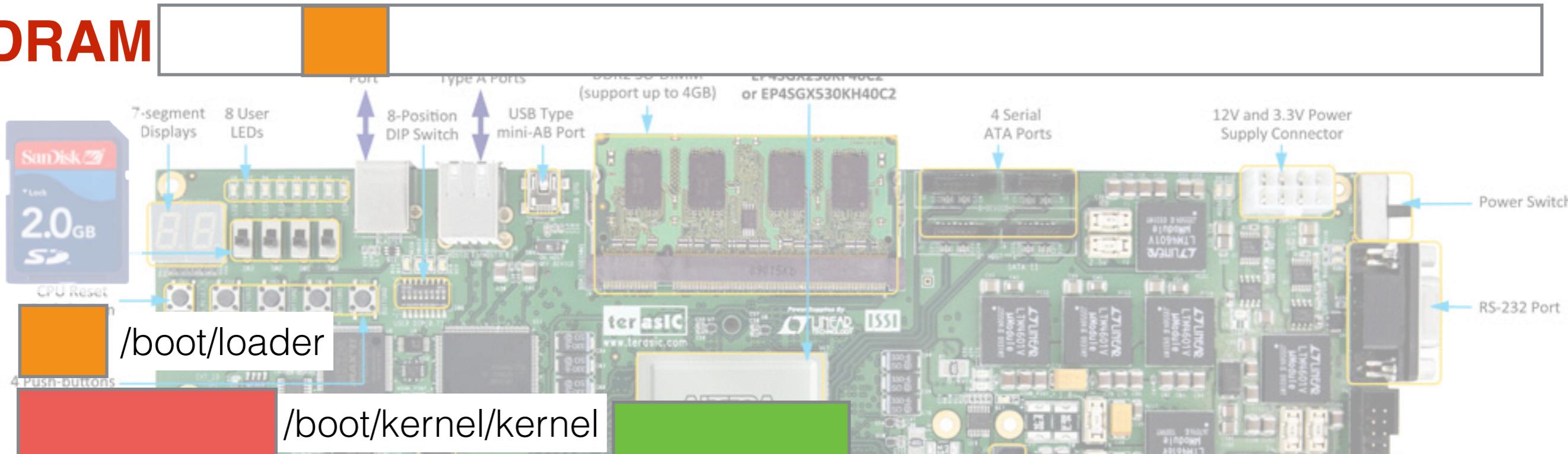
# Booting the DE4

DRAM



# Booting the DE4

DRAM



Flash

128k

FPGA 1

12MB

FPGA2

12MB

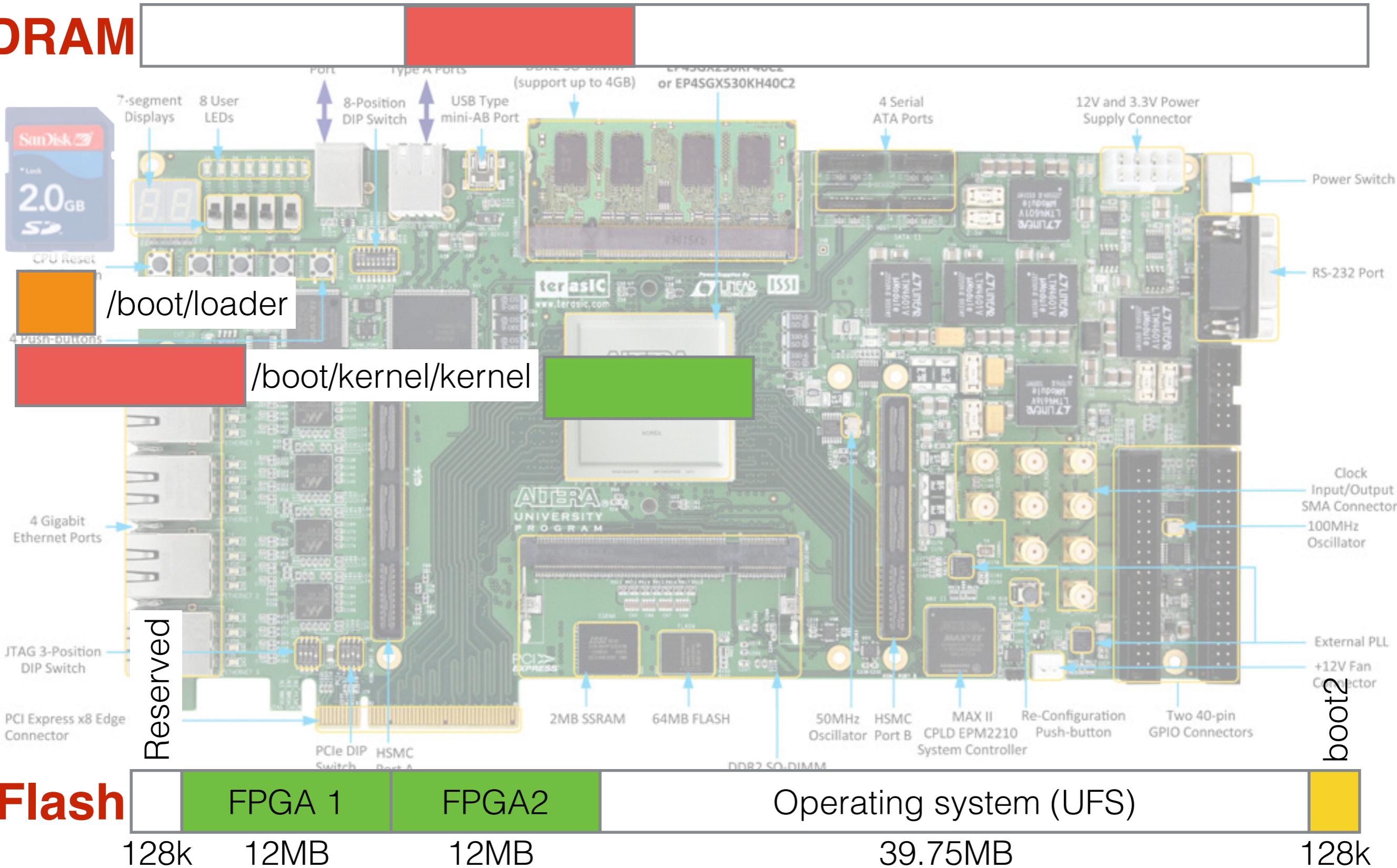
Operating system (UFS)

39.75MB

128k

# Booting the DE4

DRAM



# Early kernel boot

- Enter kernel in `_locore()` at `_start`
  - Calls BERI specific `platform_init()`
  - Finally calls `mi_startup()`



# SYSINITs

- Initializer functions
  - Declared with `SYSINIT( )` macro
  - Sorted by *subsystem* and *order*
  - Run in `mi_startup( )`



# SI\_SUB\_COPYRIGHT

Copyright (c) 1992-2013 The FreeBSD Project.

Copyright (c) 1979, 1980, 1983, 1986, 1988, 1989, 1991, 1992, 1993, 1994  
The Regents of the University of California. All rights reserved.

FreeBSD is a registered trademark of The FreeBSD Foundation.



# SI\_SUB\_CONFIGURE

- `configure_first()` @ `SI_ORDER_FIRST`
  - Attaches root bus
- `configure()` @ `SI_ORDER_THIRD`
  - Attaches all devices
  - BERI uses a mix of FDT and hints



# Flat Device Tree

```
cpus {
    cpu@0 {
        device-type = "cpu ";
        compatible = "sri-cambridge,beri";
    };
};

soc {
    beripic : beripic@7f804000 {
        compatible = "sri-cambridge,beri-pic";
        interrupt-controller;
        reg = <0x7f804000 0x400 0x7f806000 0x10
              0x7f806080 0x10 0x7f806100 0x10>;
    };
    ...
};
```



# SI\_SUB\_EXEC

```
static Elf64_Brandinfo freebsd_brand_info = {  
    .brand          = ELFOSABI_FREEBSD,  
    .machine        = EM_MIPS,  
    .compat_3_brand = "FreeBSD",  
    .emul_path     = NULL,  
    .interp_path   = "/libexec/ld-elf.so.1",  
    .sysvec        = &elf64_freebsd_sysvec,  
    .interp_newpath = NULL,  
    .flags          = 0  
};
```

```
SYSINIT(elf64, SI_SUB_EXEC, SI_ORDER_ANY,  
       (sysinit_cfunc_t) elf64_insert_brand_entry,  
       &freebsd_brand_info);
```



# Starting /sbin/init

- `create_init()` at `SI_SUB_CREATE_INIT`
  - Creates process
- `kick_init()` at `SI_SUB_KTHREAD_INIT`
  - Makes process runnable
- `scheduler()` at `SI_SUB_RUN_SCHEDULER`
  - Schedules processes



# SMP



# SI\_SUB\_TUNABLES

Sets mp\_cpus and mp\_maxid  
from platform\_cpu\_mask()



# SI\_SUB\_CPU

**BSP**

**AP $n$**

```
start_ap(n) {  
...  
cpus = mp_naps;  
platform_start_ap(n);
```



# SI\_SUB\_CPU

BSP

AP $n$

```
start_ap(n) {  
...  
cpus = mp_naps;  
platform_start_ap(n);  
                      mpentry() →  
while (mp_naps <= cpus)  
    DELAY(1000);
```



# SI\_SUB\_CPU

BSP

AP*n*

```
start_ap(n) {  
...  
cpus = mp_naps;  
platform_start_ap(n);  
while (mp_naps <= cpus)    mpentry() →  
    DELAY(1000);            smp_init_secondary() {  
...  
}
```



# SI\_SUB\_CPU

BSP

AP*n*

```
start_ap(n) {  
...  
cpus = mp_naps;  
platform_start_ap(n);  
while (mp_naps <= cpus)    mpentry() →  
    DELAY(1000);  
                                smp_init_secondary() {  
...  
    mp_naps++;  
...  
    while (!aps_ready)  
        ;  
};
```



# SI\_SUB\_CPU

BSP

AP*n*

```
start_ap(n) {  
    ...  
    cpus = mp_naps;  
    platform_start_ap(n);  
    while (mp_naps <= cpus)  
        mpentry() →  
        DELAY(1000);  
    smp_init_secondary();  
    ...  
    mp_naps++;  
    ...  
    while (!aps_ready)  
        ;  
}
```



# Spin table

```
struct {  
    uint64_t entry_addr;  
    uint64_t a0;  
    uint32_t rsvd1;  
    uint32_t pir;  
};
```



# SI\_\_SUB\_\_SMP

BSP

AP*n*

```
smp_init_secondary() {  
    ...  
    while (!aps_ready)  
        ;
```



# SI\_SUB\_SMP

BSP

```
release_aps( ) {  
    /* IPI setup */  
  
    ...
```

AP*n*

```
smp_init_secondary( ) {  
    ...  
    while ( !aps_ready )  
        ;
```



# SI\_SUB\_SMP

BSP

```
release_aps( ) {  
    /* IPI setup */  
    ...  
    aps_ready = 1;
```

```
while ( !smp_started)  
    ;
```

AP*n*

```
smp_init_secondary( ) {  
    ...  
    while ( !aps_ready)  
        ;
```



# SI\_SUB\_SMP

BSP

```
release_aps( ) {  
    /* IPI setup */  
  
    ...  
  
    aps_ready = 1;  
  
    while ( !smp_started)  
        ;
```

AP*n*

```
smp_init_secondary( ) {  
    ...  
    while ( !aps_ready)  
        ;  
  
    ...  
    if ( /* last AP */ )  
        smp_started = 1;
```



# SI\_SUB\_SMP

BSP

```
release_aps( ) {  
    /* IPI setup */  
  
    ...  
  
    aps_ready = 1;  
  
    while ( !smp_started)  
        ;
```

AP*n*

```
smp_init_secondary( ) {  
    ...  
    while ( !aps_ready)  
        ;  
  
    ...  
    if ( /* last AP */ )  
        smp_started = 1;  
  
    while ( !smp_started)  
        ;
```



# SI\_SUB\_SMP

BSP

```
release_aps( ) {  
    /* IPI setup */  
    ...  
    aps_ready = 1;  
  
    while ( !smp_started)  
        ;
```

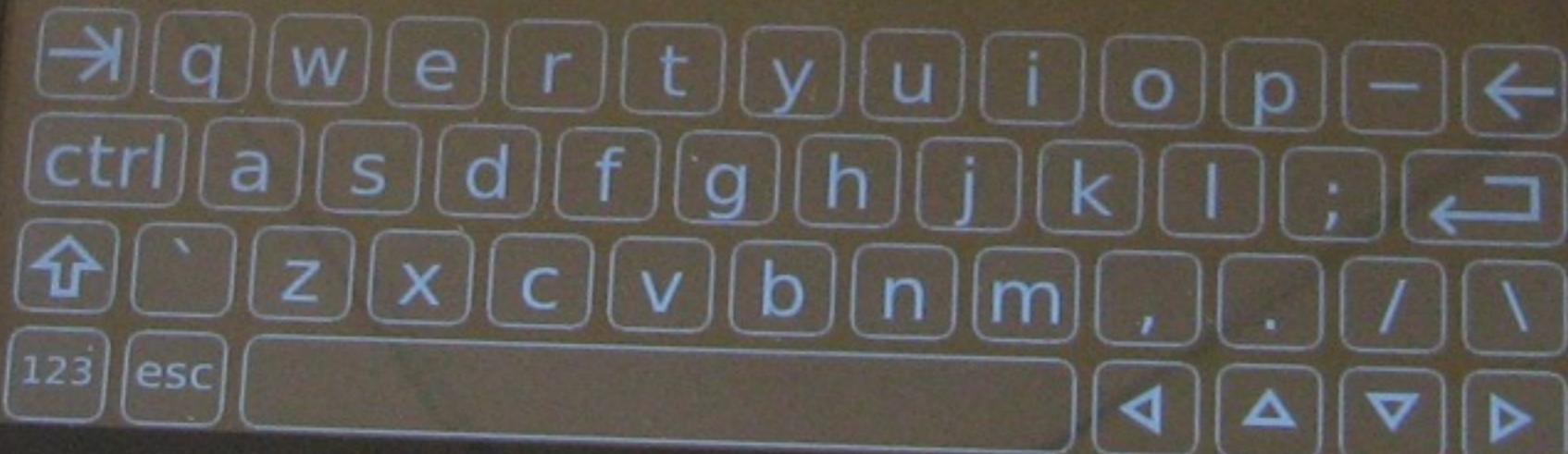
AP*n*

```
smp_init_secondary( ) {  
    ...  
    while ( !aps_ready)  
        ;  
    ...  
    if (/* last AP */)  
        smp_started = 1;  
  
    while ( !smp_started)  
        ;  
    ...  
    /* enter scheduler */  
}
```



last pid: 550; load averages: 1.93, 0.88, 0.38 up 8+00:03:42 20:16:35  
2 processes: 4 running, 3 sleeping  
CPU: 69.9% user, 0.0% nice, 2.7% system, 27.4% interrupt, 0.0% idle  
Mem: 28M Active, 5624K Inact, 14M Wired, 5448K Buf, 898M Free  
Swap:

PID	USERNAME	THR	PRI	NICE	SIZE	RES	STATE	TIME	WCPU	COMMAND
543	root	1	102	0	37996K	28888K	RUN	0:46	100.00%	pictview
550	root	1	20	0	11936K	2600K	RUN	0:01	0.98%	top
545	root	1	52	0	10476K	1928K	RUN	0:01	0.00%	getty
546	root	1	52	0	10476K	1928K	RUN	0:01	0.00%	getty
524	root	1	20	0	10488K	1484K	select	0:00	0.00%	syslogd
547	root	1	20	0	11184K	2588K	wait	0:00	0.00%	sh
544	root	1	52	0	10476K	1928K	ttyin	0:00	0.00%	getty



A close-up photograph of a pile of ripe, dark purple gooseberries. The berries are round and have a slightly textured surface. Some small green stems and brownish-orange calyxes are visible where the berries were attached to the vine.

<http://beri-cpu.org>



# bringing up NIPS

Porting FreeBSD  
to a new CPU, even  
within a previously  
supported family,  
is a significant  
undertaking.

FreeBSD Journal  
<http://freebsdjurnal.org>