PNIC HARDWARE SPECIFICATION

Preliminary Information

Rev.1.0

Dec. 1, 1994

LITE

First Edition, January 1995

LITEON Inc.
720 S. Hillview Drive
Milpitas, California 95035

Printed in USA

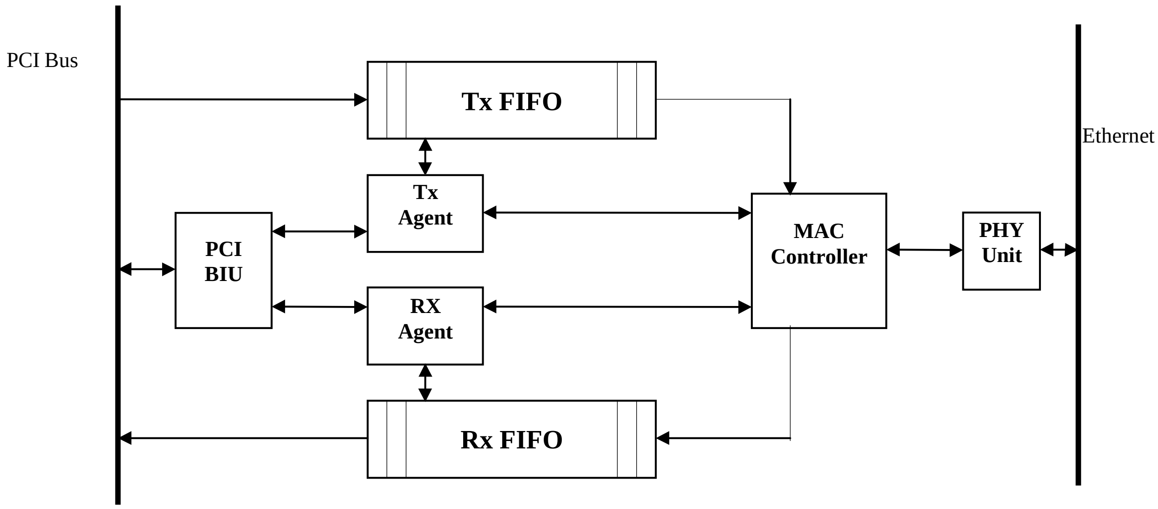
1. Introduction

PCI Network Interface Controller(PNIC) is a high performance and highly integrated PCI bus Ethernet controller chip. Its bus master architecture greatly reduces host CPU involvement in transferring transmit and receive data to/from network. Thus CPU utilization is kept very low which allows more CPU processing power for other applications.

1.1 Features

- Single chip PCI Ethernet controller for 10Mbps/100Mbps.
- Direct interface to PCI bus.
- Compliance to PCI local bus specification (Revision 2.0 and 2.1).
- On-chip integrated attachment unit interface(AUI) port and 10BASE-T transceiver.
- On-chip External 10Mbps ENDEC interface.
- Full duplex operation supported.
- Bus speed up to 33 MHz. No wait state on bus master operation.
- On-chip DMA with programmable, unlimited burst size.
- Two large independent FIFO for transmit and receive.
- Big and little endian byte ordering supported.
- Compliance to ISO 8802-3 (IEEE/ANSI 803.3,802.3u), 100BASE-T4, 100BASE-TX and Ethernet standards.
- Direct serial EEPROM interface for Ethernet ID address and jumperless board design.
- 256K Boot ROM or Flash memory support for diskless application.
- Different address filtering modes:
  16 perfect addresses or
  512 hash-filtered multicast addresses and one perfect address
  512 hash-filtered physical addresses and multicast addresses
  Inverse perfect filtering
- MII interface for external 10Mbps/100Mbps PMA unit.
- On-chip 100Base-TX scrambler and descrambler functions.
- Software switchable 10Mbps/100Mbps Ethernet MAC.
- Blast mode transmission capability.
- Option for padding for short transmit frames.
- Transmit CRC on frame by frame basis.
- Late collision detection.
- Receive CRC stripping.
- Long receive frame abortion.
- Internal loopback, external loopback and ENDEC loopback support.
- Auto polarity detection and correction capability for 10BASET.
- IEEE 802.3u N-way Auto negotiation standard supported.
- Support Power down mode for Green PC application.
- LEDs for Transmit, receive, collision, link-pass, network speed.
- Support 3.3V and 5.0V power supply.

1.2 Block Diagram



PNIC is partitioned into 7 major blocks: **PCI Bus Interface Unit, Tx Agent, Tx FIFO, Rx Agent, Rx FIFO, MAC Controller, and Ethernet PHY Interface**.

- **PCI Bus Interface Unit**, it generates and receives PCI signals. It also contains the programming interface. Registers are provided for the program to control and monitor the status of each blocks.
- **Tx Agent**, it takes the transmit command from the host and manage the transmission process.
- **Tx FIFO**, Tx Agent puts data into the Tx FIFO and requests services from the MAC controller to send out the data to the network..
- **Rx Agent**, it is responsible to move data from Rx FIFO to the host memory.
- **Rx FIFO**, Media Agent stores the receiving packets in the Rx FIFO.
- **MAC Controller**, it schedules the outgoing packets and grabs the packets belong to the host. It handles all the IEEE802.3 Data Link Layer protocol to transmit and receive data.
- **Ethernet PHY Interface**, it generates and receives Ethernet signals.

In Chapter 2, IO are listed.
In Chapter 3, it covers the programming interface and the Register sets definition.
In Chapter 4, the communication between the host and the Tx Agent and the Rx Agent will be discussed.
In Chapter 5, transmit and receive process will be discussed in greater details, as well as the address filtering setup.
In Chapter 6, Different Errors conditions are summarized.

1.3 Reference

- PCI local bus specification Rev2.0 and Rev2.1.
- IEEE/ANSI 803.3, 802.3u, 100BASE-T4, 100BASE-TX.

2. Pin and signal Descriptions

2.1 Signal Convention

- "*" before a signal name indicates possible pin sharing.
- "#" at the end of a signal name indicates active low signal.

2.2 Signal Description

2.2.1 PCI Interface

Name	Type	Description
AD[31:0]	BIDIR	multiplex PCI address/data lines
CBE#[3:0]	BIDIR	PCI bus command code/byte enable
CLK	INPUT	PCI bus clock
DEVSEL#	BIDIR	Device select
FRAME#	BIDIR	PCI cycle frame signal
REQ#	OUTPUT	PCI bus request
GNT#	INPUT	PCI bus grant
IDSEL	INPUT	Initialization device select
INTR#	OUTPUT	PCI interrupt request
IRDY#	BIDIR	Initiator ready
PAR	BIDIR	Parity
PERR#	BIDIR	Parity error
RST#	INPUT	Chip reset
SERR#	OUTPUT	System error
TRDY#	BIDIR	Target ready
STOP#	BIDIR	PCI stop indicator

2.2.2 EEPROM Interface

Name	Type	Description
* EPCLK/BADR17	OUTPUT	Serial EEPROM (MicroWire) clock. When EPCS is active, this output pin provides clock to the MicroWire EEPROM. If EPCS is not active, this pin is Boot ROM/Flash address bit 17.
EPDI	INPUT	Serial EEPROM (MicroWire) data input. This is serial data input pin from the external serial EEPROM.
*EPDO/BADR16	OUTPUT	Serial EEPROM (MicroWire) data output. When EPCS pin is active, this output pin provides data to the MicroWire EEPROM. If EPCS is not active, this pin is Boot ROM/Flash address bit 16.
EPCS	OUTPUT	Serial EEPROM (MicroWire) chip select. This pin provides external serial EEPROM chip select. It is active high.

2.2.3 ROM Interface

Name	Type	Description
BADR[15]	OUTPUT	Boot ROM/Flash memory Address bus bit 15.
*BADR[14]/DUP_LED	OUTPUT	In normal operation, this pin drives external Full duplex LED. If BCS# is active, this pin provides address bit 14 to Boot ROM/Flash memory.

*BADR[13]/ MED_LED	OUTPUT	In normal operation, this pin drives external Media LED. If BCS# is active, this pin provides address bit 13 to the Boot ROM/Flash memory.
*BADR[12]/SPD_LED	OUTPUT	In normal operation, this pin drives external Speed LED. If BCS# is active, this pin provides address bit 12 of the Boot ROM/Flash.
*BADR[11]/COL_LED	OUTPUT	In normal operation, this pin drives external Collision LED. If BCS# is active, this pin provides address bit 11 to the Boot ROM/Flash.
*BADR[10]/LNK_LED	OUTPUT	In normal operation, this pin drives external Link LED. If BCS# is active, this pin provides address bit 10 to the Boot ROM/Flash memory.
*BADR[9]/ACT_LED	OUTPUT	In normal operation, this pin drives external Activity LED. If BCS# is active, this pin provides address bit 9 to the Boot ROM/Flash memory.
BADR[8:0]	OUTPUT	Boot ROM/Flash address bit 8 to bit 0.
BDATA[7:0]	BIDIR	Boot ROM/Flash memory Data bus.
*BCS#/TEST	BIDIR	In normal operation, this pin acts as the Chip select for the Boot ROM/Flash memory. It is active low. Internally, there is a pull-up. If it is pulled down externally, on-chip serial EEPROM interface enters test mode upon hardware reset. In test mode, the whole chip is not held in reset during EEPROM configuration cycle.
*BOE#/EXT_ENDEC	BIDIR	Boot ROM/Flash memory output enable. It is active low. This pin has internal pull-up. If this pin is externally pulled down, the default network interface is set for external ENDEC after power-up, otherwise it will default to internal PHY interface.
BWE#/END_TXD	OUTPUT	Flash memory Write enable when it is asserted along with BCS#. It is active low. When external ENDEC is selected, this pin provides transmit data to the external ENDEC when EXT_TXE is active.

2.2.4 AUI Interface

Name	Type	Description
AUI_CD-	INPUT	AUI collision input (differential)
AUI_CD+	INPUT	AUI collision input (differential)
AUI_RD-	INPUT	AUI receive input (differential)
AUI_RD+	INPUT	AUI receive input (differential)
AUI_TD-	OUTPUT	AUI transmit output (differential)
AUI_TD+	OUTPUT	AUI transmit output (differential)
RBIAS	INPUT	Bias resistor

2.2.5 10BASE-T Interface

Name	Type	Description
TP_RD-	INPUT	10BASET receive data (differential)
TP_RD+	INPUT	10BASET receive data (differential)
TP_TD+	OUTPUT	10BASET transmit data (differential)
TP_TD-	OUTPUT	10BASET transmit data (differential)
TP_TP+	OUTPUT	10BASET transmit data resistive feedback
TP_TP-	OUTPUT	10BASET transmit data resistive feedback

2.2.6 Media Independent/External ENDEC/SYM Interface

Name	Type	Description
*MCRS/END_CRS#	BIDIR	In MII or external ENDEC mode, this pin provides carrier signal to on-chip MII interface or 10Mbit MAC. Default is input.
*MCOL/END_COL#	BIDIR	In MII or external ENDEC mode, this pin provides PNIC collision detection signal. Default is input.
*MTXEN/END_TXE#	BIDIR	In MII mode, this pin provides transmit enable signal to external PHY. In external ENDEC mode, this pin provides transmit enable signal to external ENDEC. Default is output.
*MTCLK/SYMTCLK	BIDIR	In MII mode, this pin provides transmit clock for on-chip MII logic. In SYM mode, this pin provides transmit clock for on-chip 100BASE-TX logic. Default is input.
*MRCLK/SYMRCLK	BIDIR	In MII or SYM mode, this pin provides receive clock to 10/100Mbit MAC logic. Default is input.
*MDIO/END_RXD	BIDIR	In MII mode, this pin provides and accepts MII management data to/from external PHY. In external ENDEC mode, this pin provides PNIC 10Mbit receive data, Default is input.
*MMCLK	OUTPUT	In MII mode, this pin provides MII management clock to external PHY chip.
*MRXERR/END_RXC	INPUT	In MII mode, this pin signals receive data error during frame reception. In external ENDEC mode, this pin provides receive clock to PNIC.
*MRXDV/END_TXC	INPUT	In MII mode, this pin signals receive data valid during frame reception. In external ENDEC mode, this pin provides transmit clock to PNIC.
SYMTXD[4]	BIDIR	In SYM mode, this pin is transmit data bit 4. Default is output.
*MTXD[3:0]/ SYMTXD[3:0]	OUTPUT	In MII mode, MTXD[3:0] are transmit data bundle. In SYM mode, SMTXD[3:0] are transmit data bundle.
SYMRXD[4]	BIDIR	In SYM mode, this pin is the receive data bit 4. Default is input.
*MRXD[3:0]/ SYMRXD[3:0]	INPUT	In MII mode, MRXD[3:0] are receive data bundle. In SYM mode, SYMRXD[3:0] are receive data bundle.

2.2.7 100BASE-TX Interface

*MTXD[4:0]	OUTPUT	Transmit data output for 100BASE-TX
*MRXD[4:0]	INPUT	Receive data input for 100BASE-TX
*MTCLK	INPUT	Transmit clock for 100BASE-TX
*MRCLK	INPUT	Receive clock for 100BASE-TX

2.2.8 General Purpose Pins

*GENP[0]/ SPEED_RLY	BIDIR	In normal operation, this pin can be used to control the external 10/100Mbit relay. This pin defaults to input.
*GENP[1]/ 100M_LPKB	BIDIR	In normal operation, this pin can be used to control loop back pin of external 100BASE-TX chip. For 10/100Mbit switchable adapter card, this pin should have an external pull down. In 10Mbit only chip, this pin is unbounded. This pin defaults to input.
*GENP[2]/	BIDIR	In normal operation, this pin can be used to control the external

BNC_XMER		12V-9V DC-to-DC converter for BNC. This pin defaults to input.
*GENP[3]/ LNK100X	BIDIR	In MII mode, this pin provides external MII PHY chip select. In normal operation, this pin provides 100BASE-TX link status to PNIC. Default is input.

2.2.9 Miscellaneous Pins

XTAL1	INPUT	Crystal input (20 MHz) for 10Mbps.
XTAL2	OUTPUT	Crystal output (20 MHz) for 10Mbps.

2.2.10 Power and Ground

VDDR	INPUT	Analog RX power.
VSSR	INPUT	Analog RX ground.
VDDT	INPUT	Analog TX power.
VSST	INPUT	Analog TX ground.
VDDI/VDD	INPUT	Power.
VSSI/VSS	INPUT	Ground.

2.3 Signal vs. Pin cross reference

2.3.1 Sorted by pin number

PIN #	NAME	PIN #	NAME	PIN #	NAME	PIN #	NAME
1	RBIAS	41	AD22	81	AD6	121	BDATA4
2	AUI_DI-	42	AD21	82	VSS	122	BDATA3
3	AUI_DI+	43	VSSI	83	AD5	123	VSSI
4	AUI_CD-	44	VSS	84	AD4	124	BDATA2
5	AUI_CD+	45	AD20	85	VDD	125	BDATA1
6	VDDR	46	VDDI	86	AD3	126	VDDI
7	TP_RD-	47	VDD	87	VSS	127	BDATA0
8	TP_RD+	48	AD19	88	AD2	128	VSS
9	VSSR	49	AD18	89	AD1	129	BCS#
10	AUI_DO-	50	VSS	90	AD0	130	BOE#
11	AUI_DO+	51	AD17	91	VSS	131	BWE#
12	VDDT	52	AD16	92	EPCS	132	MTCLK
13	TP_TD+	53	CBE#2	93	EPDI	133	MMCLK
14	TP_TP+	54	FRAME#	94	EPCLK	134	MDIO
15	TP_TP-	55	IRDY#	95	EPDO	135	VDD
16	TP_TD-	56	VSS	96	GENP2	136	XTAL2
17	VSST	57	TRDY#	97	VSS	137	XTAL1
18	GENP0	58	DEVSEL#	98	BADR15	138	GENP3
19	INTR#	59	STOP#	99	VDD	139	MTXEN
20	RST#	60	VDD	100	BADR14	140	VSS
21	CLK	61	PERR#	101	BADR13	141	MCOL
22	VSS	62	SERR#	102	BADR12	142	MTXD4
23	VSS	63	PAR	103	BADR11	143	MTXD3
24	GNT#	64	CBE#1	104	BADR10	144	MTXD2
25	VDD	65	AD15	105	VSS	145	MTXD1
26	AD31	66	VSS	106	BADR9	146	MTXD0
27	AD30	67	AD14	107	BADR8	147	VDD
28	VSS	68	AD13	108	BADR7	148	GENP1
29	AD29	69	AD12	109	BADR6	149	MRXERR
30	AD28	70	VSS	110	BADR5	150	MRXDV
31	AD27	71	AD11	111	BADR4	151	MCRS
32	VSS	72	AD10	112	BADR3	152	VSS
33	AD26	73	VDD	113	BADR2	153	MRCLK
34	AD25	74	AD9	114	BADR1	154	MRXD4
35	VDD	75	VDDI	115	VDD	155	VDDI
36	AD24	76	VSS	116	BADR0	156	MRXD3
37	VSS	77	AD8	117	VSS	157	MRXD2
38	CBE#3	78	VSSI	118	BDATA7	158	VSSI
39	IDSEL	79	CBEB0	119	BDATA6	159	MRXD1
40	AD23	80	AD7	120	BDATA5	160	MRXD0

2.3.2 Sorted by name

NAME	PIN#	NAME	PIN#	NAME	PIN#	NAME	PIN#
AD0	90	BADR2	113	GNT#	23	VDD	60
AD1	89	BADR3	112	IDSEL	39	VDD	73
AD2	88	BADR4	111	INTR#	19	VDD	85
AD3	86	BADR5	110	IRDY#	55	VDD	99
AD4	84	BADR6	109	MCOL	141	VDD	115
AD5	83	BADR7	108	MCRS	151	VDD	135
AD6	81	BADR8	107	MDIO	134	VDD	147
AD7	80	BADR9	106	MMCLK	133	VDDI	46
AD8	77	BADR10	104	MRCLK	153	VDDI	75
AD9	74	BADR11	103	MRXDV	150	VDDI	126
AD10	72	BADR12	102	MRXD0	160	VDDI	155
AD11	71	BADR13	101	MRXD1	159	VDDR	6
AD12	69	BADR14	100	MRXD2	157	VDDT	12
AD13	68	BADR15	98	MRXD3	156	VSS	22
AD14	67	BCS#	128	MRXERR	149	VSS	28
AD15	65	BDATA0	127	MTCLK	132	VSS	32
AD16	52	BDATA1	125	MTXD0	146	VSS	37
AD17	51	BDATA2	124	MTXD1	145	VSS	44
AD18	49	BDATA3	122	MTXD2	144	VSS	50
AD19	48	BDATA4	121	MTXD3	143	VSS	56
AD20	45	BDATA5	120	MTXEN	139	VSS	66
AD21	42	BDATA6	119	PAR	63	VSS	70
AD22	41	BDATA7	118	PERR#	61	VSS	76
AD23	40	BOE#	130	RBIAS	1	VSS	82
AD24	36	BWE#	131	REQ#	24	VSS	87
AD25	34	CBE#0	79	RST#	20	VSS	91
AD26	33	CBE#1	64	SERR#	62	VSS	97
AD27	31	CBE#2	53	STOP#	59	VSS	105
AD28	30	CBE#3	38	MRXD4	154	VSS	117
AD29	29	CLK	21	MTXD4	142	VSS	128
AD30	27	DEVSEL#	58	TP_RD+	8	VSS	140
AD31	26	EPCLK	94	TP_RD-	7	VSS	152
AUI_CD+	5	EPCS	92	TP_TD+	13	VSSI	43
AUI_CD-	4	EPDI	93	TP_TD-	16	VSSI	78
AUI_DI+	3	EPDO	95	TP_TP+	14	VSSI	123
AUI_DI-	2	FRAME#	54	TP_TP-	15	VSSI	158
AUI_DO+	11	GENP0	18	TRDY#	57	VSSR	9
AUI_DO-	10	GENP1	148	VDD	25	VSST	17
BADR0	116	GENP2	96	VDD	35	XTAL1	137
BADR1	114	GENP3	138	VDD	47	XTAL2	136

3. Register Definition

Two register domains are provided to control PNIC:

- **PCI configuration register set:** The PCI configuration register set is required to be implemented by the PCI bus standard.
- **PNIC Tx/Rx Command and Status register set:** It is provided for the host system to communicate with PNIC in order to control the transmit and receive operation.

3.1 PCI Configuration register set:

IO ADDR Offset	NAME	READ/WRITE	DESCRIPTION
00H	CFID	READ ONLY	Identification register
04H	CFCS	READ WRITE	Command and status registers
08H	CFRV	READ ONLY	Revision register
0CH	CFLT	READ WRITE	Latency timer register
10H	CFIOB	READ WRITE	I/O base address register
14H	CFMEMB	READ WRITE	Memory base address register
18H-2CH			Reserved
30H	CFROMB	READ WRITE	ROM base address register
34H-38H			Reserved
3CH	CFINT	READ WRITE	Interrupt register
40H	CFDA	READ WRITE	Driver area register

3.1.1 CFID

Name: **Identification Register**
Address Offset: **00**
R/W Attribute: **Read-only**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1	1	0	1	0	1	1	0	1

Field		Description
bit[31:16]		Device ID, Hardwired to 0001H.
bit[15:00]		Vendor ID, Hardwired to 11ADH

3.1.2 CFCS

Name: **Command and Status Register**
Address Offset: **04H**
R/W Attribute: **Read/Write**
Reset Default: **02800000H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PE	SSE	RA	RTA		DEV Timing		DPT	FBB															SEE		PER				BM	MSAC	IOAC

Field	Name	Description
bit[31]	PE	**Detected parity error**. This bit will be set by PNIC whenever it detects parity error regardless bit[6]. This bit can be cleared by writing an “1” to this bit.
bit[30]	SSE	**Signal system error**. When PNIC asserts SERR#, this bit will be set. This bit can be cleared by writing an “1” to this bit.
bit[29]	RA	**Receive master abort**. When PNIC is in master operation and it terminates its transaction with a master abort, this bit will be set. This bit can be cleared by writing an “1” to this bit.
bit[28]	RTA	**Receive target abort**. When PNIC is in master operation and it detects target abort, this bit will be set. This bit can be cleared by writing an “1” to this bit.
bit[27]		Reserved
bit[26:25]	DVT	**DEVSEL# signal timing**: 00: fast; 01: medium; 10: slow. It determines the response time of the device select signal, DEVSEL#. It is hardwired to “01”. It is read only.
bit[24]	DPT	**Data parity detect**. This bit is set if the following three conditions are met: a) PNIC is in master mode. b) PNIC detects PERR# asserted. and c) bit[6] is set to “1”.
bit[23]	FBB	**Fast back to back**. It is hardwired to “1”. It is read only.
bit[22:09]		Reserved
bit[08]	SEE	**SERR enable**. If this bit and bit[6] are set, PNIC will assert a system error signal, SERR# when a parity error is seen on the address cycle.
bit[07]		Reserved
bit[06]	PER	**Parity error response enable**. This bit is used to enable the assertion of SERR# and PERR# signal by PNIC.
bit[05:03]		Reserved
bit[02]	BM	**Bus master operation enable**, PNIC will be allowed to perform master operation when this bit is set.
bit[01]	MSAC	**Memory space access enable**. PNIC responds the memory space access if this bit is set.
bit[00]	IOAC	**IO space access enable**. PNIC responds the IO space operation.

3.1.3 CFRV

Name: **Revision Register**
Address Offset: **08H**
R/W Attribute: **Read Only**
Reset Default: **02000001H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	Reserved								0	0	0	0	0	0	0	1

Field		Description
bit[31:24]		**Network card code**, it is hardwired to 00000010.
bit[23:16]		**Ethernet controller code**, it is hardwired to 00000000
bit[15:08]		Reserved
bit[07:00]		**Step revision number**. The first version is hardwired to 00000001

3.1.4 CFLT

Name **Latency Timer Register**
Address Offset: **0CH**
R/W Attribute: **Read/Write**
Rest Default: **00000000H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																Latency Timer								Reserved							

Field		Description
bit[31:16]		Reserved
bit[15:08]		**Latency timer**. PNIC terminates its master operation if the latency timer expires.
bit[07:00]		Reserved

3.1.5 CFIOB

Name: **CSRs IO Base Address Register**
Address Offset: **10H**
R/W Attribute: **Read/Write**
Reset Default: **00000001H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IO Base Address																								0	0	0	0	0	0	0	1

Field		Description
bit[31:08]		**IO base address of CSRs**. It defines the IO address base of the Tx/Rx Command and Status register set.
bit[7:0]		Hardwired to 00000001

3.1.6 CFMEM

Name: **CSRs Memory Base Register**
Address Offset: **14H**
R/W Attribute: **Read/Write**
Reset Default: **00000000H**

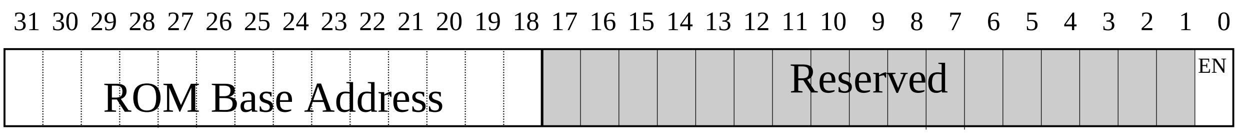
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mem Base Address																								0	0	0	0	0	0	0	0

Field		Description

bit[31:08]		**Memory base address of CSRs**. It defines the memory address base of the Tx/Rx Command and Status register set.
bit[7:0]		Hardwired to Zero

3.1.7 CFROM

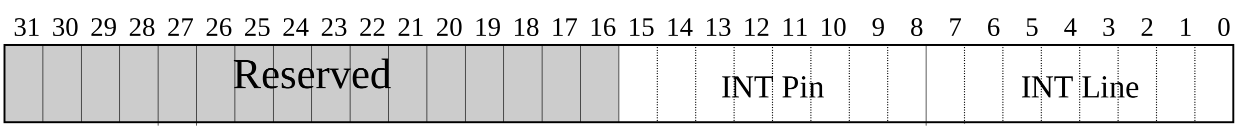
Name: **ROM Base Address Register**
Address Offset: **30H**
R/W Attribute: **Read/Write**
Reset Default: **00000000H**



Field		Description
bit[31:18]		**ROM base address**. It specifies the base address of the boot ROM address.
bit[17:1]		Hardwired to zero.
bit[0]		**ROM Address decode enable**

3.1.8 CFINT

Name: **Interrupt Configuration Register**
Address Offset: **3CH**
R/W Attribute: **Read/Write**
Reset Default: **00000100H**



Field		Description
bit[31:16]		Reserved
bit[15:08]		**INT pin selection**. Hardwired to 00000001 to indicate that PNIC uses INTA#.
bit[07:00]		**Interrupt Line**. This 8-bit register will be written by the POST software. The value of this register indicates which input of the system interrupt controller PNIC's interrupt pin is connected to.

3.1.9 CFDA

Name: **Driver Area Configuration Register**
Address Offset: **40H**
R/W Attribute: **Read/Write**
Reset Default: **00000000H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PD	Reserved															Driver Specail Area								Reserved							

Field		Description
bit[31]	PD	**Power down enable**. If this bit is set, the whole chip (including PHY block) will be powered down into sleep mode. In sleep mode, only configuration register space is available for host to access. To bring the chip out of the sleep mode, a “0” should be written into this bit.
bit[30:16]		Reserved
bit[15:08]	DR	**Driver special use area**. It is reserved for driver to specify the use of the register.
bit[07:00]		Reserved.

3.2 PNIC Tx/Rx command and status register set

It is summarized in the following table.

	OFFSET	SHORT NAME	FULL NAME
CSR0	00H	CBMOD	Bus configuration register
CSR1	08H	CTXPL	Transmit poll register (Write-only)
CSR2	10H	CRXPL	Receive poll register (Write-only)
CSR3	18H	CRXLA	Receive list base address
CSR4	20H	CTXLA	Transmit list base address
CSR5	28H	CSTAT	Tx/Rx operation Status Register
CSR6	30H	CCTRL	Control Register
CSR7	38H	CINTM	Interrupt mask register
CSR8	40H	CMISF	Missed Frame Counter
CSR9	48H	CROMD	Ethernet ID EEPROM data register
CSR10	50H		Reserved
CSR11	58H		Reserved
CSR12	60H	CGPRG	General purpose register
CSR13	68H		Reserved
CSR14	70H		Reserved
CSR15	78H	CENDC	ENDEC General register
CSR16	80H		Reserved
CSR17	88H		Reserved
CSR18	90H	CEPWR	EEPROM power-up register
CSR19	98H	CROMC	EEPROM control register
CSR20	A0H	CMIIM	MII management register
CSR21	A8H		Reserved
CSR22	B0H		Reserved
CSR23	B8H	CNWAY	N-way Auto-detection register

3.2.1.1 CSR0

Name: **Bus Configuration Register**
Address Offset: **00H**
R/W Attribute: **Read/Write**
Reset Default: **00000000H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												TAP				CAL		BLN						BLE	DSL					BAR	SRT

Field	NAME	Description
bit[31:20]		Reserved
bit[19:17]	TAP	**Transmit automatic polling.** PNIC automatically wakes up the suspended transmit process if TAP are set. The wake-up delays are defined as the following table:
	000	No automatic transmit polling. Writing transmit polling register, CSR1, is the only way to wake up the suspended process.
	001	PNIC automatically polls the transmit process every 200 microseconds.
	010	PNIC automatically polls the transmit process every 800 microseconds.
	011	PNIC automatically polls the transmit process every 1600 microseconds.
	100	PNIC automatically polls the transmit process every 12.8 miliseconds.
	101	PNIC automatically polls the transmit process every 25.6 miliseconds.
	110	PNIC automatically polls the transmit process every 51.2 miliseconds.
	111	PNIC automatically polls the transmit process every 102.4 miliseconds.
bit[16]		Reserved.
bit[15:14]	CAL	**Cache alignment**. If the address is not cache line aligned, PNIC initiates the transaction with the not aligned address followed by cache line aligned transaction. If the bridge between the PCI bus and the memory bus is able to insert transaction break on the cache boundary, PNIC should be programmed to do as much of burst transactions as possible in order to achieve optimum throughput.
	00	Not defined.
	01	8 doubleword boundary alignment.
	10	16 doubleword boundary alignment.
	11	32 doubleword boundary alignment.
bit[13:08]	BLN	**Programmable Burst length**. It specifies the maximum number of double-word that PNIC can do in one PCI burst transaction when PNIC is the master of the PCI bus. If BLN=0, the maximum number of double-word that PNIC can transfer through PCI bus is bounded by the valid data(>=16 double-words) in the receive FIFO and the available space(>=64 double-words) left in the transmit FIFO.
bit[07]	BLE	**Big/little Endian**. 0= little endian, and 1= big endian.
bit[06:02]	DSL	**Descriptor skip length**. It may maximize the system performance by placing each descriptor on cache line boundary. This field is programmed to skip a number of doublewords for the distance between two adjacent descriptors. This bit is meaningful only when descriptor is in ring structure.
bit[01]	BAR	**Bus arbitration**. When set to one, round robin scheme is applied to achieve the fair granting to both transmit process and receive process. Arbiter inside PNIC grants to each process in turns. If this bit is reset, PNIC favors the receive process to assure less packet lost. However, if PNIC starts

		transmitting a packet, PNIC will give the priority to the transmit process to avoid transmit FIFO underrun.
bit[00]	SRT	**Software reset**. When set, PNIC reset all the hardware but leave the configuration area unchanged.

3.2.2 CSR1

Name: **Transmit polling register**
Address Offset: **08H**
R/W Attribute: **Write Only**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															PE

Field	Name	Description
bit[31:01]		Reserved
bit[0]	TPE	**Transmit polling enable**. Any writes to this register resumes the transmit process.

3.2.3 CSR2

Name: **Receive polling register**
Address Offset: **10H**
R/W Attribute: **Write only**

31 … 1	0
Reserved	RPE

Field	Name	Description
bit[31:01]		Reserved
bit[0]	RPE	**Receive polling enable**. Writes to this register resumes the receive process.

3.2.4 CSR3

Name **Receive descriptor list base address register**
Address Offset: **18H**
R/W Attribute: **Read/Write**
Reset Default: **00000000H**

31 … 2	1 0
Receive descriptor list Base Address	Dont Care

Field		Description
bit[31:02]		**Base address of receive descriptor list**. This register points to the first descriptor of the receive descriptor list. It is strongly recommended that this register is written while receive process is in its STOP state.
bit[01:00]		Reserved

3.2.5 CSR4

Name: **Transmit descriptor list base address register**
Address Offset: **20H**
R/W Attribute: **Read/Write**
Reset Default: **00000000H**

31 … 2	1 0
Transmit descriptor list Base Address	Dont Care

Field		Description
bit[31:02]		**Base address of transmit descriptor list.** This register points to the first descriptor of the transmit descriptor list. It is strongly recommended that this register is written while transmit process is in its STOP state.
bit[01:00]		Reserved

3.2.6 CSR5

Name: **Tx/Rx Operation Status register**
Address Offset: **28H**
R/W Attribute: **Read/Write**
Reset Default: **02001102H**

31 30 29 28 27	26	25 24 23	22 21 20	19 18 17	16	15	14	13	12	11 10	9	8	7	6	5	4	3	2	1	0
Reserved		System error type	Tx Process state	Rx Process state	NSI	ASI		SE	LF	Reserved	RTO	RPS	RNA	RC	TUR	LP	TJTO	TNA	TPS	TC

Field	Name	Description	
bit[31:27]		Reserved	
bit[26]		**Tx abort.** It is due to error summary bit from the Tx status field in the Tx descriptor.	
bit[25:23]		**System error type.** It encodes the type of system error that PNIC run into.	
		Type	**Restore Scheme**
	000	Parity error.	Software Reset, CSR[0]=1.
	001	Master abort.	System error, CSR5[13]=1, set and system error interrupt if it is enabled CSR7[13]=1.
	010	Target abort.	System error, CSR5[13]=1, set and system error interrupt if it is enabled CSR7[13]=1.
	011	Reserved.	
	1xx	Reserved.	
bit[22:20]		**Transmit process state**	
	000	**Tx Stop state:** After reset or when Tx start bit is off, PNIC is in this state.	
	001	**Descriptor Fetch State:** PNIC reads 4 doublewords of Tx descriptor.	
	010	**Wait end of frame state:** In this state, PNIC will wait for end of frame from MAC control.	
	011	**Tx buffer read state:** PNIC reads Tx buffer data in this state.	
	100	**Tx abort state:** When PNIC detects Tx error, it will enter this state.	
	101	**Setup frame state:** This is a state where PNIC processes setup frame.	
	110	**No buffer state:** When PNIC detects no Tx buffer available, it will enter this state.	
	111	**Descriptor close state:** This is the state where PNIC closes the Tx descriptor.	
bit[19:17]		**Receive process state**	
	000	**Rx stop state:** After reset or before Rx start bit is set to one, PNIC will be in this state.	
	001	**Descriptor fetch state:** PNIC reads 4 doublewords of Rx descriptor.	
	010	**Prefetch state:** This is a state where PNIC fetches next descriptor.	
	011	**Wait for Rx frame state:** PNIC waits for incoming Rx frame.	
	100	**No buffer available state:** When PNIC detects no Rx buffer, it enters this state.	
	101	**Descriptor close state:** This is the state where PNIC closes Rx descriptor.	
	110	**Rx dump state:** This is a state where PNIC dumps Rx frame from the Rx FIFO.	

	111	**Buffer write state:** PNIC writes Rx data into Rx buffer.
bit[16]	NSI	**Normal status interrupt** It is the logical OR of: • transmit complete, CSR5[0]. • transmit buffer not available, CSR[2]. • receive complete, CSR5[6].
bit[15]	ASI	**Abnormal status interrupt**. It is the logical OR of the following interrupts • System error, CSR5[13]. • Link test fail, CSR5[12]. • receive watchdog time-out, CSR5[09]. • receive process stop, CSR5[08]. • receive buffer not available, CSR5[07] • transmit underrun, CSR5[05]. • transmit jabber time-out, CSR5[03]. • transmit process stop, CSR5[01].
bit[14]		Reserved
bit[13]	SE	**System error.** It means a system error has happen. The error type is defined in CSR5[25:23].
bit[12]	LF	**Link test fail.** A link fail has occurred in the twisted-pair lines. Refer to CSR12[2] for the link fail status.
bit[11:10]		**Reserved -**
bit[09]	RTO	**Receive watchdog time-out.** When set, the receive watchdog timer has expired. The other nodes on the network may have been babbling. The reception of the current frame will be aborted. PNIC closes the receive descriptor with length error, RD0[14], and last descriptor, RD0[8], set. The Abnormal interrupt CSR5[15] will be set and the receive process remains in running state.
bit[08]	RPS	**Receive process stopped.** Indicate that the receive process has been stopped.
bit[07]	RNA	**Receive buffer not available**. The next descriptor that PNIC tries to acquire is not available. The OWN bit, RD0[31], is zero. Receive process will go into pending state waiting for polling command or next recognized incoming packet to wake up the receive process. To resume the process, the host should change the ownership of the descriptor and issue a polling command.
bit[06]	RC	**Receive complete.** At the completion of receiving a frame, PNIC has moved data from the receive FIFO to the host memory. PNIC sets this bit and closes the descriptor with proper status bits set.
bit[05]	TUR	**Transmit underrun.** The transmit FIFO underruns. Transmit process will be suspended.
bit[04]	LP	**Link test pass.** This is the inversion of bit[12].
bit[03]	TJTO	**Transmit jabber time-out.** Jabber time-out timer expired. Transmitter was babbling. PNIC stops the transmit process immediately and sets this bit to one.
bit[02]	TNA	**Transmit buffer not available.** The host did not set the OWN bit, TD0[31l, to one. Transmit process is suspended. To resume the process, the host has to initiate a poll command. If the automatic polling is used, PNIC wakes up the transmit process automatically.
bit[01]	TPS	**Transmit process stopped.** Transmit process has been stopped.
bit[00]	TC	**Transmit complete.** After successfully transmitting a frame to the media, PNIC sets this bit and closes the descriptor with proper status bits set.

3.2.7 CSR6

Name: **Tx/Rx Control register**
Address Offset: **30H**
R/W Attribute: **Read/Write**
Reset Default: **00000040H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	EED	DRC	Reserved				SM	CSM	MSP	SF	IT	DHB	MEN	TBEN		TC		TXEN	FCM	OP Mode		FDEN	R	RMC	PM	SBC	INFT	RBF	HOFT	RXEN	HPFT

Field	Name	Description
bit[31]		Reserved
bit[30]	EED	**External ENDEC enable**. If this bit is set, PNIC's internal 10Mbps PHY will not be used for Tx or Rx frames. Instead, it will use external ENDEC device.
bit[29]	DRC	**Receive CRC disable.** If set to one, Rx CRC words will not be moved to the Rx buffer.
bit[28:25]		Reserved
bit[24]	SM	**Scrambler and Descrambler enable**. When this bit is set to one, the scrambler and descrambler functions will be active for Tx and Rx frames. This bit is valid only for 100BASE-TX mode.
bit[23]	CSM	**CS mode enable**. When set, 100BASE-TX mode is active.
bit[22]	MSP	**Media speed.** 1= 10Mbps; 0= 100Mbps. See attached table.
bit[21]	SF	**Store and forward**. When set, PNIC reads the whole packet from the host memory to transmit FIFO first, then starts to transmit.
bit[20]	IT	**Immediate Tx.** When set, PNIC does not care for the transmit FIFO threshold. Whenever there is data in the FIFO, PNIC transmits out to the media right away. Unless the PCI bus bandwidth is allocated to the PNIC, setting this bit may cause transmit FIFO underrun.
bit[19]	DHB	**Heart beat disable.** When set, SQE test will be disabled.
bit[18]	MEN	**MII/SYM enable**.(1= MII/SYM; 0= int/ext ENDEC)
bit[17]	TBEN	**Tx backoff offset enable.**
bit[16]		Reserved.
bit[15:14]	TC	**Transmit threshold control bits.** It defines the number of bytes read into the transmit FIFO before the transmission. If the frame length is less than the threshold value, PNIC will start to transmit after a full frame is in the FIFO. To modify these bits, it is recommended to stop the transmit process.
	00	72 Bytes
	01	96 Bytes
	10	128 Bytes
	11	160 Bytes
bit[13]	TXEN	**Transmit enable**. When set, transmit process goes into running status. If CSR4 has not been accessed, PNIC reads the descriptor from the top of the list. Otherwise, PNIC fetches the one after the descriptor closed before it was stopped. When reset, PNIC completes transmission then stops the transmit process. The next descriptor address is saved. When transmit process is enabled again, PNIC will start from the saved location for the first descriptor.
bit[12]	FCM	**Force collision mode**. When set, collision is forced to the next transmission in order to test the collision logic in PNIC. This feature is only meaningful when PNIC is running in internal loopback mode. 16 attempts in transmission causes a excessive collision report in TD0[8].

bit[11:10]	OP Mode	**Operating mode**.(01 = int loopback; 10 = ext.loopback; 00 = normal operation.)
bit[09]	FDEN	**Full duplex mode enable**. When enabled, PNIC operates in a full-duplex mode. PNIC transmits and receives simultaneously. When duplex is enabled, heartbeat check is disabled and the heartbeat fail in TD0[7] should be ignored.
bit[08]		Reserved
bit[07]	RMC	**Receive multicast**. When set, all multicast addresses are received. The physical address is still checked with the filtering logic.
bit[06]	PM	**Promiscuous mode**. When set, PNIC receives all the packets on the media. After reset, PNIC goes into promiscuous mode immediately.
bit[05]	SBC	**Stop backoff counter on carrier**.
bit[04]	INFT	**Inverse filtering**. The setup frame determines the type of address filtering that PNIC is adopting. When this bit set, PNIC rejects the addresses which match the address table and receives the ones do not match any entries in the address table. This is a read-only bit. This function can be enabled in the control field of the Rx descriptor.
bit[03]	RBF	**Receive bad frame**. When set, PNIC receives all packets pass the address filtering. It includes runt frames, collided fragments or the truncated frames.
bit[02]	HOFT	**Hash only filtering mode enable**. The setup frame sets up the filtering type. When set, hash function is applied to the address of every incoming packet. If the corresponding bit is set in the hash table, PNIC receives the packet. Otherwise, it rejects the packet. This is a read-only bit. This function can be enabled in the control field of the Rx descriptor.
bit[01]	RXEN	**Receive enable**. When set, receive process goes into running status. If CSR3 has not been accessed, PNIC reads the descriptor from the top of the list. Otherwise, PNIC fetches the one after the descriptor closed before the process was stopped.
bit[00]	HPFT	**Hash/perfect filtering mode enable.** The setup frame defines the address filtering type. When set, PNIC compares the physical address with the only physical entry in the table. On the other hands, PNIC looks up the hash table for the multicast addresses. This is a read-only bit. This function can be enabled in the control field of the Rx descriptor.

- Media type and speed selection is summarized in the following table:

bit30	bit23	bit22	bit18	Description
x	x	1	1	MII 10Mbps
0	x	x	0	Internal ENDEC
1	x	x	0	External ENDEC
x	0	0	1	MII 100Mbps
x	1	0	1	100BASE-TX

- NOTE: x stands for “Don’t care.”.

3.2.8 CSR7

Name: **Interrupt enable register**
Address Offset: **38H**
R/W Attribute: **Read/Write**
Reset Default: **00000000H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					TMIE	Reserved									NSIE	ASIE		SEIE	LFIE	Reserved		RTOE	RPSE	RNAE	RCIE	TURE	LPIE	TJTE	TNAE	TPSE	TCIE

Field	Name	Description
bit[31:27]		Reserved
bit[26]	TMIE	Tx MAC abort interrupt enable
bit[25:17]		Reserved
bit[16]	NSIE	**Normal status interrupt enable.** When set, Normal status interrupt is enabled. When reset, PNIC does not report Normal status interrupt. It masks the following bits: CSR5[0], transmit complete. CSR5[2], transmit buffer unavailable. CSR5[6], receive complete.
bit[15]	ASIE	**Abnormal status interrupt enable**. When set, Abnormal status interrupt report is enabled. When reset, PNIC does not report the abnormal status interrupt. It masks the following bits: CSR5[1], transmit process stop. CSR5[3], transmit jabber time-out. CSR5[5], transmit underflow. CSR5[7], receive buffer unavailable. CSR5[8], receive process stop. CSR5[9], receive watchdog time-out. CSR5[12], link fail. CSR5[13], system error.
bit[14]		Reserved
bit[13]	SEIE	**System error interrupt enable**. When set with CSR7[15] set, PNIC enables the system error interrupt report. When reset or the abnormal status interrupt enable is reset, PNIC does not report system error interrupt.
bit[12]	LFIE	**Link fail interrupt enable**. When set with the abnormal status interrupt enable set, PNIC reports link fail interrupt.
bit[11:10]		Reserved
bit[09]	RTOE	**Receive watchdog time out interrupt enable**. When set with the abnormal status interrupt enable set, PNIC reports receive watchdog time-out interrupt.
bit[08]	RPSE	**Receive stopped interrupt enable**. When set with the normal status interrupt enable set, PNIC reports the receive process stopped interrupt.
bit[7]	RNAE	**Receive buffer unavailable interrupt enable**. When set with the abnormal status interrupt enable set, PNIC posts the receive buffer unavailable interrupt.
bit[06]	RCIE	**Receive complete interrupt enable**. When set with the normal status interrupt enable set, PNIC posts the receive complete interrupt.
bit[05]	TURE	**Transmit underrun interrupt enable**. When set with the abnormal status interrupt enable set, PNIC posts the transmit underrun interrupt.
bit[04]	LPIE	**Link test pass interrupt enable**.
bit[03]	TJTE	**Transmit jabber time-out interrupt enable**. When set with the abnormal status interrupt enable set, PNIC posts the jabber time-out interrupt.
bit[02]	TNAE	**Transmit buffer unavailable interrupt enable**. When set with the normal status interrupt enable set, PNIC posts the transmit buffer not available interrupt.
bit[01]	TPSE	**Transmit stopped interrupt enable.** When set with the abnormal status interrupt enable set, PNIC posts the transmit process stopped interrupt.
bit[00]	TCIE	**Transmit complete interrupt enable** When set with the normal status interrupt enable set, PNIC posts the transmit complete interrupt.

3.2.9 CSR8

Name: **Missed frame counter**
Address Offset: **40H**
R/W Attribute: **Read only**
Reset Default: **00000000H**

31 … 17	16	15 … 0
Reserved	OF	Missed frame Counter[15:0]

Field		Description
bit[31:17]		Reserved
bit[16]	OF	**Missed frame counter overflow**. When set, the miss frame counter is overflowed. The value in the counter is not reliable.
bit[15:00]		**Missed frame counter**. PNIC reports number of Rx frames that are dropped from Rx FIFO. Reading this register will reset this counter.

3.2.10 CSR9

Name: **Serial EEPROM data register**
Address Offset: **48H**
R/W Attribute: **Read/Write**
Reset Default: **0000FFFFH**

31	30 … 16	15 … 0
B	Reserved	EEPROM DATA[15:0]

Field		Description
bit[31]	B	**Busy**, When set, data cannot be written to EEPROM data register and data read from EEPROM data register is not valid. This is a read-only bit.
bit[30:16]		Reserved
bit[15:00]		**EEPROM data**, Data to be written to EEPROM or data read from EEPROM.

- NOTE: In order to write data into EEPROM, data register need to be written prior to the control register.

3.2.11 CSR12

Name: **General purpose register**
Address Offset: **60H**
R/W Attribute: **Read/Write**
Reset Default: **0000000FH**

31 … 8	7 … 4	3 … 0
Reserved	GP control	GP DATA

Field		Description
bit[31:08]		Reserved
bit[08:04]		**General purpose control**, 0 = inputs, 1 = outputs. bit[4] controls GENP[0] pin, bit[5] controls GENP[1] pin, bit[6] controls GENP[2] pin and bit[7] controls GENP[3].
bit[03:00]		**General purpose data**. These bits are the source or the destination of the GENP[3:0] pins depending on the corresoponding control bit. When the corresponding control bit is reset to zero, the value of GENP pins will be recorded in this register. On the other hands, if the correspoding control bit is set, data in this register will be sent out on the corresponding GENP pins.

3.2.12 CSR15

Name: **ENDEC General register**
Address Offset: **78H**
R/W Attribute: **Read/Write**
Reset Default: **00000000H**

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
Reserved	JDIS

Field		Description
bit[31:0]		Reserved
bit[00]	JDIS	**Jabber disable**. When set, the Tx jabber timer will be disabled.

3.2.13 CSR18

Name: **Serial EEPROM power-up register**
Address Offset: **90H**
R/W Attribute: **Read only**
Reset Default: **N/A**

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2	1	0
To be assigned.	CB	MCE

Field		Description
bit[31:02]		To be assigned.
bit[01]	CB	**Cache boundary alignment burst type**. 1= burst until it reaches cache boundary, 0= single cycle until it reaches boundary.
bit[00]		**Memory read line command enable.**

After hardware reset, serial EEPROM interface block should hold the whole chip in reset while it is in the process of extracting data at location 3 and 4 (address 03 and 04 in bank 0) from external serial EEPROM into power-up register. This way, some initial chip configuration information can be prestored in the serial EEPROM. This will make PNIC adapter card truly jumperless.

Address location 00 through 02 in the serial EEPROM are used to store Ethernet ID address.

3.2.14 CSR19

Name: **Serial EEPROM control register**
Address Offset: **98H**
R/W Attribute: **Read/Write**
Reset Default: **00000000H**

31	30 – 10	9 – 8	7 – 6	5 – 0
B	Reserved	OP Code	Reserved	Read/Write Address

Field	Name	Description
bit[31]	B	**Busy**, This bit has the same function as CSR9 bit[31]. (This bit is read only.)
bit[30:10]		Reserved
bit[09:08]		**Op-code** (see the next table for definition).
bit[07:06]		Reserved
bit[05:00]		**EEPROM read/write address.** (see the next table for definition).

- **The Op-code and the most significant two bits of the address are defined in the following table:**

OP-code	ADDR[05:04]	Description
11	XX	Erase the register specified by address.
10	XX	Read the data in the register specified by address
01	XX	Write the register specified by address
00	11	Enable writes to EEPROM. This command must precedes all write/erase commands.
00	10	Ease all register in EEPROM.
00	01	Write all register in EEPROM with data in CSR9(EEPROM data register).
00	00	Disable all write/erase modes.

3.2.15 CSR20

Name: **MII management register**
Address Offset: **A0H**
R/W Attribute: **Read/Write**
Reset Default: **40020000H**

31	30	29 – 28	27 – 23	22 – 18	17	16	15 – 0
B	1	OP Code	Physical Address	Register Address	1	0	Read/Write Data

Field		Description
bit[31]	B	**Busy**, (This bit is read only.)

bit[30]		Hard-wired to 1.
bit[29:28]		**Op-code**.
	10	Read the data in the register specified by address.
	01	Write the register specified by address.
bit[27:23]		**Physical address**. 00000 is used to address physical interface that connect to MII mechanical connector. See IEEE 802.3u MII Spec.
bit[22:18]		**Register address**. 00000 is for control register. 00001 is for status register. See IEEE 802.3u MII Spec.
bit[17:16]		Hard-wired to 10.
bit[15:00]		**read/write data**.

The contents of this register is shifted out to a PHY device after a 32-bit patterns of '1' have been shifted out. bit 31 of this register is shifted first, bit 0 is shifted last. As a result, the bit patterns appear at the MDIO pin for a read operation are shown as follows:

<1....1><01><10><AAAAA><RRRRR><Z0><DDDDDDDDDDDDDDDD><Z>

The bit patterns appear at the MDIO pin for a write operation should look as follows:

<1....1><01><01><AAAAA><RRRRR><10><DDDDDDDDDDDDDDDD><Z>

PHY address, register address and read/write data fields are transmitted or received MSB first. For more information in regard to the usage of this register related to a PHY device, please consult IEEE 802.3 MII spec.

3.2.16 CSR23

Name: **N-way register**
Address Offset: **B8H**
R/W Attribute: **Read/Write**
Reset Default: **02000078H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T4	XM	XF	TF	TM	RF	RN				Reserved						Defined in the table.			NW	10/100	DM	DL	FD	AF	TP	DX	LU	LC	BX	PD	RS

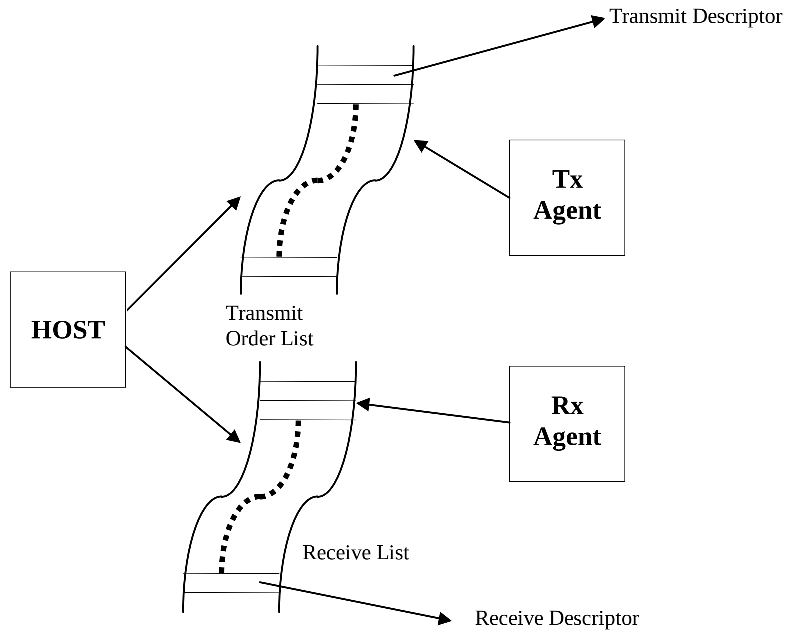
Field	Name	Description
bit[31]	T4	**N-way accepted 100BASE-T4 mode**. (Read-only). It indicates that 100BASE-T4 is accepted after N-way negotiation.
bit[30]	XM	**N-way accepted 100BASE-TX mode**. (Read-only) It indicates that 100BASE-TX is accepted after N-way negotiation.
bit[29]	XF	**N-way accepted 100BASE-TX full duplex**.(Read only). It indicates that 100BASE-TX full duplex is accepted after N-way negotiation.
bit[28]	TF	**N-way accepted 10BASE-T full duplex**. (Read-only) It indicates that 10BASE-T full duplex is accepted after N-way negotiation
bit[27]	TM	**N-way accepted 10BASE-T mode**. (Read-only) It indicates that 10BASE-T is accepted after N-way negotiation
bit[26]	RF	**Remote fault bit**. When it is written, this bit will be sent to the network by N-Way logic. when this bit is read, this bit reflects the Remote Fault bit received by N-Way logic from the network.

bit[25]	RN	**Re-negotiation enable**. When this bit is written, a signal pulse is generated to tell the N-way logic to re-negotiate. While the N-way logic is negotiating, this bit remains set. After negotiation is done, N-way logic resets this bit to indicate the end of re-negotiation.
bit[24:18]		reserved
bit[17]		**Capable of supporting 100BASE-T4 mode**. This bit tells N-way logic that this chip is capable of supporting 100BASE-T4 operation.
bit[16]		**Capable of supporting 100BASE-TX mode**. This bit tells N-way logic that this chip is capable of supporting 100BASE-TX operation.
bit[15]		**Capable of supporting 100BASE-TX full duplex**. This bit tells N-way logic that this chip is capable of supporting 100BASE-TX full duplex operation.
bit[14]		**Capable of supporting 10BASE-T full duplex**. This bit tells N-way logic that this chip is capable of supporting 10BASE-T full duplex operation.
bit[13]		**Capable of supporting 10BASE-T mode**. This bit tells N-way logic that this chip is capable of supporting 10BASE-T operation.
bit[12]	NW	**N-Way auto-detection enable**. When set, N-way logic is enabled.
bit[11]	10/100	**10/100 speed selection**. 0= 10Mbps, 1= 100Mbps.
bit[10]	DM	**Disable media auto-detection of AUI/TP**. When reset, PNIC automatically detects AUI or TP.
bit[09]	DL	**Disable link integrity test**. When reset, link integrity test is enabled.
bit[08]	FD	**Full duplex mode**. When set, full duplex is enabled.
bit[07]	AF	**AUI Full or Half step**. When set, AUI idle output voltage = 2.5V(Full step). Otherwise. AUI idle output voltage = 0V.
bit[06]	TW	**Select twist pair media**.(Default to 1).
bit[05]	DX	**Disable X-polarity correction function**.(Def.1). When reset, PNIC automatically corrects the polarity error on the TW input signals.
bit[04]	UV	**Set twist pair receiver with low unsquelch voltage**. (Default to 1). When set, PNIC supports extended cable length longer than 100 meters.
bit[03]	LC	**Set AUI driver at low current mode**.(Def.1) When set, AUI transmit is terminated.
bit[02]	BX	**Bypass transceiver, analog driver tri-state**. When set, analog transmit circuit is turned off. It is in high impedance state.
bit[01]	PD	**Power down all logic in the PHY interface block, all current shut off**.
bit[00]	RS	**Reset all logic in the PHY interface block**.

NOTE: if bit[01] and bit[00] are set, the whole internal analog block will be powered down. If bit[01] bit is set and bit[00] is not set, all analog logic are shut off except the Tx jabber timer which requires running to serve 100BASE-TX protocol.

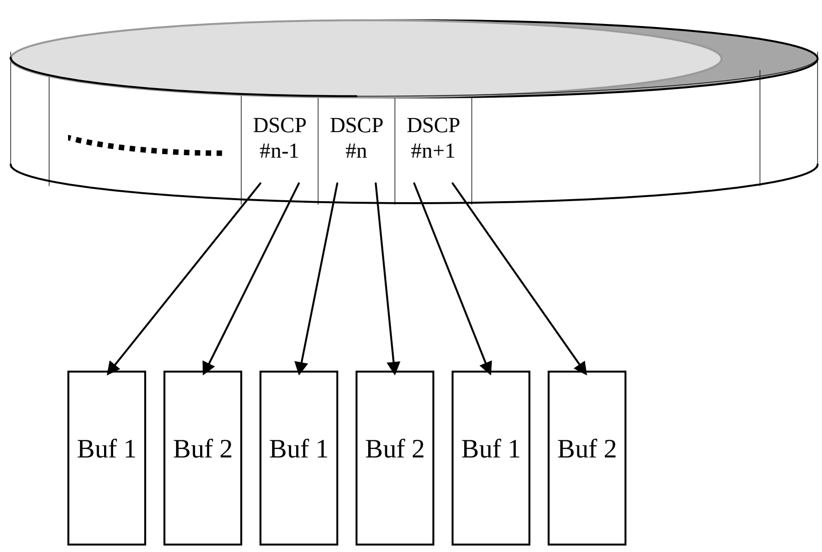
4. Communication between the Host and the Agents

Communication between the host and the agents are conducted through two descriptor lists: the transmit descriptor list and the receive descriptor list.

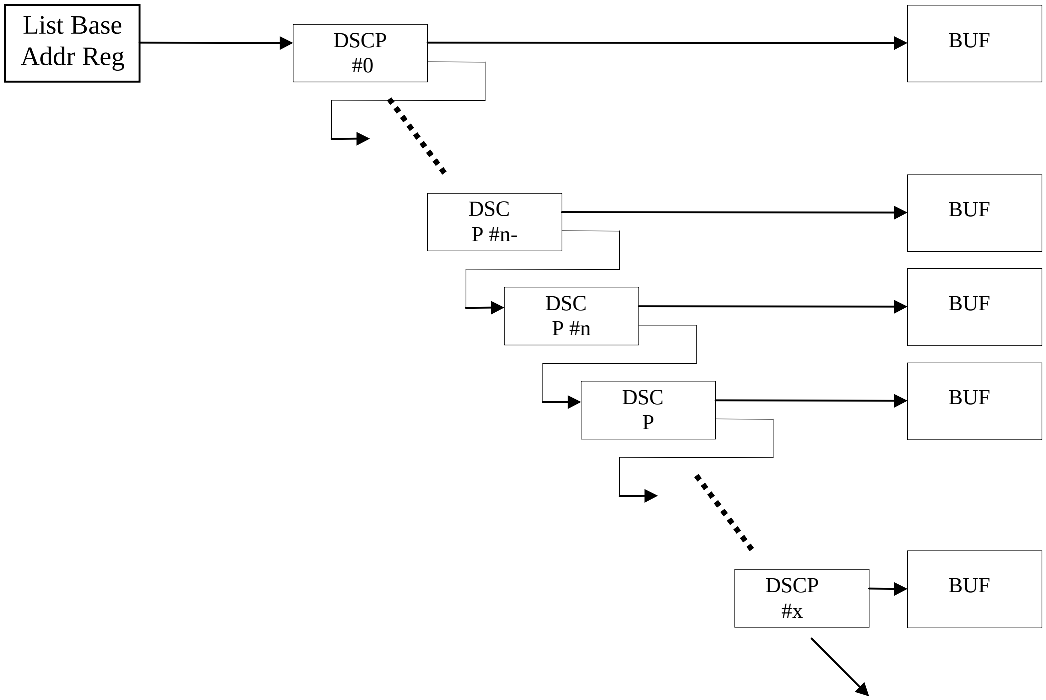


These two lists could be built either in a physical ring structure or in a link list structure. In the physical ring structure, descriptors are resided in a continuous address space. The last descriptor ends the list by setting End of Ring bit, so PNIC will loop back to the beginning of the list to form a ring. In the link list structure, the address of the next descriptor is specified by the current descriptor.

Physical ring structure:



Link list structure:



4.1 Transmit Descriptor

	31			0
TD0	OWN	Status		
TD1	Control Bits	Buffer1 Size in Byte	Buffer2 Size in Byte	
TD2	Buffer1 Base Address pointer			
TD3	Buffer2 Base Address/Next DSCP Pointer			

For transmission, PNIC scans the transmit descriptor list to get the transmit commands. The host prepares the data in the packet buffer, then fills up the transmit descriptors and returns the ownership back to the PNIC by setting TD0[31]

.

Every descriptor includes four parts: TD0, TD1, TD2 and TD3.

- TD0 contains the Transmit Status. It is the information that PNIC sends back to the host at the end of the transmission. At the end of a transmission, with or without errors, PNIC writes Transmit Status in the last descriptor of the transmitted packet.
- .TD1 TD2 and TD3 contain the control information as well as the buffer size and buffer location. The host fills up TD1, TD2 and TD3 to specify the service and data of the transmission.

4.1.1 TD0, Transmit Status Words

31	30–16	15	14	13	12	11	10	9	8	7	6–3	2	1	0
OWN	Reserved	ES	TO		ID	LO	NC	LC	EC	HF	CC CNT[3:0]	LF	UF	DF

Field		Description
bit[31]	OWN	**OWN**, When set the descriptor belongs to the PNIC. Data in the transmit buffer is ready for transmit. PNIC will read it from the host memory to the on-chip transmit FIFO. If the OWN bit is reset, PNIC will set transmit buffer unavailable, CSR5[2], to report that PNIC tried to open descriptor unsuccessfully. PNIC reset the bit when it closes the descriptor.
bit[30:16]		Reserved.
bit[15]	ES	**Error Summary**. It is the logic OR of the following bits: TD0[1], underflow error. TD0[2], link fail. TD0[8], excessive collision. TD0[9], late collision. TD0[10], no carrier. TD0[11], lost of carrier. TD0[14], transmit jabber time-out.
bit[14]	TO	**Transmit Jabber Time-out**. When set, the transmit jabber timer expired. PNIC's transmitter is babbling. PNIC sets the jabber time-out interrupt CSR5[3] and aborts the transmit process right away. After closing the descriptor with transmit jabber time-out, PNIC jumps into transmit STOP

		state.
bit[13]		Reserved.
bit[12]	ID	**Illegal descriptor**. When set, PNIC has fetched an undefined descriptor. PNIC closes the descriptor with this bit set and goes to Tx Abort state.
bit[11]	LOA	**Lost of Carrier**. When set, carrier is lost during the transmission. PNIC closes the descriptor with lost of carrier and goes to Tx Abort state.
bit[10]	NC	**No Carrier**. When set, carrier is not present during the transmission. PNIC closes the descriptor and goes to Tx Abort state.
bit[9]	LC	**Late Collision**. When set, PNIC has run into a collision after the collision window of 64 bytes. This bit should be ignored if transmit FIFO underflow error, TD0[1], is set.
bit[8]	EC	**Excessive Collisions**. When set, transmission was aborted because of 16 consecutive collision.
bit[7]	HF	**Heartbeat failure**. When set, it means SQE test fails.
bit[6:3]	CC	**Collision Count**. Number of collision before the frame is transmitted. When excessive collision is set, ignore these bits.
bit[2]	LF	**Link Fail**. When set, link fail test failed.
bit[1]	UF	**Underflow Error**. When set, transmission was aborted because the transmit FIFO is underflow. It may be caused by PCI bus overloaded or low threshold in the transmit FIFO.
bit[0]	DE	**Deferred**. When set, frame was delayed to be transmitted because of the carrier was asserted.

4.1.2 TD1, Transmit Control Words

31	30	29	28	27	26	25	24	23	22	21–11	10–0
IC	LS	FS	FT	SP	CD	ER	LR	DP	FT	BUF2 Size[10:0]	BUF1 Size[10:0]

Field		Description
bit[31]	IC	**Interrupt on Completion**. When set, PNIC sets the CSR5[0] at the end of transmission. This bit is valid only when the last segment bit, TD1[30], is set.
bit[30]	LS	**Last Segment**. The last segment of the frame. When PNIC sees this bit set, it knows the data in the Tx buffer of the current descriptor is the last Tx data of the current frame.
bit[29]	FS	**First Segment**. The first segment of the frame. After finishing the previous frame, PNIC scans though the transmit descriptor list to find the descriptor with first segment bit set. The descriptors between the last segment of the frame and the first descriptor of the next frame are no-op descriptors. PNIC skips those no-op descriptors by resetting the OWN in TD0[31].
bit[28]	FT1	**Filter Type bit1**. (see definition in section 5.4). PNIC ignores this bit when setup packet, TD1[27], is reset.
bit[27]	SP	**Setup Packet**. When set, the packet is to define the filtering table. It is for internal table setup only, PNIC does not transmit the data out to the media.
bit[26]	CD	**Disable CRC at the end**. When set, the media agent does not attach CRC value at the end of the packet.
bit[25]	ER	**End of the Transmit Ring**. When set with Ring bit set, this descriptor is the last descriptor in the descriptor list. PNIC will loop back the base of the descriptor list for the next descriptor. In Link-list structure, this bit is ignored.

bit[24]	CH	**Link list enable**. When set, the descriptor list is constructed in a link-list structure. TD3 is the pointer of the next descriptor..
bit[23]	DP	**Disable padding**. When set, the media agent does not pad extra bits at the end of the packet if the frame is less than 64 bytes long. This bit is ignored if the last segment, TD1[30], is not set.
bit[22]	FT0	**Filter Type bit0**. see definition in section 5.4). PNIC ignores this bit when setup packet, TD1[27], is reset
bit[21:11]	BS2	**Buffer2 Size.** Number of bytes in the second data buffer. In Link-list structure, TD1[24] is set, these bits are ignored.
bit[10:0]	BS1	**Buffer1 Size.** Number of bytes in the second data buffer.

4.1.3 TD2, Transmit Buffer1 Base Address Pointer

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Buffer1 Base Address																															

Field		Description
bit[31:0]]	BA1	**Buffer1 Base Address[31:0].** This is the buffer pointer that points to the location of the Tx data buffer1.

4.1.4 TD3, Transmit Buffer2 Base Address Pointer or Next Descriptor Pointer

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Buffer2 Base Address/Next DSCP Pointer																															

Field		Description
bit[31:0]	BA2/ NDP	**Buffer2 Base Address[31:0]. or Next Descriptor Pointer[31:2].** In the ring structure, this is the buffer pointer that points to the location of the Tx data buffer2. In the Link-list structure, it points to the next descriptor. Descriptors are doubleword aligned, so the least significant two bits are ignored.

4.2 Receive Descriptor

	31			0
RD0	OWN	Status		
RD1	Control Bits	Buffer1 Size in Byte	Buffer2 Size in Byte	
RD2	Buffer1 Base Address Pointer			
RD3	Buffer2 Base Address Pointer/Next Descriptor Pointer			

4.2.1 RD0, Receive Status Words

31	30–16	15	14	13–12	11	10	9	8	7	6	5	4	3	2	1	0
OWN	Frame Length[14:0]	ES	LE	DT[1:0]	RF	MF	FS	LS	FL	CS	FT	R		DB	CE	OF

Field		Description
bit[31]	OWN	**OWN**. When set the descriptor belongs to the PNIC. If the OWN bit is reset, PNIC sets receive buffer unavailable, CSR5[7] and suspends the receive process. PNIC resets the bit when it closes the descriptor.
bit[30:16]	FL	**Frame Length[14:0].** Length in bytes of the received frame including the CRC. Ignore these bits when last segment, RD0[8], is set and Length Error, RD0[14], is set.
bit[15]	ES	**Error Summary**. It is the logical OR of the following bits: RD0[0], FIFO overflow. RD0[1], CRC error. RD0[6], collision seen. RD0[7], frame too long. RD0[11], runt frame. RD0[14], length error. This bit is valid only when last segment is set.
bit[14]	LE	**Length Error**. If PNIC detects an unavailable buffer when it pre-fetches the next descriptor, PNIC truncates the frame and set this bit.. This bit is valid only when last segment is set.
bit[13:12]	DT	**Data Type**.
	00	Serial received frame (normal operation).
	01	Internal loopback frame.
	10	External loopback frame.
	11	Reserved**.**
bit[11]	RF	**Runt Frame**. When set, the received frame is corrupted by premature termination before the collision window had passed. This only happens when pass bad frames bit, CSR6[3], is set. Ignore this bit when last segment,

		RS0[8], is reset or overflow, RS0[0], is set.
bit[10]	MF	**Multicast Frame**. When set, the frame received frame is a multicast frame. This bit is valid only when last segment, RS0[8], is set.
bit[9]	FS	**First segment**. When set, the buffer is the first segment of the received frame.
bit[8]	LS	**Last segment**. When set, the buffer is the last segment of the received frame.
bit[7]	FL	**Frame too long**. When set, the received frame is longer than the maximum Ethernet specified length 1518 bytes.
bit[6]	CS	**Collision seen**. When set, a late collision after the collision window has happened during receiving of the frame. This bit is valid only if the last segment is set.
bit[5]	FT	**Frame Type**. When set, it is an Ethernet type frame. Otherwise, it is an IEEE 802.3 frame.
bit[4]	RW	**Receive Watchdog time-out.** When PNIC receives a frame longer then 2048 bytes, PNIC set this bit. When this bit is set, the frame length in RD0[30:16] is not valid. When watchdog timer expired, PNIC does not set length error. This bit is valid only when last segment is set.
bit[3]		Reserved
bit[2]	DB	**Dribbling bit**. When set, the received frame is not a integer multiple byte frame. This bit is reported only if the dribbling bits are more than 2 bits. This bit is not valid if the runt frame, RD0[11], is set or collision seen, RD0[6], is set. This bit is valid only when last segment is set.
bit[1]	CE	**CRC error**. When set, Cyclic redundancy check failed.
bit[0]	OF	**Rx-FIFO Overflow**. When set, the receive FIFO is full. PNIC flushes the receive FIFO and closes the descriptor with this bit set. The frame is truncated. This bit is valid only when last segment is set.

4.2.2 RD1, Receive Control Words

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						ER	LR			BUF2 Size[10:0]											BUF1 Size[10:0]										

Field		Description
bit[31:26]		Reserved.
bit[25]	ER	**End of the Receive Ring**. When set with Link-list structure bit reset, this descriptor is the last descriptor in the descriptor list. PNIC will loop back the base of the descriptor list for the next descriptor. In Link-list structure, this bit is ignored
bit[24]	CH	**Link-list structure**. When set, the descriptor list is constructed in a Link-list structure. RD3 is the pointer of the next descriptor.
bit[23:22]		Reserved.
bit[21:11]	BS2	**Buffer2 Size.** Number of bytes in the second data buffer. In Link-list structure, RD1[24] is set, these bits are ignored.
bit[10:0]	BS1	**Buffer1 Size.** Number of bytes in the second data buffer.

4.2.3 RD2, Receive Buffer1 Base Address Pointer

31–0
Buffer1 Base Address

Field		Description
bit[31:0]	BA1	**Buffer1 Base Address[31:0].** This is the buffer pointer that points to the location of the Receive data buffer1.

4.2.4 RD3, Receive Buffer2 Base Address Pointer or Next Descriptor Pointer

31–0
Buffer2 Base Address/Next DSCP Pointer

Field		Description
bit[31:0]	BA2/ NDP	**Buffer1 Base Address[31:0]. or Next DSCP Pointer[31:2].** In ring structure, this is the buffer pointer that points to the location of the receive data buffer2. In the Link-list structure, it points to the next descriptor. Descriptors are doubleword aligned, so the least significant two bits are ignored.

5. Functional Operation

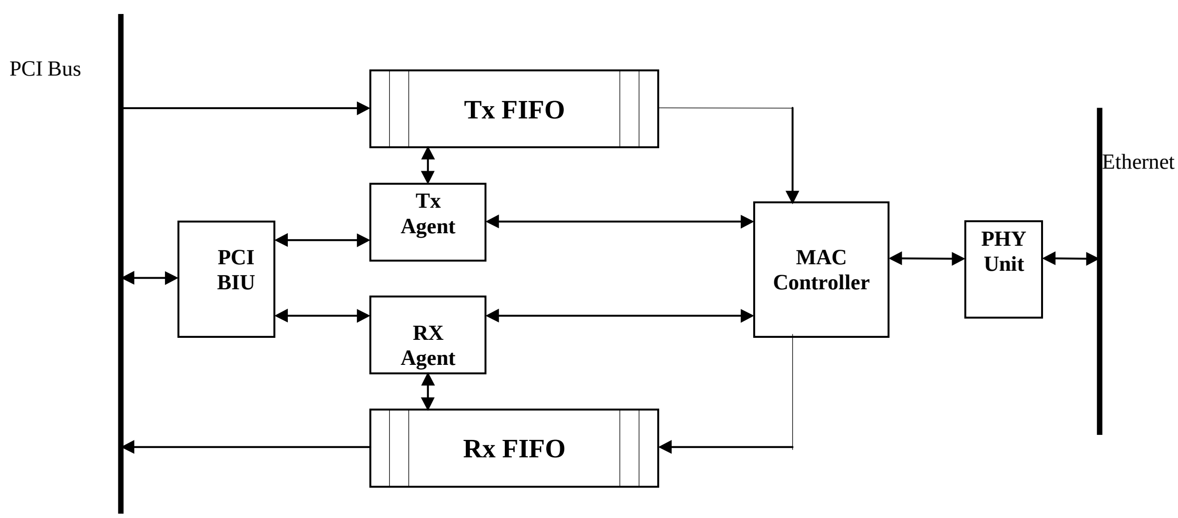
Logically, PNIC is the agent between the host and the Ethernet media. It sends out the information to the Ethernet network for the host and receives the information belongs to the host from the Ethernet network.

For transmission, the host prepares data in the transmit packet buffers and then writes appropriate commands to the descriptors to inform PNIC that there is data to be transmitted. PNIC reads the ready data from the packet buffer in the host memory and moves it to the on-chip Tx-FIFO. The MAC controller then pops out the data from the FIFO and transmits it onto the Ethernet network.

On the receiving side, PNIC looks up the destination address of every packet on the network. If the destination address matches one of the address in the address table or the packet is a broadcast packet, PNIC takes it and pushes it into the Rx-FIFO. Not only the perfect filtering is supported, group filtering is also provided to recognize other packets. Once the packet is received, the Rx-Agent then moves data from the Rx-FIFO to the Rx data buffer in the host memory based on the Rx descriptor specification of the receiving buffers.

In the following sections, diagrams and descriptions are illustrated to explain the operations in detail.

5.1 Block Diagram



5.2 Address Filtering

Three types of address filtering are supported by the PNIC:

- Receive if Match.
- Reject if Match..
- Receive if it is in the Hash table.

5.2.1 Filtering Table Setup

5.2.1.1 Descriptor setup

In the Transmit Descriptor, if bit27, SP, of TD1 is set, the packet is an address filtering setup packet. The filtering setup packet size has to be exactly 192 bytes, and it is not transmitted out to the Ethernet. It is used to setup the address filtering table on the chip. It is recommended that the transmit and the receive process are stopped before setting up the filtering table.

FT1 and FT0 of the TD1 specifies the type of filtering when the receive process is started. It is defined in the following table:

FT1	FT0	Lookup	Description
0	0	Physical Addr Match	Receive if the address match.
0	1	Physical Addr Match, if addr[47]=0; Hash Table lookup, if addr[47]=1.	Receive if Match or the address is in the Hash table.
1	0	Physical Addr Match	Reject if the address match.
1	1	Hash Table lookup	Receive if the address is in the hash table only.

5.2.1.2 Address Table setup

Two types of setup:

1. Ethernet Physical Address setup.
2. Hash Table setup.

- **Ethernet Physical Address setup.**

Max. of 16 Ethernet addresses can be setup in the filtering table. Whenever there is a new packet, the destination address will compare with every addresses in the filtering table. If it is one of the addresses in the table, address match is generated for the media agent to receive or reject the packet based on the filtering type defined in the TD1 of the filtering table setup packet.

When PNIC fetches the descriptor with TD1[27]=1, it reads the buffer and write the data to the table. It overwrites the 16 entries in the filtering table. The buffer size of the filtering table setup packet has to be exactly 192 bytes. They are mapped to the filtering table as defined in the following table.

addr offset	31 … 16	15 … 0
00H	Don’t care.	Ethernet Address 00 Byte[1:0]
04H		Ethernet Address 00 Byte[3:2]
08H		Ethernet Address 00 Byte[5:4]
0cH		Ethernet Address 01 Byte[1:0]
10H		Ethernet Address 01 Byte[3:2]
14H		Ethernet Address 01 Byte[5:4]
		⋮
a8H		Ethernet Address 14 Byte[1:0]
acH		Ethernet Address 14 Byte[3:2]
b0H		Ethernet Address 14 Byte[5:4]
b4H		Ethernet Address 15 Byte[1:0]
b8H		Ethernet Address 15 Byte[3:2]
bcH	Don’t care.	Ethernet Address 15 Byte[5:4]

- **Hash Table setup.**

In the Hash Table setup mode, a 512 bits hash table and a Ethernet Physical Address are setup.

addr offset	31 16	15 0
00H	Don't care.	Hash Table[15:00]
04H		Hash Table[31:16]
08H		Hash Table[47:16]
0cH		Hash Table[63:48]
10H		Hash Table[79:64]
14H		Hash Table[95:80]
		⋮
		Hash Table[495:480]
		Hash Table[511:496]
9cH		Ethernet Address Byte[3:2]
a0H		Ethernet Address Byte[3:2]
a4H		Ethernet Address Byte[3:2]
b8H		
bcH	Don't care.	

For each incoming packet, PNIC calculates the 32bit CRC of the destination address, takes the most significant 9 bits of the CRC value and inverts it to get the hash table index. If the indexed entry in the table is set, PNIC will receive the packet. Otherwise, PNIC rejects the packet. In the FT1,FT0=01 mode, if the received address is a physical address, PNIC will compare it with the only one entry in the Ethernet Physical Address table. Only the multicast address uses the hash table lookup. On the other hands, FT1,FT0=11 mode, both physical and multicast address use the hash table lookup.

6. Errors

PNIC may run into errors either when it tries to move data between host memory and the on-chip FIFO or when it contacts with media. When errors happen, proper procedure has to be executed in order to record the problem and restore the machine from errors.

6.1 Types of Error

Errors are summarized in the following tree structure.

PNIC Errors

- **Tx Errors**
  - **Local Errors:**
    1. PCI bus parity error.
    2. Tx FIFO underflow.
  - **Media Errors:**
    1. Link Fail
    2. Late collision
    3. No carrier.
    4. Lost of carrier.
    5. Transmit jabber time-out.
- **Rx Errors**
  - **Media Errors:**
    1. CRC error.
    2. Collision seen.
    3. Frame too long.
    4. Runt frame.
    5. Length error.
  - **Local Errors:**
    1. PCI bus parity error.
    2. Rx FIFO overflow.

6.2 Error Handling

When PNIC runs into error, PNIC first suspends the process and sends an interrupt to the host if the corresponding interrupt is enabled. If there is an outstanding opened descriptor, PNIC will immediately close the descriptor with the proper error information set in the descriptor. Similar action need to be performed to recover the on-chip FIFO. Flushing or purging the FIFO may be required to clean up the left over data in the FIFO. The host receives an interrupt and it will read the status register to identify the problem. After handling the errors, host may poll the agents to resume the process.

Basically, the action is summarized in the following list::

1. PNIC runs into an error.
2. If there is an outstanding descriptor, PNIC closes it with error information set.
3. If there is leftover data in the FIFO, PNIC purges the data.
4. PNIC updates the status register.
5. If the corresponding interrupt is enabled, PNIC asserts interrupt to the host.
6. PNIC suspends the process, and wait for the polling command or the wake-up activity.