PCI Bus Master Fast Ethernet LAN Controller

Winbond LAN
W89C840F
100/10Mbps Ethernet Controller

Publication Release Date:April 1997
Revision A1

The W89C840F is a highly integrated Ethernet LAN controller for both 100BaseT and 10BaseT Ethernet. It provides a host bus interface complying with the PCI local bus specification revision 2.1, and the MII interface complying with the IEEE802.3u standard for easily implementing an Ethernet LAN adapter. The built-in 2K bytes transmit FIFO and 4K bytes receive FIFO, controlled by the on-chip bus master, are designed for improving network performance and reducing the host bus utilitzation.

The on-chip DMA controller handles the data transfer between the host memory and the FIFOs. The data received from network are queued into the receive FIFO and then, directly moved into the host memory through the PCI bus. On the other hand, the transmitted data are fetched from the host memory and directly queued into the transmit FIFO. No extra on-board memory is needed for data buffering during the data transceiving operation.

Many versatile registers, inculuding host bus control registers, direct memory access(DMA) control registers, media access control registers, and signature identification registers, are implemented for system configuring. All of these long word accessible registers perform the status report and the precisely control on the transmit and receive operation. It also provides an extra channel for the on-line application program to update the on-board expansion ROM device in some specific application environment.

Features

- Complies with IEEE 802.3, 802.3u, ANSI 8802-3 and Ethernet standards
- Supports PCI bus master mode for DMA operation, fully complying with PCI 2.1 standard
- Early interrupt function available for both transmit and receive
- Both half duplex and full duplex available
- Independent deep receive and transmit FIFO and no onboard memory required
- Flexible data structure for host compatibility and system performance
- Supports 25 to 33 Mhz PCI clock speed
- Supports full MII management function
- Provides EEPROM and flash memory on-board programming function
- Supports both big and little endian byte ordering for descriptor and buffer
- Flexible address filtering modes
  -- 64-bit hash-table and one perfect address
  -- all multicast and promiscuous
- A boot ROM interface, capable of supporting up to 256KB
- Supports programmable sub-vendor ID with automatic loading into configuration register
- Internal and external loopback mode for diagnostic
- Single 5 volt power supply
- 100 pins PQFP package

Pin Assignment

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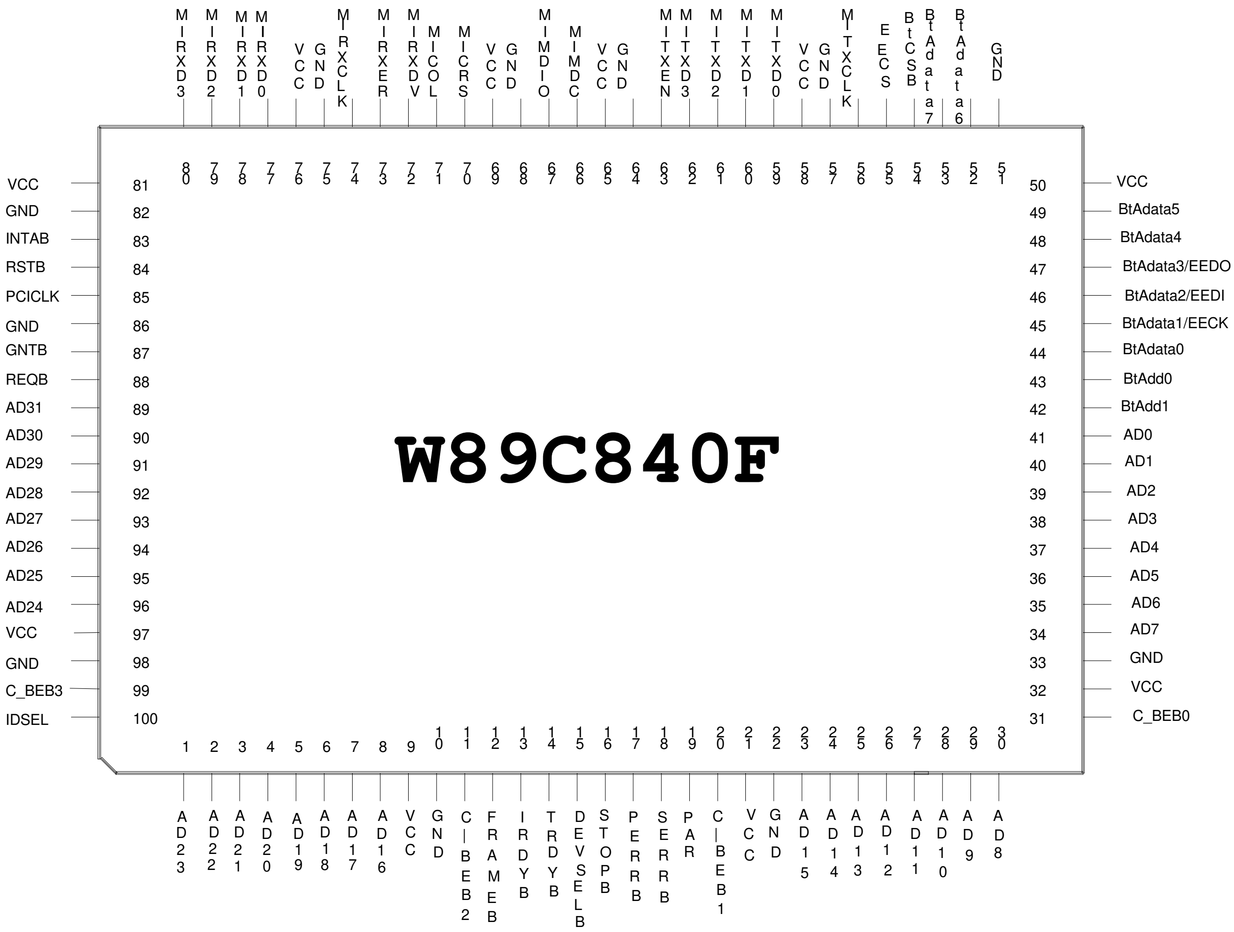


Fig 1: W89C840F pin configuration

Block Diagram

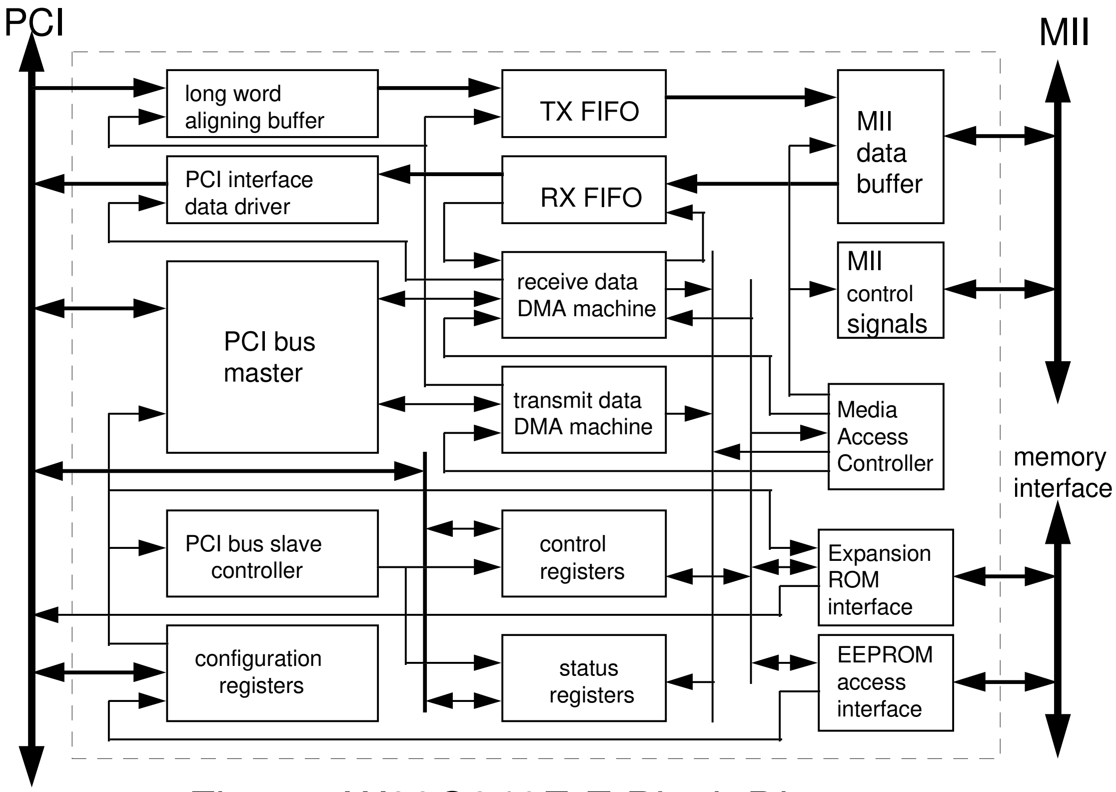
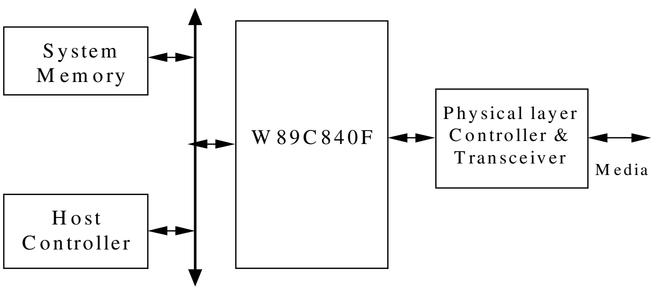


Fig. xx: W89C840F-E Block Diagram

System Diagram



W89C840F Typical Application
Fig. 3

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Pin Function Descriptions

1) PCI Interface

Signal Name	Pin Type	Pin Number	Pin Description
PCICLK	I		PCI Clock Input: The W89C840F supports PCI clock rate ranged from 25Mhz to 33MHz continuously. All PCI signals except RST# and INTA#, are referenced on the rising edge of this clock.
RSTB	I		Hardware reset signal: When asserted(active low), all PCI output of W89C840F will be in high impedance state, and all open drain signals will be floated. The configurations inside W89C840F will be in its initial state. This signal must be asserted for a period of, at least, 10 PCI clocks to have a reset on hardware correctly.
AD[31:0]	IO/TS		Multiplexed Address and Data bus: During the first cycle that FRAME# asserts, they act as an address bus; on the other cycles, they are switched to be a data bus.
C_BEB[3:0]	IO/TS		Multiplexed command and byte enables: These signals are driven by current bus master. During address phase, it means a bus command; on the other phase, it presents byte enable of the transaction.
PAR	IO/TS		Parity signal. This PAR represents even parity across AD[31:0] and C_BEB[3:0]. It has the same timing as AD[31:0] but delayed by one clock.
FRAMEB	IO/STS		PCI Cycle Frame: The current bus master asserts FRAMEB to indicate the beginning and duration of a bus access. This signal will keep asserted while the current transaction is ongoing and will keep deasserted to indicate that the next data phase is the final data phase.
IRDYB	IO/STS		Initiator Ready: The IRDYB asserted by the current initiator to indicate the ability to complete the data transfer at the current data phase. The initiator asserts IRDYB to indicate the valid write data, or to indicate it is ready to accept the read data. More than or exactly one wait state will be inserted if IRDYB deasserted during the current transaction. Data is transferred at the clock rising edge when both IRDYB and TRDYB are asserted at the same time.

TRDYB	IO/STS		Target Ready: Asserted by the current target to indicate ability to complete data transfer at the current data phase. When W89C840F is operating at the bus slave mode, it asserts TRDYB to indicate that the valid read data presents on the bus or to indicate it is ready to accept data. Wait states will be inserted if TRDYB deasserted. Data is transferred at the rising edge of the PCI clock when IRDYB and TRDYB are both asserted at the same time.
STOPB	IO/STS		PCI Stop: Asserted by the current target to request master to stop the current transaction.
IDSEL	I		PCI Initialization Device Select: Asserted by host to signal the configuration access request to W89C840F.
DEVSELB	IO/STS		PCI Device Select: Asserted by the current target to indicate that it has decoded its address as the current access target. When W89C840F is the current master, it checks if the target asserted this signal within 5 PCI clocks. If not, W89C840F will abort the access operation. When W89C840F is the target, it asserts DEVSELB in a medium speed, i.e., within 2 clocks.
REQB	O/TS		PCI Request: Asserted by W89C840F to request bus ownership. REQB will be tri-stated when RSTB asserted.
GNTB	I/TS		PCI Grant: Asserted by host to grant that W89C840F have got the bus ownership. When RSTB asserted, W89C840F will ignore GNTB.
PERRB	IO/STS		PCI Parity Error: Asserted by the current data receiptor. When W89C840F is the bus master, if a data parity error is detected and the parity error response bit (FCS<6>) is also set, it will set both bits of FCS<24> and C14<13> as 1 to terminate the current transaction after the current data phase is finished. When W89C840F is the target, a data parity error is detected and the bit FCS<6> is set, it will assert PERRB.

SERRB	O/OD		System Error: This pin will be asserted with one PCI clock width within two PCI clocks after an address parity error is detected and keep in high impedance state when idle. The interrupt function caused by this event is gated by the bits in FCS register. The W89C840F will assert SERRB and set a high to the Detect Parity Error bit FCS<31>, the Signal System Erro bit FCS<30> if an error, address parity error, is detected and SERRB enable bit FCS<8> is previously set to 1. The Bus Error Status bit C14<13> will be set to high if an address parity error is detected and the parity error response bit FCS<6> is set to high. To assert SERRB, when W89C840F detects an address parity error, the bit FCS<31> will be set to high. If the parity error response bit is set, the bit C14<13> will also be set. Under this case, if the SERRB enable bit FCS<8> is previously set too, W89C840F will assert SERRB and set the bit FCS<30> high. When W89C840F detects an address parity error, it will, within two PCI clocks after detecting, assert SERRB for one clock width and then tri-stated the signal.
INTAB	O/OD		Interrupt A: INTAB is asserted when any of the unmasked interrupt bits in C14/CISR are set. It will be kept asserted until all of the unmasked interrupt bits are cleared.

2) BootROM and EEPROM Interface

Signal Name	**Pin Type**	**Pin Number**	**Pin Description**
BtAdd0	I/O		BootROM address bit 0
BtAdd1	I/O		BootROM address bit 1
BtAdata[7:4]	I/O		BootROM address and data bus: bit7 - bit4.
BtAdata[3]/EEDO	I/O		EEPROM data output; BootROM address &data:bit3
BtAdata[2]/EEDI	I/O		EEPROM data input; BootROM address & data:bit2.
BtAdata[1]/EECK	I/O		EEPROM data clock; BootROM address & data:bit1.
BtAdata[0]	I/O		BootROM address & data:bit0
BtCSB	I/O		BootROM chip select
EECS	I/O		EEPROM chip select

3) MII Interface

Signal Name	**Pin Type**	**Pin Number**	**Pin Description**

MTXCLK	I		Transmit clock: MTXCLK is a continuous uniformed clock source driven by the external PHY. It provides the timing reference for the signals MTXEN and MTXD. MTXCLK should be either 25MHz or 2.5MHz clock.
MTXD[3:0]	O		Transmit Data: This nibble byte width transmit data bus is synchronized with MTXCLK. It should be latched by the external PHY at the rising edge of MTXCLK. MTXD[0] is the least significant bit.
MTXEN	O		Transmit enable: It indicates that transmits activity to an external PHY. It will be synchronized with MTXCLK.
MMDC	O		MII management reference clock. It is the reference clock of MMDIO. Each data bit will be latched at the MMDC rising edge.
MMDIO	I/O		MII management data input/output. This pin is used to transfer the MII control and status information between PHY and MAC.
MCRS	I		Carrier Sense Signal: This shall be asserted by PHY device when media is busy, and deasserted when media is idle. MCRS shall keep asserted, even at the duration of a collision.
MCOL	I		Collision detected: This shall be asserted by the PHY device upon detecting a collision happened over the medium. It will be asserted and lasted until collision condition wholly vanishes.
MRXDV	I		Received data valid: This pin is driven by PHY device. It will be asserted when received data is coming and present, and deasserted at the end of the frame. MRXDV is synchronized with MRXCLK from PHY device.
MRXER	I		Received data error: This pin is driven by PHY device. It indicates a data conversion error is detected by PHY device. The assertion of MRXER should be lasted for longer than a period of MRXCLK. When MRXER asserted, W89C840F will report a Receive Error detection and a CRC error.

MRXCLK	I		Received clock source: This clock is from PHY device. It will be either 25Mhz or 2.5Mhz receive clock, determined by auto-negotiation device in PHY and supported by W89C840F. The minimun duty cycle at its high state or low state of MRXCLK should be 35% of the nominal period under all condition. PHY device should drive MRXCLK as a continuous clock.
MRXD[3:0]	I		Received data pins: This is driven by external 100/10 Mbps PHY. MRXD should be syncronized with clock source MRXCLK and valid only when MRXDV is valid. MRXD[0] is the least significant bit.

$. Functional Description

Receive direct memory access function

On receiving a data packet, the receive DMA function will transfer these data from the internal receive FIFO which has a size of 4k bytes to the host memory with the assistance of the on-chip PCI bus master. During the transaction cycle, the media access controller(MAC) requests the receive DMA state machine to move the data in the receive FIFO onto the PCI bus, and then move it to the host memory with a kind of data structure which is constructed and described by descriptors.

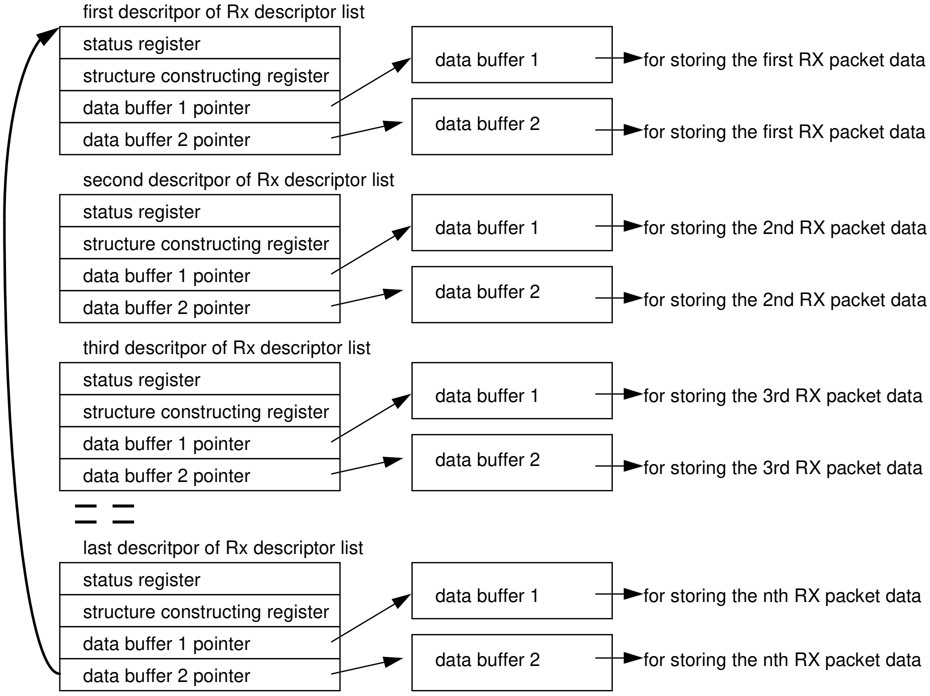
A number of receive descriptors in the chip, which generated by chip itself, are used to specify the descriptor structure and indicate the memory spaces for storing the received packet data. The receive descriptors are also used to store the received packet status when a valid packet is received. Each descriptor has a size of 4 long words that resides in the host memory. The first 32 bits are used to keep the received packet status information. The second 32 bits are used to specify the descriptor structure type and the size of the received data buffer. The remains 64 bits are used to specify the size and the address of the allocated memory for this data buffer and the next one.

The received packet can be described by a single descriptor or multiple descriptors. It depends on the configuration, previously set by software driver, and the received packet length. The received packet data also can be stored in a single data buffer or multiple data buffers.

The descriptor structure can be either a ring structure or a chain structure. A mixed structure mode is also allowed, too.

In the descriptors with the ring structure, Host allocates a big continuous memory for keeping all the descriptor information. Each descriptor can point to two data buffer addresses to store the received packet data. Though the data buffers are not necessarily be contiguous, the descriptors must be contiguous one after the other.

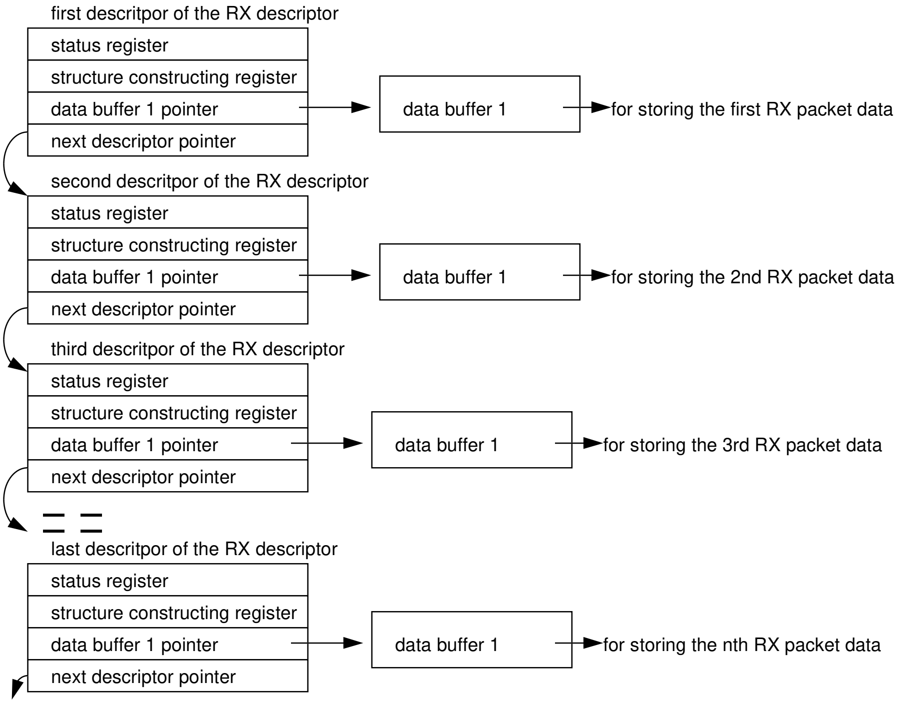
The following figures describe the ring structures of receive descriptor.



The software driver can request more than one descriptors and data buffers at a time. As described in the above diagram, the total descriptors are constructed as a ring. A packet can be stored in more than one data buffers. In that case, the data buffer 1 is stored first and then data buffer 2. If a packet contains more data than the two data buffer can accommodate, it fetches the next descriptor and two new data buffers to save the extra more data. That is a packet can be stored in more than one descriptors. In the contrary, a descriptor is not allowed to hold more than one packet. If the data buffer 1 can completely store the received packet, the data buffer 2 will be left empty and the next packet will be firstly stored at the data buffer 1 in the next descriptor. The diagram shown above is just one case of the buffer application. When the last descriptor is used by a received packet, the next descriptor should be the first descriptor of the ring. Once the descriptors are processed by the driver, it can be released to the ring for later use. In the ring structure, the start address of the next descriptor is specified by the skip length, bit2 to bit6 of C00/CBCR register, and the start address of the first descriptor is specified by the C0C/CRDLA register.

. For the descriptors with the chain structure, host is allowed to allocate scatterly a block of memory with the size of 4 long words, linked by the pointer which located at the 'next descriptor pointer' field. Each descriptor has only one link to a data buffer to store the received packet data. The descriptors are located randomly and linked by the second pointer in each descriptor, which points to the start address of the next descriptor.

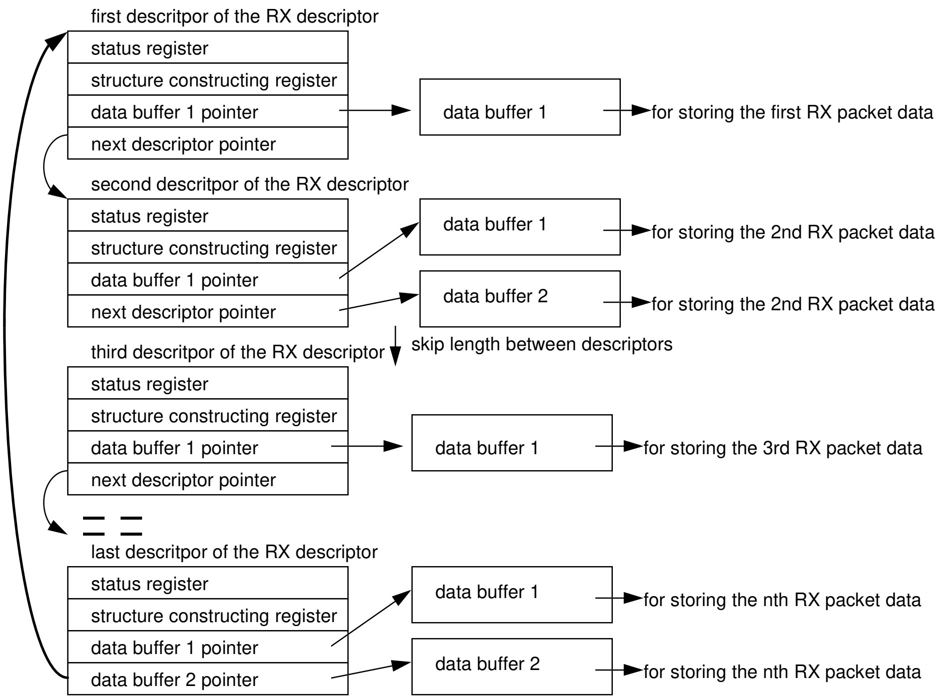
The following figures describe the chain structures of receive descriptor.



As shown in the above diagram, all descriptors are linked by pointers to construct a chain. The data can be stored in more than one data buffers. In the last descriptor of the descriptor chain, the content of the R03 register will be ignored by the receive DMA state machine if the RLINK bit of the R01 register in the last descriptor is set to high. When the last descriptor has already been used, the next descriptor pointer in this one will link to the start address of the first descriptor in the chain if it is available.

In the chain structure, the base address of the first descriptors is specified by the C0C/CRDLA register, the receiving descriptors list address register and the base address of the next descriptor is pointed by the R03 of the current descriptor.

The following figure describes the mixed mode list, composed of both the ring and the chain structures at the same time.

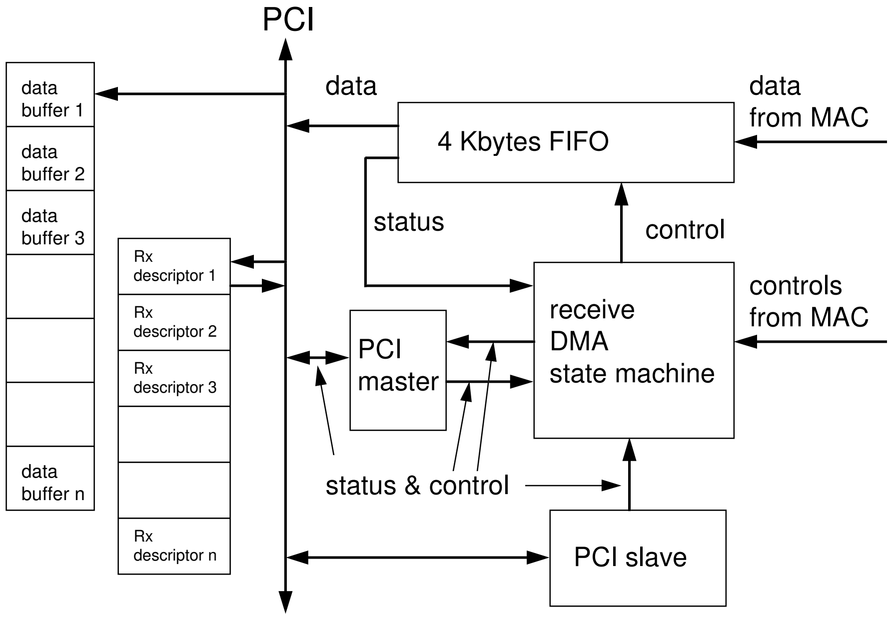


As shown by the above diagram, the descriptors construct a mixed structure. Each descriptor with the chain structure can link to only one data buffer and the last 32 bits are treated as the next descriptor pointer. When the RLINK bit of the current descriptor, other than the last descriptor in the descriptor list, is reset to low and this descriptor is programmed to be a ring structure, the current descriptor can point to two data buffers and the skip length between descriptor is used to point to the next descriptor starting address.

In the last descriptor in the descriptor list, the R03 register will be used to designate the base address of the data buffer 2 while the RLINK bit of the last descriptor is reset to low, but will be ignored if the RLINK bit of the last descriptor is set to high. That is, if the last descriptor is a ring structure, it acts as a ring and vice versa.

The next descriptor field of the last descriptor will be the starting address of the first descriptor, no matter what the value of the RLINK bit of the last descriptor is low or high.

The data flow of a packet in the receiving path is shown as the following diagram.



As shown the above diagram, the receiving DMA state machine controls the data receiving processing and the receiving status monitoring. On receiving the data packets, the receiving DMA will start to move these data from FIFO to the data buffer, pointed by descriptors in the host memory if there is an available data buffer and the byte count of the data received into the FIFO is larger than or equals to 64 bytes. If the received packet length is less than 64 bytes and runt packet is not accepted, the receiving DMA will discard this invalid packet and give it a record in the status register. The receiving DMA will start to move the data in FIFO after the full packet is received if runt packet is accepted. Once a valid packet is received, the receive DMA will advance the descriptor pointer for the next incoming packet. However, the current data buffer and the descriptor will be re-used if the current receiving packet is not a valid packet, i.e. the receive state machine will ignore the previously received packet data in the data buffer. Each received packet will be treated as a valid packet if it meets the requirement in the bits 3, 4, 5, 6 and 7 of C18/CNCR register. In some case of the data buffer unavailable temporarily, the incoming packet data from media will be queued in the FIFO temporarily, meanwhile, the receive DMA will enter suspend state at this time and a buffer unavailable interrupt will be issued. The receive DMA will start moving the data whenever the data buffer is available and a receiving operation is demanded, On the other hand, the data will be lost if the FIFO is overflowed. The receiving status, e.g., the receive descriptor access status, the receive completion status, the received data byte count, the received packet error status, the received packet data type, ... and so on., will be written back into the descriptor by the receive DMA when the packet is received successfully.

During receiving a packet, the receive DMA will release the access right of the descriptor and the data buffer to the driver immediately after the free byte space of the data buffers pointed by the current descriptor is counted down to zero and the receive DMA will fetch the next available descriptor for the current incoming packet. It is known that the LLC layer data is packed into the first 64 bytes of the packet in most application program. The driver and the upper layer application program can read the protocol messages carried in the first 64 bytes of the incoming packet when the receive DMA release the descriptor and the data buffer for the current incoming packet, although the current incoming packet is not yet received completely. The function of the receive DMA releasing the descriptor and the data buffer which have been used during receiving a packet allows the software and the hardware to process the receiving packet concurrently. This parallel processing of software and the hardware can improve the system receiving performance significantly.

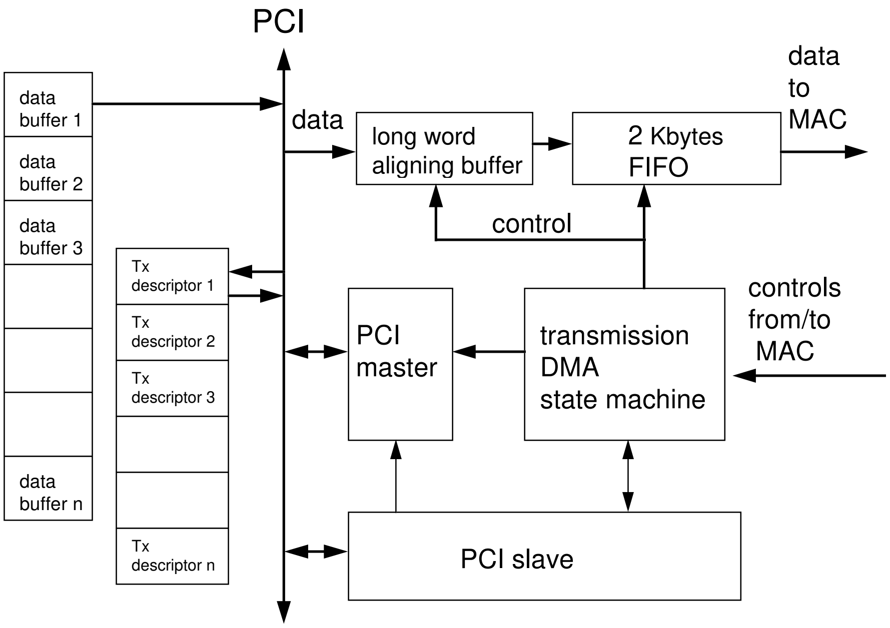
When the incoming packet is received completely, the receive DMA will write the same copy of the packet receiving status to the first descriptor and the last descriptor of the current frame respectively. The receiving status includes the receive completion status, the received byte count, the receive error type,...etc. All of the status is specified in the receive descriptor R00. When the software and hardware are concurrently processing , the software needs not to go back to read the first descriptor of the current incoming packet for knowing the receive completed status or other receiving status when it is processing the last descriptor and the data buffer of the current incoming packet. But, if there is only one descriptor needed for the current incoming packet, all of receiving status will be updated in the unique descriptor.

The W89C840F transmit DMA function performs the data transfer from the host memory through on-chip PCI bus master into the internal 2 Kbytes transmit FIFO. The transmit DMA state machine will request the MAC to send out the data in the FIFO onto the MII.

The transmit descriptor is used to set the transmit configuration and to point to the transmit data buffer locations. Each packet to be transmitted can be described by one or more than one descriptor. And each descriptor consists of four consecutive long word. The first long word(T00) is for the transmit frame status register. The T00 describes the descriptor access right control, the packet transmitting status,...etc. The second long word(T01) is for the control register used to specify the transmission configuration, including the CRC inhibit control, padding function control, the descriptor structure control ... etc. The third long word (T02) is for the first data buffer pointer and the fourth long word is used as the second data buffer pointer in the ring structure.

The transmit descriptor list also can be constructed as a ring structure or a chain structure. The mixed chain and ring structure is also allowed to be constructed. The scheme for constructing the transmit descriptor list is same as the one for receiving descriptor list, but, each transmit data buffer size is limited to under 1 Kbytes other than the 2 Kbytes receiving data buffer. In the consequence of the 1 Kbytes transmit data buffer, each descriptor can point to a maximum two 1 Kbytes data buffer totally.

The data flow of the packet transmission is shown as the following diagram



The data to be transmitted is stored in the transmit data buffer in the host memory. The transmission DMA state machine will fetch the data in the host memory into the transmit FIFO. when the transmission DMA is started up. All of the data fetched from the data buffer will be long word aligned before being queued into the transmission FIFO. The driver program can inform the transmit DMA the location of the data to be transmitted in the host memory and then the transmit DMA will fetch the data from that location directly. Because the address of the data may not long word aligned, so that the transmit DMA need to align the data for passing the data to the MAC in a long word aligned format. The aligned long word data, and then, is queued into the transmit FIFO. The transmission DMA will not request the MAC to fetch the data in the FIFO for transmitting until the byte count of the data in the FIFO is reach the threshold defined by C18/CNCR bit 14~20.

The transmission DMA is implemented a pre-fetch function for speeding the transmit performance. With this implementation, the transmit DMA will pre-fetch the next packet data in the host memory after the current packet data is moved into the transmit FIFO completely. Before starting to fetch the next packet data, the transmit DMA will assert an interrupt if the transmit early interrupt is enabled. If there is no more packet to be transmitted, the transmit DMA will report a buffer unavailable status and assert an interrupt if the transmit buffer unavailable interrupt is enabled. After all of the current packet data in the transmit FIFO are transferred out by the MAC block, the transmit DMA will try to fetch the next packet data again automatically if the transmit DMA is not fetching the data from the host memory. A packet transmit interrupt will be asserted when the current packet is transmitted if the packet transmitted interrupt is enabled.

The transmit DMA will write back the current packet transmit status into the first descriptor of the current transmit packet when the packet is successfully transmitted or is aborted due to excessive collision.

For consecutively transmitting multiple packets, the software driver can previously program all the packet data in the host memory and then release the access right to the W89C840F. Once the transmit DMA is turned on, the DMA will transmit all of the packet out automatically. The inter-frame gap between these packets will be specified by the MAC block for complying with the IEEE802.3u specification.

For concurrently processing the packets transmitting, the transmission DMA asserts the transmit early interrupt to trigger the software driver to set up the next transmitting packet data more earlier. The data transmission rate on the MII bus can be either 10 Mbps or 100 Mbps which is quite lower than the rate on PCI bus. Mostly, the packet data is not yet completely transmitted onto the MII bus even though the packet data with only a few bytes have been all moved into the transmit FIFO, the transmission DMA still does not issue an interrupt to host. This will drop the transmit performance if the software driver waits for the current packet being transmitted onto the MII completely and then set up the next packet data. The transmit early interrupt can avoid the time consumption when waiting for the transmit completion of the current packet occurs.

Media Access Control function(MAC)

The function of W89C840F MAC fully meets the requirements, defined by the IEEE802.3u specification. The following paragraphs will describe the frame structure and the operation of the transmission and receive.

The transmission data frame sent from the transmit DMA will be encapsulated by the MAC before transmitting onto the MII bus. The sent data will be assembled with the preamble, the start frame delimiter(SFD), the frame check sequence and the padding for enforcing those less than 64 bytes to meet the minimum size frame and CRC sequence.

The out going frame format will be as following

10101010- - - - 10101010	1010111	d0	d1	d2	--	dn	padding	CRC31	CRC30	---	CRC0

As mentioned by the above format, the preamble is a consecutive 7-byte long with the pattern 10101010″ and the SFD is a one byte 10101011 data. The padding data will be all 0 value if the sent data frame is less than 64 bytes. The padding disable function specified in the bit23 of the transmit descriptor T01 is used to control if the MAC needs to pad data at the end of frame data or not when the transmitted data frame is less than 64 bytes. The padding data will not be appended if the padding disable bit is set to high. The bits CRC0 ... CRC31 are the 32 bits cyclic redundancy check(CRC) sequence. The CRC encoding is defined by the following polynomial specified by the IEEE802.3.

$$G(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^{8} + x^{7} + x^{5} + x^{4} + x^{2} + x^{1}$$

This 32 bits CRC appending function will be disabled if the Inhibit CRC of the transmission descriptor T01 is set to high.

The MAC also performs many other transmission functions specified by the IEEE802.3, including the inter-frame spacing function, collision detection, collision enforcement, collision backoff and retransmission. The collision backoff timer is a function of the integer slot time, 512 bit times. The number of slot times to delay between the current transmission attempt to the next attempt is determined by a uniformly distributed random integer algorithm specified by the IEEE802.3. The integer, r, is specified as the following

$$0 \leq r \leq 2^{k} \qquad \text{where } k = \min(n, 10)$$

The MAC performs the receive functions specified by the IEEE802.3 including the address recognition function, the frame check sequence validation, the frame disassembly, framing and collision filtering.

The W89C840F categorizes the input stream from media into three types of frame. These three types are the packet with unicast destination address, the multicast destination address and the broadcast destination address. A unicast address is defined as a destination address with its first bit(the LSB) low. A multicast address is defined as a destination address with its first bit(the LSB) high but the other 47 bits are not all one. A broadcast address is defined as a destination address with its all 48 bits are one. All the three types of the packet reception is selectively determined by the configuration of the bit 3, 4 and 5 of the C18/CNCR register of the W89C840F.

The C40/CPA0 and C44/CPA1 are used to store your own 48 bits Ethernet ID. of the network node before starting to receive a packet. Its contents comes from EEPROM after power-on reset.

The mapping relationship between the 48 bits ID and the C40/CPA0 and C44/CPA1 is as following table.

	Bit 31~ 24	Bit 23 ~ 16	Bit 15 ~ 8	Bit 7 ~ 0
C40/CPA0	32th ~ 25th	24th ~ 17th	16th ~ 9th	8th ~ 1st
C44/CPA1	reserved	reserved	48th ~ 41th	40th ~ 33th

The incoming packet with unicast address will be accepted if the bit 3 of C18/CNCR is reset to low and the destination address of the incoming unicast packet has to match with the content of C40/CPA0 and C44/CPA1 setting.

All of the incoming packet with unicast address will be accepted if the bit 3 of C18/CNCR is set to high.

In broadcast case, to accept a packet with a broadcast destination address, the bit 5 of C18/CNCR must be set to high. Otherwise, the W89C840F will reject this broadcast packet.

In multicast case, a packet with a multicast destination address will be accepted if the destination address is grouped into the selected group specified by the registers of C38/CMA0 and C3C/CMA1. These two registers are used to store the group mapping for the multicast packet.

The following table shows the group mapping relationship between the groups and the contents of C38/CMA0 and C3C/CMA1. It is obviously shown that each bit in the registers C38/CMA0 and C3C/CMA1 represents one group.

	Bit 31~ 24	Bit 23 ~ 16	Bit 15 ~ 8	Bit 7 ~ 0
C38/CMA0	Group 32 ~ 25	Group 24 ~ 17	Group 16 ~ 9	Group 8 ~ 1
C3C/CMA1	Group 64 ~ 57	Group 56 ~ 49	Group 48 ~ 40	Group 39 ~ 33

All the 48 bits destination address(including physical address, multicast address and broadcast address) of the incoming packet will be fed into the CRC generating mechanism. The six most significant bits of the CRC(CRC31, CRC30, ... CRC26) will determine which group the incoming packet belongs to. The relationship between these six bits of CRC content and the group which the multicast address belongs to is shown as the following table.

CRC 31,30,29	CRC28,27,26							
	111	110	101	100	011	010	001	000
000	grp 8	grp 7	grp 6	grp 5	grp 4	grp 3	grp 2	grp 1
001	grp 16	grp 15	grp 14	grp 13	grp 12	grp 11	grp 10	grp 9
010	grp 24	grp 23	grp 22	grp 21	grp 20	grp 19	grp 18	grp 17
011	grp 32	grp 31	grp 30	grp 29	grp 28	grp 27	grp 26	grp 25
100	grp 40	grp 39	grp 38	grp 37	grp 36	grp 35	grp 34	grp 33
101	grp 48	grp 47	grp 46	grp 45	grp 44	grp 43	grp 42	grp 41
110	grp 56	grp 55	grp 54	grp 53	grp 52	grp 51	grp 50	grp 49
111	grp 64	grp 63	grp 62	grp 61	grp 60	grp 59	grp 58	grp 57

A packet with multicast address which belongs to the nth group will be accepted if the relative bit of the nth group in C38/CMA0 and C3C/CMA1 is set to high and the bit 4 of C18/CNCR is also set to high.

Besides the address recognition function, the MAC also performs the frame check sequence validation function. Each incoming packet data, including the destination address, source address, the packet data and the 4 bytes CRC data will be fed into the MAC′s CRC generating logic to generate a 4 bytes CRC sequence. The MAC will compare this new CRC data with the one, included in the incoming packet. It will be recognized as an error packet if these two 4-byte CRC data is not the same. But the bit 7 of C18/CNCR will determine if the MAC accepts the error packet or not. A high value of this bit will force MAC to accept the error packet, and low to reject. An incoming packet without byte alignment will be treated as an error packet. Some packets with the length less than 64 bytes caused by the collision event on the network are also treated as an error packet. The terminology for the packet with the length less than 64 bytes is called as runt packet. The extra control bit for accepting the runt packet is defined as the bit 6 of C18/CNCR. To accept a runt packet, both of the bit 6 and bit 7 of C18/CNCR should be set to high.

The MAC will, finally, do the framing function to strip the preamble and the SFD before sending the receive data to the receive DMA machine. The data sent to the receive DMA state machine includes the LLC data and the 4 bytes CRC.

Loopback diagnostics function

The loopback mode defined for W89C840F is used for diagnostic. The transmit out data will appear on the MII interface and will then be fed back into the internal receive channel of the MAC block and then be moved back into the host memory by the receive DMA state machine. In loopback mode, the transmission function will work normally as it is in normal mode, but, only the data is processed by the MAC. The COL, CRS will be ignored in loopback mode.

To program the W89C840F into loopback mode, the Loopback Mode of C18/CNCR should be set to 01H.

Full duplex and half duplex function

The transmit DMA and the receive DMA are independently operating no matter what the W89C840F is set in full duplex mode or in half duplex mode. However, in MAC side, the operations are different and depends on the full duplex or half duplex mode is selected.

In the half duplex mode, the MAC should perform the transmission or reception operation at the different time frame. Simultaneous transmission and reception operation are not allowed. Once the half duplex mode is selected, the MII input signals, COL and CRS , will be valid inputs for the W89C840F. During the time the MAC is transmitting a packet, an active signal COL on MII bus will be judged to be a transmit collision event, occurred on the media. However, in the time duration from 10 bits time to 16 bits time after the packet is transmitted, the active COL signal is recognized as a SQE test signal but not a collision event. The active signal CRS will be recognized as a loopback carrier sense signal when the MAC is transmitting a packet. The carrier sense lost status is relied on the CRS. Normally, there should not be any carrier sense lost during transmitting if the media and devices are functional.

In the full duplex mode, the MAC can perform the transmission and receive operation at the same time. In this case, the COL and CRS signal on MII will be ignored. There are no collision event, SQE lost and carrier sense lost defined in the full duplex mode. Any activity on COL and CRS will not affect the operation inside the MAC.

To select the full duplex mode or the half duplex mode, you have to set the full duplex control bit of C18/CNCR.

Network media speed selection function

The W89C840F is specifically designed for both 100BASE-T and 10BASE-T Ethernet. The transmission rate is based on the clock speed of the MII input signals TXCLK and RXCLK. The MAC will transmit the data based on the clock rate of TXCLK, and receive the MII input data based on the clock rate of RXCLK.

In 100BASE mode, the TXCLK and RXCLK will be at 25MHz, however, in 10BASE mode, the TXCLK and RXCLK will be at 2.5 MHz. The clock rate of the RXCLK and the TXCLK is dependent and determined by the external physical layer device(PHY) which supports 10/100M bit rate.

The Fast_Ethernet_Select in C18/CNCR register is used to select the mode in which the W89C840F is working in 10M or 100Mbps. In 100Mbps (100BASE) mode, the MAC will not check the

SQE status when transmitting a packet. In 10Mbps(10BASE) mode, the SQE signal will be checked by MAC. No further function is controlled by the Fast_Ethernet_Select of C18/CNCR register.

Device identifying function

This function is to utilize the device configuration data stored in the device configuration registers, in which some of them loaded from the external EEPROM. You can tell the vendor, device type, revision, signature and your own defined code through reading the contents of these registers.

The F00/FID is a read-only register which contains the vendor ID. and device ID., used for identification. Its ' contents is loaded from the external EEPROM when hardware reset only.

The second read only register F08/FREV used for identification. It contains the revision ID. which is also loaded from EEPROM only. The Ethernet device identification code is also included in F08/FREV, but it is a built in code, not loaded form EEPROM.

The another identification register is the F40/FSR, a read only, too. The signature code for Winbond W89C840F is built in the F40/FSR signature register. The 12Hth and 9aHth bytes will be read out recursively when a number of consecutive PCI configuration space read operation is accessed to the F40/FSR. The first, third, fifth,...etc. odd read operation will get 12H, however, the second, fourth, sixth,...etc. even read operation will get 9aH.

For some special requirement, the field of driver area of F40/FSR can be used as a word-width data buffer for latching the user defined identification code.

EEPROM hardware reset auto load and software programming function

The following configuration parameters should be stored in a EEPROM device for configuring the W89C840F and can be loaded into the corresponding configuration register while power-on reset occurring.

1) the 6 bytes Ethernet ID.
2) the 2 bytes subsystem ID.
3) the 2 bytes subsystem vendor ID.
4) the 2 bytes device ID.
5) the 2 bytes vendor ID.
6) the 1 bytes revision ID.
7) the 1 byte booting device size
8) the 1 byte maximum latency
9) the 1 byte minimum grant

The data mapping and its offset address for all of the above parameters is as the following table.

Address	High Byte (BIT 15 ~ BIT 8)	Low Byte (BIT 7 ~ BIT 0)
09H~3FH	reserved	reserved
08H	C48	Revision ID
07H	Vendor ID(high byte)	Vendor ID(low byte)
06H	Device ID(high byte)	Device ID(low byte)
05H	Subsystem Vendor ID(high byte)	Subsystem Vendor ID(low byte)
04H	Subsystem ID(high byte)	Subsystem ID(Low byte)
03H	MAXLAT	MINGNT
02H	Ethernet Address 5	Ethernet Address 4
01H	Ethernet Address 3	Ethernet Address 2
00H	Ethernet Address 1	Ethernet Address 0

The W89C840F will generate a nine-word reading command to the EEPROM to read the configuration data and store these data into the configuration registers and the control register of the W89C840F after hardware reset. The serial EEPROM 93C06 or 93C46 will be the choice as the storage device for storing these configuration data.

Other than the reading after hardware reset, the EEPROM can be read by the application program. The C24/CMIIR register provides an alternative path to access the data in EEPROM. The bits 0, 1, 2, ... and 7 of CMIIR are general I/O port. When the bit 11 of CMIIR is set to high, the bits 0, 1 and 2 will be put on the EECS, BtAdata1/EECK, and BtAdata2/EEDI, respectively , to trigger EEPROM. The data from EEPROM running over the pin BtAdata3/EEDO will be hold and latched by the bit 3 of CMIIR, and be read by W89C840F. The application program can program bits 0, 1 and 2 of CMIIR to generate the chip select signal, clock and read command, based on the AC timing spec. of the EEPROM device, to EEPROM, and running over the pins EECS, BtAdata1/EECK, and BtAdata2/EEDI respectively. For reading the output data from EEPROM, the application program should make the necessary level transition as a clock on BtAdata1/EECK. One falling edge will trigger the EEPROM device to drive the next bit of output data relative to the input command.

The EEPROM can be programmed through the general I/O port of the W89C840F. The application program can write data into the EEPROM through programming the bits 0, 1 and 2 of the register CMIIR. In the write cycle of the EEPROM device, the data on BtAdata3/EEDO is meaningless.

BOOT ROM system read and software programming function

The W89C840F can address up to 256 Kbytes memory space for the on-board boot ROM device. The on-board boot ROM device will be mapped into the host memory by the system BIOS (Basic Input/Output System). After power-on reset, The BIOS will write a set of value with all 1 to the F30/FERBA configuration register and then read the value back. The W89C840F will return the all 1 value, except some bits with 0, depending on the configuration of C48/CBRCR. The relationship between the return value from the register F30/FERBA and the setting to the register C48/CBRCR is described as the following table.

ROM size	C48/CBRCR configuration	F30/FERBA return value

No boot ROM	00000000H	00000000H
No boot ROM	00000001H	00000000H
8 Kbytes ROM	00000002H	FFFFE001H
16 Kbytes ROM	00000003H	FFFFC001H
32 Kbytes ROM	00000004H	FFFF8001H
64 Kbytes ROM	00000005H	FFFF0001H
128 Kbytes ROM	00000006H	FFFE0001H
256 Kbytes ROM	00000007H	FFFC0001H

According to the return value from the register F30/FERBA, The system BIOS can determine how large the memory space is required and then write the memory space base address back to the register F30/FERBA. In the cases of no boot ROM, the system BIOS will write back all 0 back into F30/FERBA.

The address decoder of W89C840F for accessing the on-board ROM memory will be enabled if both the bit 0 of F30/FERBA and the bit 1 of F04/FCS are set to high at the same time. the on-board boot ROM data will be fetched by W89C840F and loaded into the host memory. On the other hand , the address decoder will be disabled if the bit 0 of F30/FERBA is reset to 0. Under this case, W89C840F will ignore the C48/CBRCR, no matter what content it has.

Usually, the on-board boot ROM data can be read by the system BIOS during host system booting or power-on reset, the W89C840F also provides another access way for the application program to do some unusual applications, like down loading the ROM code or re-programming the ROM code on line.

The procedures for on-line reading the on-board ROM device are described as following.

1) write the offset address into the C28/CBROA.

2) reset the bit 11 of C24/CMIIR to 0.

3) set the bit 14 of C24/CMIIR to 1.

4) read back the data form C24/CMIIR

The procedures for on-line writing the on-board ROM device are described as following

1) write the offset address into the C28/CBROA.

2) reset the bit 11 of C24/CMIIR to 0.

3) write the one byte data into C24/CMIIR bit 0 to bit 7.

4) set the bit 13 of C24/CMIIR to 1.

The bit 13 and bit 14 of the register C24/CMIIR should not be set to 1 at the same time. In the case of both of the bit 13 and bit 14 are 1, it will not properly initialize the read or the write operation for ROM device. The application program can check the contents of the register C24/CMIIR to know if the read or write operation is already completed or not. The W89C840F will start the read or the write operation when the bit 14 or bit 13 are set to high and will reset the bit 14 or bit 13 to 0 automatically after the read/write operation is completed. For the writing operation, the software driver should not start up the next write data request until the bit 13 of C24/CMIIR is reset to 0 by the W89C840F. For the read operation, the read data will be valid only if the bit 14 of the register C24/CMIIR is reset to 0 by the W89C840F.

The operation of reading or writing for the on-board ROM device through the registers C24/CMIIR and C28/CBROA will not affect the memory space configuration of the host system because either read or write operation is performed through the PCI I/O access command.

MII management function

The MII management function provided by W89C840F can be used to access the registers of the external physical layer device. The bits 16, 17, 18 and 19 of C24/CMIIR are designed for MII management . When the bit 18 is reset to low, the MDIO signal on MII bus is an input of W89C840F. The data on the MDIO will be reflected transparently on the bit 19 of the register C24/CMIIR. No data latching function for this input data. While the bit 18 is set to high, the MDIO signal on MII will be changed to be an output pin of W89C840F and the data written to the bit 17 of the register C24/CMIIR will be driven onto the MDIO. To generate the necessary clock for MII management, the application program can write 1 and 0 alternately to the bit 16 of the register C24/CMIIR. The clock is used by the external physical layer device to clock in the written data or to clock out the read data.

System resource configuring function

The W89C840F will require the I/O space, memory space and the interrupt line to perform the communication between the network and the host.

The system BIOS can write all 1 data into the register F10/FBIOA and read back its value to determine how large the I/O space the W89C840F requires. The W89C840F will return a FFFFF801H value if the system BIOS has previously written all 1 value into the F10/FBIOA. This means that the W89C840F requires 128 bytes system I/O space. The I/O space allocated for the W89C840F is relied on which I/O address base is written into F10/FBIOA. The W89C840F will decode the address message based on the content of the register F10/FBIOA to determine if the current PCI transaction is accessed to its registers.

For memory space allocation, the system BIOS can write all 1 value into the register F14/FBMA of the W89C840F and read back its value to determine how large memory space the W89C840F requires. The W89C840F will also return FFFFF801H value if the system BIOS has previously written all 1 value into the register F14/FBMA. This means that the W89C840F requires 128 bytes system memory space. The memory space allocated for the W89C840F depends on which memory address base is written into the register F14/FBMA. The W89C840F will decode the address message based on the content of the register F14/FBMA to determine if the current PCI transaction is accessed to its registers.

The W89C840F uses only one interrupt pin, INTA#. However, the interrupt line resource assignment is determined by the system BIOS by writing the related data into the bits 0 to 7 of the register F3C/FIR in the W89C840F. The data written into the bits0 to 7 of the register F3C/FIR can be used by the driver program to decide the interrupt service subroutine configuring.

PCI Configuration register

The general attributes of the PCI configuration registers implemented in the W89C840F are described as the following:

1) Writes to the reserved configuration registers are treated as no-op. The bus access will complete without affecting any data in the W89C840F internal registers.

2) Read from the reserved or un-implemented registers will be returned 0's value.

3) S/W reset has no effect on the PCI configuration registers.

4) H/W reset will clear the PCI configuration registers.

5) The implemented configuration registers support any byte enable combination access.

6) Burst access to the configuration registers will be terminated after 1st data transfer completed with a with a disconnect without data.

The following table outlined all the PCI configuration registers inside this chip and summarized its function.

Code	Abbr.	Meaning	System I/O offset
F00	FID	Identification	00H
F04	FCS	Command and status	04H
F08	FREV	Revision	08H
F0C	FLT	Latency timer	0cH
F10	FBIOA	Base I/O address	10H
F14	FBMA	Base memory address	14H
----	----	Reserved	18~28H
F2c	FSSID	Subsystem ID	2cH
F30	FERBA	Expansion ROM base address	30H
----	----	Reserved	34~38H
F3c	FIR	Interrupt	3cH
F40	FSR	Signature	40H

The initial value of the W89C840F PCI configuration registers after hardware reset and software reset is listed as following table.

Code	Abbr.	hardware reset	software reset
F00	FID	00000000H	non affected
F04	FCS	02800000H	non affected
F08	FRE	02000000H	non affected
F0C	FLT	00000000H	non affected
F10	FBIOA	FFFFFF81H	non affected
F14	FBMA	FFFFFF80H	non affected
F2c	FSSID	00000000H	non affected
F30	FERBA	00000000H	non affected
F3c	FIR	00000100H	non affected
F40	FSR	00000012H	non affected

F00/FID Device ID Register

The register F00/FID specifies the vendor ID and the particular device ID in the W89C840F.

Bit	Attribute	Bit name	Description
31:16	R	DID	Device ID. Loaded from EEPROM after hardware reset de-asserted.
15:0	R	VID	VendorID. Loaded from EEPROM after hardware reset de-asserted.

F04/FCS Command and Status Register

The F04/FCS comprises two parts, the one is the command register (FCS[15:0]) which provides the control of 840 PCI activity, and the other is the status register (FCS[31:16]) which shows the status information of PCI event.

Writing 00h to the command registers will put W89C840F logically isolated from all PCI access except configuration access.

Writing 1 to the bits of the status register will clear them; writing 0 has no effect.

Bit	Attribute	Bit name	Description
31	R/W	DPE	Detected Parity Error. The DPE will be set if a parity error is detected by W89C840F even the parity error response bit of F04/FCS(bit 6) is disabled.
30	R/W	SSE	Signaled System Error. The SSE will be set if W89C840F assert SERRB.
29	R/W	RMA	Received Master Abort. The RMA will be set if 840 master transaction take a master abort.
28	R/W	RTA	Received Target Abort. The RTA will be set if the 840 master transaction is terminated by a target abort.
27	R/W	STA	Signaled Target Abort. The STA will be set if the W89C840F slave transaction take a target abort.
26:25	R	DT	DEVSEL# Timing: Fixed at 01 to indicate a medium DEVSEL# assert timing.

24	R/W	DPED	Data Parity Error Detected. The DPED will be set if the following three conditions are met: 1). The W89C840F asserts PERRB or detects out that PERRB asserted by other device. 2). The W89C840F acts as a master in the transaction that the error occurs. 3). The parity error response bit (bit 6) is set.
23	R	FBTBC	Fast Back to Back Capable. Fixed at 1 to indicate capability of accepting fast back to back transactions which are not accessing to the same target.
22:9	R	---	Reserved. Fixed at 0.
8	R/W	SE	SERR# Enable. Set SE high to enable the W89C840F to assert SERR# if an address parity error is detected. This bit and bit 6 must be set 1 to signal SERR event.
7	R	----	Reserved. Fixed at 0.
6	R/W	PER	Parity Error Response. Set PER to high to enable the W89C840F to respond to parity error. When PER is reset, the W89C840F will ignore any parity error and continue the normal operation. The W89C840F internal parity checking and generation function will not be disabled even PER is reset.
5:3	R	---	Reserved. Fixed at 0.
2	R/W	BM	Bus Master. Set BM to high will allow W89C840F acting as a bus master. Reset BM to low will disable the W89C840F's bus master ability.
1	R/W	MS	Memory Space. Set MS to high will allow W89C840F to respond to memory space access by the host.
0	R/W	IOS	I/O Space. Set IOS to high will allow W89C840F to respond to I/O space access by the host.

F08/FREV Device Revision Register

This register, a read-only with built-in code, shows W89C840F revision number and its class code.

Bit	Attribute	Bit name	Description

31:24	R	BC	Base Class Code. Fixed at 02h to indicate a network controller.
23:16	R	SC	Subclass Code. Fixed at 00h to indicate a Ethernet controller.
15:8	R	IC	Interface Code. Fixed at 0.
7:0	R	REV	Revision ID. This field represents the revision number. Loaded from EEPROM after hardware reset de-asserted

F0C/FLT Latency Timer Register

This register specify the W89C840F master bus latency timer.

Bit	Attribute	Bit name	Description
31:16	R	---	Fixed to 0.
15:8	R/W	LT	Latency Timer. Specify, in units of PCI clocks, the latency timer value of W89C840F. When W89C840F asserts FRAMEB, its latency timer starts counting up. The W89C840F will initiate the transaction termination as soon as its GNT# de-asserted If the timer expired before W89C840F de-asserts FRAMEB.
7:0	R	---	Fixed at 0.

F10/FBIOA Base I/O Address Register

This register is written by software after power-on to specify W89C840F base I/O address in the system.

Bit	Attribute	Bit name	Description
31: 7	R/W	BIOA	Base I/O Address. Written by power-on software to specify base I/O address. The W89C840F requires a 128 bytes wide I/O space.
6:1	R	---	Reserved. Fixed at 0.
0	R	IO	I/O Space Indicator. Fixed at 1.

F14/FBMA Base Memory Address Register

This register is written by power-on software to specify W89C840F base memory address in the system.

Bit	Attribute	Bit name	Description
31: 7	R/W	BMA	Base Memory Address. Written by power-on software to specify base memory address. The W89C840F requires a 128 bytes wide memory space.
6:1	R	---	Reserved. Fixed at 0.
0	R	MEM	Memory Space Indicator. Fixed at 0.

F2C/FSSID Subsystem ID Register

This register is loaded from the external EEPROM. The W89C840F will issue a Retry signals to host when the host tries to access to this register while the EEPROM auto-loading is not yet completed.

Bit	Attribute	Bit name	Description
31:16	R	SBID	Subsystem ID. Loaded from EEPROM after Hardware reset de-asserted.
15:0	R	SBVID	Subsystem Vendor ID. Loaded from EEPROM after Hardware reset de-asserted

F30/FERBA Expansion ROM Base Address Register

This register is written by power-on software to specify the on-board boot ROM base address in the system.

Bit	Attribute	Bit name	Description
31:13	R/W	EROMB	Expansion ROM Base Address. Written by power-on software to specify expansion ROM base address. The W89C840F will request op to 256K bytes memory space for the on board boot ROM device according the configuration of C48/CBRCR. The return back read value of bit 0 to bit 17 of F30/FERBA will depend on the configuration of C48/CBRCR.
12:1	R	---	Reserved. Fixed at 0.
0	R/W	ROME	Expansion ROM Enable. Set both this bit and F04/FCS bit 1 to 1 to enable expansion ROM access ability. The F04/FCS bit 1 has precedence over this bit.

F3C/FIR Interrupt Register

The upper half of this register is loaded from external serial EEPROM while the lower half is written. The W89C840F will issue a Retry signals to host when the host tries to access to this register while the EEPROM auto-loading is not yet completed.

Bit	Attribute	Bit name	Description
31:24	R	MAXLAT	Max_Lat. This indicates how often, in units of 0.25µS, the W89C840F needs to gain access to PCI bus. Assuming PCI clock rate is 33 MHz.
23:16	R	MINGNT	Min_Gnt. This indicates how long a burst period, in units of 0.25µS, is needed by the W89C840F. Assuming PCI clock rate is 33 MHz.
15:8	R	IPIN	Interrupt Pin. Fixed at 01H to indicate INTA# is used.
7:0	R/W	ILINE	Interrupt Line. Written by power-on software to specify routing of interrupt line.

F40/FSR Signature Register

The F40/FSR register is designed for identifying the hardware of W89C840F.

Bit	Attribute	Bit name	Description
31:16	R/W	DVAR	Driver Area This field is for driver special use. The driver can write some specific pattern to these bits for bundling the software and hardware of W89C840F together.
15:8	R	---	Reserved. Fixed at 0.
7:0	R	SIG	Signature. After the hardware reset, these 8 bits value is toggled as following SIG = 12H at (2N-1)th read 9AH at 2Nth read where N= 1, 2, ...

W89C840F register

The W89C840F is implemented many registers, listed in the table below, to perform the function control and monitor the status of MAC.The general attributes of the W89C840F register is described as the following:

1) The W89C840F register are mapped into the host I/O or memory space.

2) The registers of the W89C840F are long word-aligned. Each register consists of 32 bits and may be accessed using any byte enable combinations with long word-aligned address.

3) The byte enabling and addressing must meet the specification for I/O access addressing rule when the register is in I/O space.

4) Burst access to the W89C840F register will be terminated after 1st data transfer completed with a Disconnect without Data.

5) S/W reset will have the same effect as done by H/W reset on the W89C840F register, except for the registers or bits C00<0>, C38, C3c, C40, C44, C48.

6) Any read on the reserved register will be returned with 0‘s value.

The following table outlined all the control/status registers inside this chip and its offset address, and summarized its function.

Code	Abbr.	Meaning	Base offset from FBIOA, FBMA
C00	CBCR	Bus Control	00H
C04	CTSDR	Transmit Start Demand	04H
C08	CRSDR	Receive Start Demand	08H
C0C	CRDLA	Receive Descriptor List Address	0CH
C10	CTDLA	Transmit Descriptor List Address	10H
C14	CISR	Interrupt Status	14H
C18	CNCR	Network Configuration	18H
C1C	CIMR	Interrupt Mask	1CH
C20	CFDCR	Frame Discarded Counter	20H
C24	CMIIR	MII Management and ROM	24H
C28	CBROA	Boot ROM Offset Address	28H
C2C	CGTP	General Timer	2CH
C30	CRDAR	Current Receive Descriptor Address	30H
C34	CRBAR	Current Receive Buffer Address	34H
C38	CMA0	Multicast Address 0	38H
C3C	CMA1	Multicast Address 1	3CH
C40	CPA0	Physical Address 0	40H
C44	CPA1	Physical Address 1	44H
C48	CBRCR	Boot ROM Size Configuration	48H
C4c	CTDAR	Current Transmit Descriptor Address	4cH

C50	CTBAR	Current Transmit Buffer Address	50H
C54~CFF	reserved	reserved	reserved

This table lists the initial state of each register in the W89C840F after hardware reset and software reset seperately.

Code	Abbr.	hardware reset	software reset
C00	CBCR	00000010H	00000010H
C04	CTSDR	00000000H	00000000H
C08	CRSDR	00000000H	00000000H
C0C	CRDLA	00000000H	00000000H
C10	CTDLA	00000000H	00000000H
C14	CISR	03800000H	03800000H
C18	CNCR	20000030H	20000030H
C1C	CIMR	00000000H	00000000H
C20	CFDCR	00000000H	00000000H
C24	CMIIR	00000000H	00000000H
C28	CBROA	00000000H	00000000H
C2C	CGTP	00000000H	00000000H
C30	CRDAR	00000000H	00000000H
C34	CRBAR	00000000H	00000000H
C38	CMA0	00000000H	not affected
C3C	CMA1	00000000H	not affected
C40	CPA0	00000000H	not affected
C44	CPA1	00000000H	not affected
C48	CBRCR	00000000H	not affected
C4c	CTDAR	00000000H	00000000H
C50	CTBAR	00000000H	00000000H

The detail function and operation for each register in the W89C840F will be described in the following paragraph. There are total 21 registers to be described in register code order in this paragraph.

The full name of these registers are C00/CBCR Bus Control Register, C04/CTSDR Transmit Start Demand Register, C08/CRSDR Receive Start Demand Register, C0C/CRDLA Receive Descriptors List Addresses, C10/CTDLA Transmit Descriptors List Addresses, C14/CISR Interrupt Status Register, C18/CNCR Network Configuration Register, C1C/CIMR Interrupt Mask Register, C20/CFDCR Frame Discarded Counter Register, C24/CMIIR MII Management and ROM Register, C28/CBROA Boot ROM Offset Address Register, C2C/CGTR General Timer Register, C30/CRDAR Current Receive Descriptor Address Register, C34/CRBAR Current Receive Buffer Address Register, C38/CMA0 Multicast Address Register 0, C3C/CMA1 Multicast Address Register 1, C40/CPA0 Physical Address Register 0, C44/CPA1

Physical Address Register 1, C48/CBRCR Boot ROM Size Configuration Register, C4C/CTDAR Current Transmit Descriptor Address Register and C50/CTBAR Current Transmit Buffer Address Register.

C00/CBCR Bus Control Register:

This register defines the configuration of bus master, including the wait state control, the endian mode control of the descriptor, cache alignment control, burst length control, descriptor skip length and the internal bus access priority. In addition to the bus master control, the software reset will be performed after programming a logic 1 to the software reset bit of C00/CBCR. Before writing data to the C00/CBCR, the transmit and receive processes must be stopped. Otherwise the current transmit or receive operation will not be completed correctly.

The following table detailedly described the function of each bit of the register C00/CBCR.

Bit	Attribute	Bit name	Description
31:22	R	---	Reserved. Fixed at 0.
21	R/W	WAIT	Wait State Insertion When WAIT is set, the W89C840F, as a bus master, executes memory read/write with one wait state every data phase. When WAIT is reset, the W89C840F, as a bus master, executes memory read/write with zero wait state every data phase.
20	R/W	DBE	Descriptor Big Endian Mode When set, the descriptors will be handled in big endian mode; when reset, the descriptors will be treated in little endian mode
19:16	R	---	Reserved. Fixed at 0.
15:14	R/W	CA	Cache Alignment CA defines the address boundary for the burst access to the transmission or receive data. When the starting address of the data burst access is not aligned, more specifically, the starting address should be a multiple of some number such as 4, 8 etc., the W89C840F will have the first burst transfer that causes that the next burst access will has the start address aligned. After the first burst occurred, all other burst operation are aligned with the configuration of CA accordingly. The CA must be initialized with a non zero value after reset. The alignment configuration is as following: [15:14] Address Alignment -- [00] reserved [01] 8 long-word alignment [10] 16 long-word alignment [11] 32 long-word alignment

13:8	R/W	BL	Burst Length BL defines the maximum number of the long words that can be transferred within one PCI burst transaction. The burst length configuration is as following. [13:8] Burst Length -- 00H refer to CA 01H 1 long word 02H 2 long word 04H 4 long word 08H 8 long word 10H 16 long word 20H 32 long word other reserved
7	R/W	BBE	Buffer With Big Endian When set, the data buffers are treated with big endian ordering. When reset, the data buffers are treated with little endian ordering.
6:2	R/W	SKIP	Skip Length Between Descriptors This field specifies the skip length between two descriptors (from the start address of the current descriptor to the start address of the next descriptor). The unit of the skip length is long word. The default value after hardware or software reset is 04H.
1	R/W	ARB	Arbitration Between Tx And Rx Processes When set, the TX process and RX process will have the right to use the internal bus with the same priority. When reset, the RX process will have higher priority than TX process with regarding to the internal bus utilization.
0	R/W	SWR	Software Reset. Set SWR to high will reset most internal registers (except that C38, C3c, C40, C44, C48, and PCI Configuration Registers). The software reset will be lasted for 4 PCI clocks and the bit will self-clean after software reset completed. If any consequent access to the W89C840F is coming during this reset process, the W89C840F will delay asserting TRDY# until the reset process is completed. This bit is default 0 after hardware reset.

C04/CTSDR Transmit Start Demand Register

The register C04/CTSDR is used to request the W89C840F to do a transmission process.

Bit	Attribute	Bit name	Description

31:0	W	TSD	Transmit Start Demand A write to this register will trigger the W89C840F's transmit DMA to fetch the descriptor for progressing the transmission operation when the W89C840F's transmit DMA is staying at the suspend state. Otherwise, the write operation will have no effect. The W89C840F's transmit DMA will return to the suspend state if no descriptor is available. Meanwhile, the bit 2 of C14/CISR will be asserted to claim the transmit buffer unavailable If there is any descriptor available, W89C840F will start to the transmit process.

C08/CRSDR Receive Start Demand Register

The register C04/CTSDR is used to request the W89C840F to do a receive process.

Bit	Attribute	Bit name	Description
31:0	W	RSD	Receive Start Demand A write to this register will trigger the W89C840F's receive DMA to fetch the descriptor for progressing the receiving operation when the W89C840F's receive DMA is staying at the suspend state. Otherwise, the write operation will have no effect. The W89C840F's receive DMA will return to the suspend state if no descriptor is available. Meanwhile, the bit 7 of C14/CISR will be asserted to claim the receive buffer unavailable. If there is any descriptor available, W89C840F will start to the receive process and waiting for the incoming frames.

C0C/CRDLA Receive Descriptors List Addresses

The register C0C/CRDLA defines the start address of the receive descriptor list. It should be updated only when the receive DMA state machine is staying at the stop state.

Bit	Attribute	Bit name	Description
31:2	R/W	SRL	Start of Receive List.
1:0	R/W	MBZ	Must be written as 0 for long word alignment.

C10/CTDLA Transmit Descriptors List Addresses

The register C10/CTDLA defines the start address of the transmit descriptor list. It should be updated only when the transmission DMA state machine is staying at the stop state.

Bit	Attribute	Bit name	Description
31:2	R/W	STL	Start of Transmit List.
1:0	R/W	MBZ	Must be written as 0 for long word alignment.

C14/CISR Interrupt Status Register

Most bits of the C14/CISR report the interrupt status. The assertion of the interrupt status, reported by bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 10, 11 and 13, and the corresponding interrupt mask bits will cause a hardware interrupt to the host.

A write with 1's value the status bit will clear them and write 0 will have no effect.

Bit	Attribute	Bit name	Description
31:26	R	---	Reserved. Fixed at 0.
25:23	R	BET	Bus Error Type. The field indicates the error type of bus error and is valid only when bit 13, bus error, is set. the assertion of these bits does not generate interrupt. The definition of bus error is as follows. BET[25:23] Error State --------------- ------------------ 000 Parity Error 001 Master Abort 010 Target Abort 011 Reserved. 1xx Reserved. The meanings of the error type is described as following. * Parity Error --- When W89C840F operates as a bus master, it can detect a data parity error during a read transaction or sample PERRB asserted on a write transaction if Parity Error Response bit (F04[6]) is set. * Master Abort --- When W89C840F operates as a bus master, W89C840F terminates the read or write transaction with master abort. * Target Abort --- When W89C840F operates as a bus master, the read or write transaction is terminated with target abort. The initial state of this field after reset is zero.
22:20	R	TPS	Transmit Process State. This field indicates the transmit state. This field does not generate interrupt.
19:17	R	RPS	Receive Process State. This field indicates the receive state. This field does not generate interrupt.

16	R	NIR	Normal Interrupt Report. The normal interrupt report includes transmit completed interrupt, transmit buffer unavailable interrupt and the receive completed interrupt. The NIR is a logical OR result of the bits 0, 2, 6 of the register C14/CISR. Only the bits corresponding to the unmasked bits of C1C/CIMR will affect this bit.
15	R	AIR	Abnormal Interrupt Report. The abnormal interrupt includes transmit process in idle state interrupt, receive early interrupt, receive error interrupt, transmit FIFO under-flow interrupt, receive buffer unavailable interrupt, receive idle state interrupt, transmit early interrupt, timer expire interrupt and the bus error interrupt. The AIR is a logical OR result of the bits 1, 3, 4, 5, 7, 8, 10, 11, 13 of the register C14/CISR. Only these bits corresponding to the unmasked bits of the C1C/CIMR will affect this bit.
14	R	---	Reserved. Fixed at 0.
13	R/W	BE	Bus Error. A high indicates a bus error happened. The error type will be shown by bit 25~23.
12	R	---	Reserved. Fixed at 0.
11	R/W	TE	Timer Expired. A high indicates the general timer (C2C/CGTR) expired.
10	R/W	TEI	Transmit Early Interrupt The W89C840F will has Transmit Early Interrupt status set after the packet to be transmitted is completely transferred into the transmit FIFO if Transmit Early Interrupt On bit of C18/CNCR is set. The TEI will be cleared automatically after the packet is transmitted out from the transmit FIFO completely.
9	R	---	Reserved. Fixed at 0.
8	R/W	RIDLE	Receive in Idle State. Set means the receive DMA state machine is in the idle state.
7	R/W	RBU	Receive Buffer Unavailable. When there is no receive buffer available, this bit is set and the receive process enters the suspend state. When W89C840F is first initialized, this bit will not be set even if there is no buffer available. It will be set only when there has been any available buffer and no available buffer afterwards. The RBU will not accumulate the number of the receive buffer unavailable event, i.e. the write an 1‘s value to RBU will clear the RBU no matter how many times the receive buffer unavailable has been occurred before the RBU is cleared.

6	R/W	RINI	Receive Interrupt A high indicates that a frame has been received and the receive status is transferred into the receive descriptors of the current frame.
5	R/W	IUF	Transmit FIFO Under-flow A high indicates that the transmit FIFO had an under-flow error during the packet transmission. After the FIFO under-flow occurred, the transmit DMA will not continue to fetch the un-transmitted data of the current frame but fetch the descriptor of the current frame for looking for the last descriptor of the current frame. The W89C840F's transmit DMA state machine will write the transmit status to the last descriptor of the current frame with a 1's value for the bit 1 of Transmit Descriptor 0 (T00[1]). The W89C840F will continue to transmit next packet when the current frame transmit status is updated..
4	R/W	RERR	Receive Error. A high indicates that the receive DMA detects a receive error during the packet reception. The receive DMA will set this bit when some prior received data of the current incoming packet have been moved into the data buffer in the host memory and some kind of error occurred when receiving the posterior data of the current incoming packet from the MII bus. The INTAB will be asserted when a receive error is detected and the receive error interrupt enable is unmasked and the error packet will be aborted.
3	R/W	REI	Receive Early Interrupt The REI will be set when the number of the data of the incoming frame, in long word unit, transferred to the data buffer reaches Receive Early Interrupt Threshold specified by the register C18/CNCR if Receive Early Interrupt On in the register C18/CNCR is set. This bit will be cleared automatically after Receive Interrupt (RINI) or Receive Error (RERR) is set..
2	R/W	TBU	Transmit Buffer Unavailable A high indicates that there is no available transmit descriptor during or after the packet transmission. The transmit process will stay in suspend state. The TBU will not accumulate the number of transmit buffer unavailable event, i.e. write an 1 value to TBU will clear the TBU, no matter how many times the transmit buffer unavailable has been occurred before the TBU is cleared.
1	R/W	TIDLE	Transmit Process in Idle State. A high indicates the transmit state machine is in the idle state.

0	R/W	TINI	Transmit Interrupt The TINI will be set when a frame transmit is completed and the FINT (bit 31) of Transmit Descriptor 1 (T01) is set.

C18/CNCR Network Configuration Register

The register C18/CNCR defines the configuration for the data transmission or receiving and the interrupt algorithm for interrupt assertion.

Bit	Attribute	Bit name	Description
31	R/W	REIO	Receive Early Interrupt On The receive early interrupt function will be enabled when the REIO is set to high. Otherwise, the receive early interrupt function will be disabled. During receiving packet data, the W89C840F will assert an interrupt request when the bytes number of the received data, which the receive DMA has moved them into the data buffer in the system memory , excesses the receive early interrupt threshold.
30	R/W	TEIO	Transmit Early Interrupt On The transmit early interrupt function will be enabled when the TEIO is set to high. Otherwise, the transmit early interrupt function will be disabled. The W89C840F will assert an early transmit interrupt when all the current packet data have been moved into the 2 Kbytes transmit FIFO no matter the data have been put onto the MII interface completely or not.
29	R/W	FES	Fast Ethernet Select When set, W89C840F will run in 100 Mbps mode. When reset, W89C840F run in 10 Mbps mode. To change this bit, the transmit state machine must be in Idle state. The SQE test function will be enabled when FES is reset to low.

28:21	R/W	REIT	Receive Early Interrupt Threshold During receiving packet, the W89C840F will assert an interrupt request when the bytes number of the received data, which the receive DMA has moved them into the data buffer, excesses the receive early interrupt threshold. To set this field 00H will disable receive early interrupt function. The setting of the receive early interrupt is as following. REIT[28:21] receive early interrupt threshold ---------------- ----------------- 01H 4 bytes 02H 8 bytes -- -- 0fH 60 bytes 10H 64 bytes -- -- ffH 020 bytes
20:14	R/W	TTH	Transmit Threshold. These bits select the transmit threshold level of the transmit FIFO. The packet Transmission will be started immediately once the data queued into the transmit FIFO has reached the threshold level. The transmission will also be started immediately when the full packet has been transferred into the transmit FIFO even though the frame length is less than the TTH level. To change this bit, the transmit state machine must be in Idle state. The following table shows there is a difference with 16 bytes for each consecutive setting value in this field, except that the first one in the table. TTH[20:14] --------------- ----------------- 00H full packet 01H 16 bytes 02H 32 bytes -- -- 0fH 240 bytes 10H 256 bytes -- -- 7fH 2032 bytes

13	R/W	TXON	Transmit On. When set, the transmission process will be started (leave the Idle state, at first, and fetch the transmission descriptor according to the configuration of C10/CTDLA). When reset, the transmission state machine will be stopped after the current frame is completed (transmitted successfully or transmission abort with excessive collision). The register C10/CTDLA must be programmed before setting TXON high.
12	R	---	Reserved. Fixed at 0.
11:10	R/W	LBK	Loopback Mode. The LBK selects the W89C840F loop-back modes: LBK[11:10] Loop-back Mode -------------- ---------------------- 00 Normal mode 01 Internal Loop-back 10 External Loop-back
9	R/W	FD	Full Duplex Mode. When set, the W89C840F will perform the full duplex function. When reset, the W89C840F works in half duplex mode. In full duplex mode, the W89C840F can transmit and receive packets at the same time. In half duplex mode, the W89C840F can only exclusively either transmit or receive. The W89C840F is not allowed to be programmed in internal loop-back mode when it is in full duplex mode. To change this mode setting, be sure W89C840F is completely idle and the Receive On bit (RXON) and the Transmit On bit (TXON) are both reset.
8	R	---	Reserved. Fixed at 0.
7	R/W	AEP	Accept Error Packet. When set, all incoming packets passed address filtering will be accepted, including runt packets, CRC error packets, and dribbling bit error packets. When reset, only the valid incoming packets will be accepted. Default 0.
6	R/W	ARP	Accept Runt Packet. When set, the incoming packets pass the address filtering with the length less than 64 bytes are accepted. When reset, the incoming packets pass the address filtering with the length less than 64 bytes are rejected. Default 0.
5	R/W	ABP	Accept Broadcast Packet. When set, all incoming packets with a broadcast address will be accepted. When reset, the incoming packets with a broadcast address will be rejected. Default 1.

4	R/W	AMP	Accept Multicast Packet. When set, all incoming packets with a multicast address match the node multicast address table (MAR7 ~ MAR0) will be accepted. When reset, all incoming packets with a multicast address (excluding broadcast address) will be rejected. Default 1.
3	R/W	APP	Accept All Physical Packet. When set, all incoming packets with unicast address will be accepted. When reset, only the incoming packets with destination address matching the physical address of the node will be accepted. Default 0.
2	R	---	Reserved. Fixed at 0.
1	R/W	RXON	Receive On. When set, the receive process will be started (leave the Idle state, at first, and fetch the receive descriptor according to the configuration of the register C0C/CRDLA). When reset, the receive state machine will be stopped after the current frame is completed. The C0C/CRDLA, C40/PAR0, C44/PAR1, C38/MAR0 and C3C/MAR1 registers must be programmed before setting the RXON high.
0	R	---	Reserved. Fixed at 0.

C1C/CIMR Interrupt Mask Register

The register C1C/CIMR controls the interrupt enable corresponding to the bits in the register C14/CISR.

Bit	Attribute	Bit name	Description
31:17	R	---	Reserved. Fixed at 0.
16	R/W	NIE	Normal Interrupt Enable. The Normal Interrupt will be enabled if the NIE is set to high. The Normal Interrupt is disabled when the NIE is reset to low. The hardware interrupt will be asserted if both the NIE bit of the C1C/CIMR and the NIR bit of the C14/CISR NIR are set to high.
15	R/W	AIE	Abnormal Interrupt Enable. The Abnormal Interrupt will be enabled if the AIE is set to high. The Abnormal Interrupt is disabled when the AIE is reset to low. The hardware interrupt will be asserted if both the AIE bit of the C1C/CIMR and the AIR bit of the C14/CISR AIR are set to high.
14	R	---	Reserved. Fixed at 0.

13	R/W	BEE	Bus Error Enable. The Bus Error Interrupt will be enabled if both AIE(bit 15) and BEE are set to high, otherwise, the Bus Error Interrupt will be disabled. The hardware interrupt will be asserted if all of the AIE bit of the C1C/CIMR, the BEE bit of the C1C/CIMR and the BE bit of the C14/CISR are set to high at the same time.
12	R	---	Reserved. Fixed at 0.
11	R/W	TEE	Timer Expired Enable. The Timer Expired Interrupt will be enabled if both AIE(bit 15) and TEE are set to high, otherwise, the Timer Expired Interrupt will be disabled. The hardware interrupt will be asserted if all of the bit AIE in C1C/CIMR, the bit TEE in C1C/CIMR and the bit TE C14/CISR are set to high at the same time.
10	R/W	TEIE	Transmit Early Interrupt Enable. The Transmit Early Interrupt will be enabled if both AIE(bit 15) and TEIE are set to high, otherwise, the Transmit Early Interrupt will be disabled. The hardware interrupt will be asserted if all of the bit AIE in C1C/CIMR, the bit TEIE in C1C/CIMR and the bit TEI in C14/CISR are set to high at the same time.
9	R	---	Reserved. Fixed at 0.
8	R/W	RIE	Receive Idle Enable. The Receive Idle Interrupt will be enabled if both AIE(bit 15) and RIE are set to high, otherwise, the Receive Idle Interrupt will be disabled. The hardware interrupt will be asserted if all of the bit AIE in C1C/CIMR, the bit RIE in C1C/CIMR and the bit RIDLE in C14/CISR are set to high.
7	R/W	RBUE	Receive Buffer Unavailable Enable. The Receive Buffer Unavailable Interrupt will be enabled if both AIE(bit 15) and RBUE are set to high, otherwise, the Receive Buffer Unavailable Interrupt will be disabled. The hardware interrupt will be asserted if all of the bit AIE in C1C/CIMR,the bit RBUE in C1C/CIMR and the bit RBU in C14/CISR are set to high.
6	R/W	RINTE	Receive Interrupt Enable. The Receive Interrupt will be enabled if both NIE(bit 16) and RINTE are set to high, otherwise, the Receive Interrupt will be disabled. The hardware interrupt will be asserted if all of the bit NIE in C1C/CIMR, the bit RINTE in C1C/CIMR and the bit RINI in C14/CISR are set to high.
5	R/W	TFUE	Transmit FIFO Underflow Enable. The Transmit FIFO Underflow Interrupt will be enabled if both AIE(bit 15) and TFUE are set to high, otherwise, the Transmit FIFO Underflow Interrupt will be disabled. The hardware interrupt will be asserted if all of the bit AIE in C1C/CIMR, the bit TFUE in C1C/CIMR and the bit IUF in C14/CISR are set to high.

4	R/W	RERRE	Receive Error Enable. The Receive Error Interrupt will be enabled if both AIE(bit 15) and RERRE are set to high, otherwise, the Receive Error Interrupt will be disabled. The hardware interrupt will be asserted if all of the bit AIE in C1C/CIMR, the bit RERRE in C1C/CIMR and the bit RERR in C14/CISR are set to high.
3	R/W	REIE	Receive Early Interrupt Enable. The Receive Early Interrupt will be enabled if both AIE(bit 15) and REIE are set to high, otherwise, the Receive Early Interrupt will be disabled. The hardware interrupt will be asserted if all of the bit AIE in C1C/CIMR, the bit REIE in C1C/CIMR and the bit REI in C14/CISR are set to high.
2	R/W	TBUE	Transmit Buffer Unavailable Enable. The Transmit Buffer Unavailable Interrupt will be enabled if both NIE(bit 16) and TBUE are set to high, otherwise, the Transmit Buffer Unavailable Interrupt will be disabled. The hardware interrupt will be asserted if all of the bitsNIE and TBUE in C1C/CIMR and the bit TBU in C14/CISR are set to high.
1	R/W	TIE	Transmit Idle Enable. The Transmit Idle Interrupt will be enabled if both AIE(bit 15) and TIE are set to high, otherwise, the Transmit Idle Interrupt will be disabled. The hardware interrupt will be asserted if all of the C1C/CIMR AIE, C1C/CIMR TIE and C14/CISR TIDLE are set to high.
0	R/W	TINTE	Transmit Interrupt Enable. The Transmit Interrupt will be enabled if both NIE(bit 16) and TINTE are set to high, otherwise, the Transmit Interrupt will be disabled. The hardware interrupt will be asserted if all of the bits NIE and TINTE in C1C/CIMR and the bit TINI in C14/CISR are set to high.

C20/CFDCR Frame Discarded Counter Register

The register C20/CFDCR records the missed packet count and the FIFO overflow count.

Bit	Attribute	Bit name	Description
31	R	MRFO	More Receive FIFO Overflow This bit is the overflow bit of the receive FIFO Overflow counter. The actual number of the FIFO overflow must be more than the number shown by the bits field RFOC if the MRFO is set to high. This bit will be reset after a read operation

30:17	R	RFOC	Receive FIFO Overflow Counter The RFOC indicates the number of the packets that are discarded due to the receive FIFO overflow under the condition of the receive buffer is not available. This counter will be reset after being read by the driver program.
16	R	MMP	More Missed Packets Overflow bit of Missed Packet Counter. The actual number of the missed packet must be more than the number shown by the bits field MPC if MMP is set tot high. This bit will be reset after read by a read operation.
15:0	R	MPC	Missed Packet Counter The MPC indicates the number of packets that are discarded due to the receive FIFO overflow which is caused by that the receive DMA can not get sufficient utilizing on PCI bus, in which, the receive data buffer is available for the current frame. Although there is a receive data buffer available for the current frame, the received data of the current frame in the FIFO can not be completely moved into the data buffer in host memory before the receive FIFO is overflow if the receive DMA can not get sufficient utilizing on PCI bus. This counter will be reset after a read operation.

C24/CMIIR MII Management and ROM Register

The register C24/CMIIR is used to specify the control function and the data message passing for the on board EEPROM and boot ROM device access.

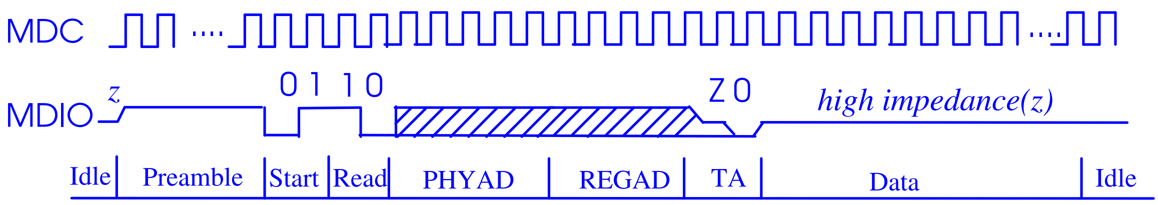
The followed table described the MII management frame format:

	MII Management Protocol							
	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
Read	1...1	01	10	AAAAA	RRRRR	Z0	16 bits	Z
Write	1...1	01	01	AAAAA	RRRRR	10	16 bits	Z

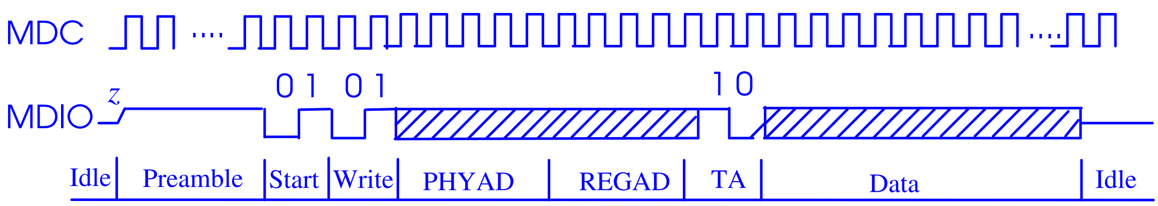
PRE:Preample, ST:Start of Frame, OP:Operation code, PHYAD:PHY address, REGAD:register address

TA:Turnaround.

The detailed timings for the read and the write operation, respectively, of the MII management function are illustrated as the figure below. Each bits in the management data frame(MDIO) are synchronized at the rising edge of the MII management clock(MDC)



Typical MDIO/MDC Read Cycle



Typical MDIO/MDC Write Cycle

Bit	Attribute	Bit name	Description
31:20	R	---	Reserved. Fixed at 0.
19	R	MDI	MII Management Port Data Input The MII management input data drove, by the external PHY , on the MIMDIO pin can be read from this bit when the MDSEL is reset. The MDI reflects the logic level on the MIMDIO pin instantly, no latching device is used for keeping the logic level message.
18	R/W	MDSEL	MII Management Port Read/Write Select The MIMDIO pin will be programmed as an input pin when the MDSEL is reset. On the other hand, the MIMDIO will be an output pin if MDSEL is set to high.
17	R/W	MDO	MII Management Port Write Data The state of the MDO will be directly output through the MIMDIO pin when the MIMDIO is performing an output pin. The serial command of the external physical device should be written into MDO serially with one bit data one MII management clock. The accessed data sequence and timing are shown as the diagram above .
16	R/W	MDC	MII Management Port Clock. The state of the MDC will be directly driven on the MIMDC pin for providing the MII management clock. To generate this clock source, the MDC should be programmed as 1 and 0 with equal duty cycle and timing width alternately. The AC timing specification with respect to the MIMDC and MIMDIO should follow the media independent interface(MII) specification defined in IEEE 802.3u.
15	R	---	Reserved. Fixed at 0.

14	R/W	RDCTL	BootROM Read Control. When EESEL(bit 11 in this register) is reset, setting this bit will perform the on-board boot ROM read operation with the reading address specified by the register C28/CBROA. The one byte data read from the on-board boot ROM will be latched into the bits field EEBRD[7:0] of this register. The bit RDCTL will be cleared automatically after BootROM read operation is completed. The RDCTL will not allow to be set high, even writing a logic 1 to RDCTL if the bit EESEL(bit 11 in this register) is set.
13	R/W	WRCTL	BootROM Write Control. When the bit EESEL (bit 11) is reset, setting this bit will trigger the W89C840F to perform the on-board boot ROM write operation with the writing address specified by the register C28/CBROA. The one byte write data should be latched by the EEBRD[7:0] before setting the WRCTL high. This bit will be cleared automatically if BootROM write operation is completed. The WRCTL will not allow to be set high, even writing a logic 1 to WRCTL if the bit EESEL(bit 11 in this register) is set.
12	R	---	Reserved. Fixed at 0.
11	R/W	EESEL	EEPROM/BootROM Select The on board boot ROM read/write function through CMIIR will be enabled if the EESEL is reset. Otherwise, on board boot ROM access function will be disabled and the CMIIR will be used to access the on board EEPROM device if the EESEL is set to high.
10:8	R	---	Reserved. Fixed at 0.
7:4	R/W	EEBRD [7:4]	EEPROM/Boot ROM Data 4 to 7: The EEBRD[7:4] are used to store the read/write data for the on board boot ROM access when EESEL is reset to low. The data of EEBRD[7:4] is of no meaning if the EESEL is set to high.

3:0	R/W	EEBRD [33:0]	EEPROM/Boot ROM Data 0 to 3: The EEBRD[3:0] are used to store the read/write data for the on-board boot ROM access when EESEL is reset to low. When EESEL is set to high, 1) the EEBRD[3] reflects the input data from the BtAdata3/EEDO pin(connected to EEPROM data output) instantly. 2) the EEBRD[2] stores the output data which will be drove onto the BtAdata2/EEDI pin(connected to EEPROM data input) directly. 3) the EEBRD[1] stores the output data which will be drove onto the BtAdata1/EECK pin (EEPROM serial clock input) directly. 4) the EEBRD[0] stores the output data which will be drove onto the EECS pin(connected to EEPROM chip select) directly. For accessing the external EEPROM device, the chip select signal, the serial clock and the data input should follow the AC specification defined by the external EEPROM device.

C28/CBROA Boot ROM Offset Address Register

The register C28/CBROA is used to specify the read or write address of the external boot ROM when accessing the boot ROM through the register C24/CMIIR of the W89C840F's.

Bit	Attribute	Bit name	Description
31:18	R	---	Reserved. Fixed at 0.
17:0	R/W	BROA	Boot ROM Offset Address. This field contains boot ROM offset address.

C2C/CGTR General Timer Register

The C2C/CGTR shows the real time content of the W89C840F's internal general timer

Bit	Attribute	Bit name	Description
31:17	R	---	Reserved. Fixed at 0.
16	R/W	RECUR	Recursive Mode: The state of the bit 0 to bit 15 in the register C2C/CGTR will be set to the states programmed by the driver program at the last time when the TIME timer count reaching zero if the RECUR is set to high. Default 0.

15:0	R/W	TIME	General Timer: The bits field TIME shows the content of the general timer inside the W89C840F . The internal general timer will count down from the pre-set value, a non zero value, programmed by the driver program automatically once the write transaction to the register C20/CGTR is completed. The time unit for the internal general timer count down is approximately 2048 times the cycle duration of the MII TXCLK. For instance, the count down time unit for a 25 Mhz MII TXCLK is approximately 82 us. The C14/CISR bit 11 will be set when TIME of C2C/CGTR reach zero. The TIME is default 0000H.

C30/CRDAR Current Receive Descriptor Address Register

The register C30/CRDAR shows that the start address of the receive descriptor which is used by the W89C840F receive DMA state machine to process the current receive frame.

Bit	Attribute	Bit name	Description
31:0	R	CRDA	Current Receive Descriptor Address. The CRDA represents the start address of the current receive descriptor which the W89C840F's receive DMA state machine is used to process the received frame.

C34/CRBAR Current Receive Buffer Address Register

The register C34/CRBAR shows that the start address of the host memory which will be used by the W89C840F's receive DMA state machine to store the current aligned long word data of the current received frame.

Bit	Attribute	Bit name	Description
31:0	R	CRBA	Current Receive Buffer Address. The CRBA contains the pointer current address in the on-using buffer of the host memory which will be used by the W89C840F receive DMA state machine to store the current aligned long word data of the current received frame.

C38/CMA0 Multicast Address Register 0

The C38/CMA0 defines the lower 32 bits of the total 64 bits multicast address hashing table.

Bit	Attribute	Bit name	Description
31:24	R/W	MAR3	Muticast Address 3. The MAR3 defines the bit 24~31 of the hashing table.
23:16	R/W	MAR2	Muticast Address 2. The MAR2 defines the bit 16~23 of the hashing table.

15:8	R/W	MAR1	Muticast Address 1. The MAR1 defines the bit 8~15 of the hashing table.
7:0	R/W	MAR0	Muticast Address 0. The MAR0 defines the bit 0~7 of the hashing table.

C3C/CMA1 Multicast Address Register 1

The C3C/CMA1 defines the upper 32 bits of the 64 bits multicast address hashing table.

Bit	Attribute	Bit name	Description
31:24	R/W	MAR7	Muticast Address 7. The MAR7 defines the bit 56~63 of the hashing table.
23:16	R/W	MAR6	Muticast Address 6. The MAR2 defines the bit 48~55 of the hashing table.
15:8	R/W	MAR5	Muticast Address 5. The MAR1 defines the bit 40~47 of the hashing table.
7:0	R/W	MAR4	Muticast Address 4. The MAR4 defines the bit 32~39 of the hashing table.

C40/CPA0 Physical Address Register 0

The C40/CPA0 defines the first 32 bits of the 48 bits MAC address. The CPA0 value is loaded from EEPROM after hardware reset

Bit	Attribute	Bit name	Description
31:24	R/W	PAR3	Physical Address 3. The PAR3 defines the bit 24~31 of the MAC address.
23:16	R/W	PAR2	Physical Address 2. The PAR2 defines the bit 16~23 of the MAC address.
15:8	R/W	PAR1	Physical Address 1. The PAR1 defines the bit 8~15 of the MAC address.
7:0	R/W	PAR0	Physical Address 0. The PAR0 defines the bit 0~7 of the MAC address.

C44/CPA1 Physical Address Register 1

The C44/CPA1 defines the last 16 bits of the 48 bits MAC address. The CPA1 value is loaded from EEPROM after hardware reset

Bit	Attribute	Bit name	Description
31:16	R	---	Reserved. Fixed at 0.
15:8	R/W	PAR5	Physical Address 5. The PAR5 defines the 40~47 bit of the 48 bit of the MAC address.
7:0	R/W	PAR4	Physical Address 4. The PAR0 defines the 32~39 bit of the 48 bit of the MAC address.

C48/CBRCR Boot ROM Size Configuration Register

This register is used to configure the size of the boot ROM. The bit 0 to bit 2 of the register C48/CBRCR are loaded form the external EEPROM after the deasserted of the hardware reset. The configuration of the BPS[2:0] will affect the return value from the register F30/FERBA to determine how large the expansion memory space the on-board boot ROM needs when it is read by the power-on software.

Bit	Attribute	Bit name	Description
31:3	R	---	Reserved. Fixed at 0.
2:0	R/W	BPS[2:0]	Boot ROM Size Select. The size of the on board boot ROM device is selected by BPS[2:0] as follows. BPS2 BPS1 BPS0 Size ------------------------- ---------------------- 0 0 X No Boot ROM 0 1 0 8K 0 1 1 16K 1 0 0 32K 1 0 1 64K 1 1 0 128K 1 1 1 256K

C4C/CTDAR Current Transmit Descriptor Address Register

The C4C/CTDAR shows that the start address of the descriptor which the W89C840F transmit DMA state machine is used to process the current frame.

Bit	Attribute	Bit name	Description
31:0	R	CTDA	Current Transmit Descriptor Address. The CTDA represents the start address of the current receive descriptor which the W89C840F's transmit DMA state machine is used to process the transmit frame.

C50/CTBAR Current Transmit Buffer Address Register

The C50/CTBAR shows that the address of the system memory from which the W89C840F's transmit DMA state machine will fetch the long word data and queue the data into the FIFO for transmission.

Bit	Attribute	Bit name	Description
31:0	R	CTBA	Current Receive Buffer Address. The CTBA contains the start address of the host memory from which the W89C840F transmit DMA state machine will fetch the long word data and queue it into the FIFO for transmission.

Descriptors

As described at the beginning of the function description, descriptors are used to handle the control and status information and the data of each received/transmitted frame. There are many information contained in descriptors, W89C840F totally implemented four registers for receiving descriptor and four registers for transmiting descriptor respectively. They are one for status descriptor, one for control descriptor, and two for buffer descriptors.

Receive Descriptors

R00, Receive Descriptor 0

The descriptor R00 is used to describe the received frame status.
After the current frame is received completely, the receive DMA state machine will update the valid status of the current received frame into the first and the last descriptor of the current received frame.
The Receive Access Control(RAC) bit is valid on each descriptor of the current frame. The receive DMA state machine will reset the RAC bit to release the descriptor for other receive operation when the data buffer pointed by this descriptor is full.

Bit	Symbol	Description

31	RAC	Receive Access Control The W89C840F receive DMA is allowed to access this descriptor if RAC is set to high by the driver program. Otherwise, the driver program will access this descriptor if the RAC is reset to low, i.e. the descriptor 0 allows to be accessed by software driver when set RAC;by hardware when reset RAC. The RAC is valid on each descriptor of the current received frame.
30	RCMP	Receive Completion. The receive DMA will set the RCMP of the first and the last descriptor of the current receive frame after the current frame is received and then transferred into the data buffer in host memory completely. This bit is valid only when either RFD (R00[9]) or RLD (R00[8]) is set, i.e. the first or the last descriptor of the current frame.
29:16	RBC	Receive Byte Count: The RBC indicates the length including CRC field of receive packet in byte unit. This bit is valid only when RFD (R00[9]) or RLD (R00[8]) is set, i.e. the first or the last descriptor of the current frame.
15	RE	Receive Error: When RE is set to high, it indicates any one of the following events occurred: R00[1] -- CRC error R00[6] -- Late event R00[7] -- Packet too long R00[11] -- Runt Packet This bit is valid only when RFD (R00[9]) or RLD (R00[8]) is set, i.e. the first or the last descriptor of the current frame.
13:12	RDT	Receive Data Type The RDT indicates the types of the packet received in the FIFO buffer. The receive DMA make a copy of the bits C18/CNCR[11:10] and write them to the bit field RDT when the current frame is received completely. The types of received packet is as following: 00 -- Normal receive packet 01 -- Internal loopback packet 10 -- External loopback 11 -- Reserved This bit is valid only when RFD (R00[9]) or RLD (R00[8]) is set, i.e. the first or the last descriptor of the current frame.
11	RP	Runt Packet : When set, it indicates that the received packet length is less than 64 bytes. This bit is valid only when RFD (R00[9]) or RLD (R00[8]) is set, i.e. the first or the last descriptor of the current frame.
10	MP	Multicast Packet : When set, it indicates that the received packet has a multicast address. This bit is valid only when RFD (R00[9]) or RLD (R00[8]) is set.

9	RFD	First Descriptor. When set, it indicates that this descriptor is the first descriptor of the current packet. The RFD is valid on each descriptor of the current receive frame.
8	RLD	Last Descriptor. When set, it indicates that this descriptor is the last descriptor of the current packet. The RLD is valid on each descriptor of the current receive frame. When both RFD and RLD are high, It means that the current receive frame is described by a single descriptor. When both RFD and RLD are low, it means that the current descriptor is neither the first nor the last descriptor of the current frame. When RFD is high and RLD is low, it means that the current descriptor is the first descriptor of the current frame. When RFD is low and RLD is high, it means that the current descriptor is the last descriptor of the the current frame.
7	PTL	Packet Too Long: When set, it indicates that the received packet length exceeds 2048 bytes. This bit is valid only when RFD (R00[9]) or RLD (R00[8]) is set, i.e. the first or the last descriptor of the current frame.
6	LE	Late Event: When set, it indicates that the MAC detected a receive collision event occurred at the time after the 64 bytes following Start Frame Delimiter (SFD) when the MAC is receiving the packet. This bit is valid only when RFD (R00[9]) or RLD (R00[8]) is set, i.e. the first or the last descriptor of the current frame.
3	MRE	MII Receive Error: When set, it indicates that the a receive error in the physical layer was reported during the frame reception. This bit is valid only when RFD (R00[9]) or RLD (R00[8]) is set, i.e. the first or the last descriptor of the current frame.
2	DB	Dribbling Bit : When set, it indicates that the receive packet contains an extra bits, not aligned with the 8 bits boundary. The received packet will be treated as a good packet even the DB bit is set if the CRC Error (R00[1]) is reset, i.e. no CRC error. This bit is not valid if a late collision (R00[6]) or runt packet (R00[11]) is set. This bit is valid only when RFD (R00[9]) or RLD (R00[8]) is set, i.e. the first or the last descriptor of the current frame.
1	CRCE	CRC Error: When set, it indicates that a cyclic redundancy check (CRC) error is occurred on the received packet. If there is a MII receive error is detected during the packet receiving, the CRC Error bit is also set even though the CRC may be correct. This bit is valid only when RFD (R00[9]) or RLD (R00[8]) is set, i.e. the first or the last descriptor of the current frame.

R01, Transmit Descriptor 1

The R01 is used to describe the receive control configuration for the current frame receiving.
The receive DMA state machine will fetch the first descriptor of the current frame , at first, to decide the receive control configuration for the current receive frame. The receive DMA state machine will also fetch each descriptor information before storing the received data to the data buffer in the host memory described by the current descritpor.

Bit	Symbol	Description
25	RLAST	Last Descriptor of the Ring. When set, it indicates the current descriptor is the last receive descriptor ring. This bit preempts the bit 24 (RLINK)of this descriptor. It means that the next descriptor pointer of the receive DMA state machine will automatically jump to the first descriptor pointed by the content of the register C0C/CTDLA, even the RLINK bit is set to high and the descriptor R03 points to an address other than the one specified by the register C0C/CRDLA. The RLAST is valid on each descriptor.
24	RLINK	Link Address in Receive Buffer Address 2 When set, it indicates that receive Buffer Address 2 in the descriptor R03 contains the start address of the next descriptor of the descriptor list. Otherwise the descriptor R03 will point to the start address of the receive buffer 2 when the RLINK is reset. The RLINK is valid on each descriptor.
23:12	RSZ2	Receive Buffer Size 2. The RSZ2 indicates the size, in bytes, of the second data buffer pointed by the current descriptor. If this field is 0, the W89C840F ignores this buffer. The buffer size must be long word aligned. The maximum size for this buffer is 4093 bytes.
11:0	RSZ1	Receive Buffer Size 1. The RSZ1 indicates the size, in bytes, of the first data buffer pointed by the current descriptor. If this field is 0, the W89C840F will ignore this buffer. The buffer size must be longword aligned. The maximum size of this buffer is 4093 bytes.

R02, Receive Descriptor 2

The R02 is used to specify the receive buffer 1 start address

Bit	Symbol	Description
31:0	RBA1	Receive Buffer Address 1 The RBA1 indicates the physical address, in the host memory space, of the first receive buffer pointed by the current descriptor. The RBA1 must be longword aligned. It is valid on each descriptor of the current frame.

R03, Receive Descriptor 3

The R03 is used to specify the start address of the receive buffer 2

Bit	Symbol	Description
31:0	RBA2	Receive Buffer Address 2 The RBA2 indicates the physical address, in the system memory space, of the second transmit buffer pointed by the current descriptor. The RBA2 must be must be longword aligned. It is valid on each descriptor of the current frame.

Transmit Descriptors

T00, Transmit Descriptor 0

The T00 is used to describe the transmited frame status.
After the current frame is transmitted, the transmit DMA state machine will update the valid status of the current transmitted frame into the last descriptor of the current transmitted frame.
The Transmit Access Control is valid on each descriptor of the current frame. The transmit DMA state machine will release the descriptor by reset the TAC bit when the data pointed by this descriptor is transmitted.

Bit	Symbol	Description
31	TAC	Transmit Access Control : When the TAC bit is set, the current descriptor allows to be accessed by W89C840F, otherwise the W89C840F can not issue any read or write request on this descriptor. When the TAC is reset to low, the driver program is allowed to access this descriptor. This bit will be reset before completing to fill data into the transmit buffer; set if the data in the transmit buffer is available. It is a valid value on each descriptor of the current frame.
15	TE	Transmit Error: It indicates any one of the following events occurs when TE is set to high. T00[1] -- Transmit FIFO underflow T00[8] -- Transmit aborted T00[10] -- No Carrier sense T00[11] -- Carrier sense lost This bit is valid only when the bit TLD (T01[30]) is set, i.e when the current descriptor is the last descriptor of the current frame.
11	CSL	Carrier Sense Lost: When set, it indicates that there is a carrier sense lost during transmission. This bit is valid only when TLD (T01[30]) is set, i.e when the current descriptor is the last descriptor of the current frame. This bit is not valid in internal loopback mode.
10	NCS	No Carrier Sense: When set, it indicates that no carrier sense is presented during transmitting. This bit is valid only when TLD (T01[30]) is set, i.e when the current descriptor is the last descriptor of the current frame. This bit is not valid in internal loopback mode.

9	LC	Late Collision: When set, it indicates that collision occurs after the 64 bytes collision window. This bit is not valid if Transmit FIFO underflow bit(T00[1]) is set. This bit is valid only when TLD (T01[30]) is set, i.e when the current descriptor is the last descriptor of the current frame.
8	TA	Transmit Aborted: When set, it indicates that the transmission was aborted after 16 successive collisions during the transmission. This bit is valid only when TLD (T01[30]) is set, i.e when the current descriptor is the last descriptor of the current frame.
7	SQE	Signal Quality Error Status: When set, it indicates that W89C840F has detected a signal quality error signal in a range of time after the frame was transmitted if the W879C840 is set in 10 Mbps mode. This bit is not valid if Transmit FIFO underflow bit (T00[1]) is set. This bit is valid only when TLD (T01[30]) is set, i.e when the current descriptor is the last descriptor of the current frame.
6:3	CC	Collision Count: The number of collisions occurred before the frame is transmitted. This bit is valid only when TLD (T01[30]) is set, i.e when the current descriptor is the last descriptor of the current frame.
1	TFU	Transmit FIFO Underflow. This bit is set when the transmission process lacks data to transmit during frame transmission. The transmit DMA state machine will enter in suspend state. This bit is valid only when TLD (T01[30]) is set, i.e. when the current descriptor is the last descriptor of the current frame.
0	DEF	Deferred: When set, it indicates that the W89C840F had to defer when ready to transmit a frame because the carrier sense input was asserted before the W89C840F gets the grant to acquire the network media. This bit is valid only when TLD (T01[30]) is set, i.e. when the current descriptor is the last descriptor of the current frame.

T01, Transmit Descriptor 1

The T01 is used to describe the Transmit Control for the current frame transmission
The transmit DMA state machine will fetch the first descriptor of the current frame , at first, to decide the transmission control configuration for the current frame. The transmit DMA state machine will also fetch each descriptor before read the transmitted data from the data buffer in the host memory.

Bit	Symbol	Description
31	FINT	Frame Interupt. The W89C840F will set the Transmit Interrupt bit(bit 0 of C14/CISR) after the current frame was transmitted if the FINT is previously set by the driver program. This bit is valid only when the current descriptor is the first descriptor of the current frame (TFD set).
30	TLD	Last Descriptor. When set, it indicates that this is the last descriptor of the current frame. The TLD is valid on each descriptor.

29	TFD	First Descriptor. When set, it indicates that this is the first descriptor of the current frame. The TFD is valid on each descriptor. When both TFD and TLD are high, it means that the current transmission frame is described by a single descriptor. When both TRFD and TLD are low, it means that the current descriptor is neither the first descriptor nor the last descriptor of the current frame. When TLD is high and TFD is low, it means the current descriptor is the last descriptor. When TLD is low and TFD is high, it means the current descriptor is the first descriptor.
26	ICRC	Inhibit CRC: The W89C840F will inhibit CRC appending after the end of transmitted frame when the ICRC is set by the driver program. Otherwise, the W89C840F appends CRC after the end of transmitted frame when ICRC is reset. This bit is valid only when First Descriptor bit (T01[29]) is set.
25	TLAST	Last Descriptor of the Ring. When set, it indicates the current descriptor is the last one of the descriptor ring. This bit preempts bit 24 (TLINK). It means that the next descriptor pointer of the transmit DMA state machine will automatically jump to the first descriptor pointed by register C10/CTDLA even the TLINK is set to high and the T03 points to an address other than the one specified by the C10/CTDLA. The TLAST is valid on each decsriptor.
24	TLINK	Link Address in Transmit Buffer Address 2 When set, it indicates that Transmit Buffer Address 2(T03) contains the start address of the next descriptor of the descriptor list. Otherwise the T03 is used to point to the start address of the transmit buffer 2 when the TLINK is reset. The TLINK is valid on each descriptor.
23	PD	Padding Disable: The W89C840F does not add the padding data on a frame shorter than 64 bytes when the PD bit is set to high. However, the W89C840F will automatically add a padding data on a frame shorter than 64 bytes when the PD bit is reset to low. The four bytes of CRC will be appended at the end of the padding field of the transmitted frame no matter what the ICRC is set or reset if the PD is reset. The total transmited frame data length will be 68 bytes if the data in the current frame is less than 64 bytes and the PD is reset. This bit is valid only when TFD (T01[29]) is set.
21:11	TSZ2	Transmit Buffer 2 Size: The TSZ2 indicates the size, in bytes, of the second data buffer pointed by the current transmit descriptor. If this field is 0, the W89C840F will ignore this buffer. The TSZ2 value is valid on each descriptor.

10:0	TSZ1	Transmit Buffer 1 Size: The TSZ1 Indicates the size, in bytes, of the first data buffer pointed by the current transmit descriptor. If this field is 0, the W89C840F will ignore this buffer. The TSZ1 value is valid on each descriptor.

T02, Transmit Descriptor 2

The T02 is used to specify the start address of the transmit buffer 1

Bit	Symbol	Description
31:0	TBA1	Transmit Buffer Address 1 The TBA1 indicates the physical address, in the system memory space, of the first transmit buffer pointed by the current descriptor. The TBA1 allow to be programmed with any value by the driver program. It is valid on each descriptor of the current frame.

T03, Transmit Descriptor 3

The T03 is used to specify the start address of the transmit buffer 2

Bit	Symbol	Description
31:0	TBA2	Transmit Buffer Address 2 The TBA2 indicates the physical address, in the system memory space, of the second transmit buffer pointed by the current descriptor. The TBA2 allow to be programmed with any value by the driver program. It is valid on each descriptor of the current frame.

$.Electrical Characteristics

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
TA	Operating Temperature	0	70	°C
TS	Storage Temperature	-55	150	°C
V_{DD}	Supply Voltage	-0.5	7.0	V
V_{IN}	Input Voltage	V_{SS}-0.5	V_{DD}+0.5	V
V_{OUT}	Output Voltage	V_{SS}-0.5	V_{DD}+0.5	V
TL	Lead Temperature (Soldering 10 seconds maximum)		250	°C

Power Supply (TA = 0 °C to 70 °C)

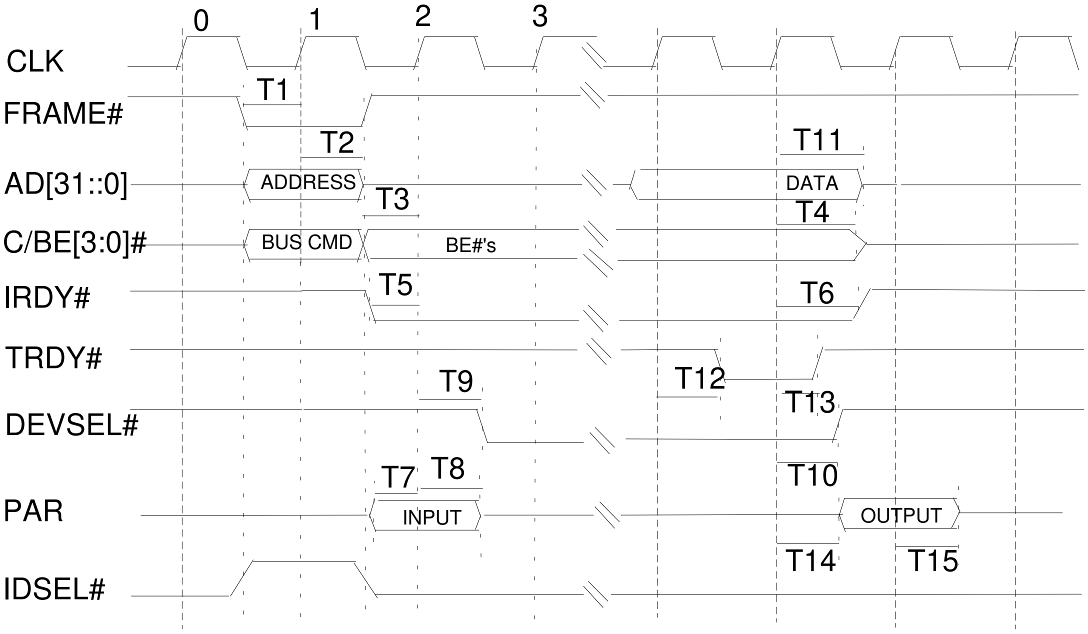
Symbol	Parameter	Condition	Maximum	Unit
IDDI	Power Supply Current (idle, clock active only)	Vdd=5.25V	150	mA
IDDT	Power Supply Current (transmitting)	Vdd=5.25V	250	mA

DC Characteristics (V_{DD}=4.75 V to 5.25V, V_{SS}=0 V,TA = 0 °C to 70 °C)

Symbol	Parameter	Condition	Maximum	Unit
V_{IL}	Input Low Voltage		0.8	V
V_{IH}	Input High Voltage		V_{DD}+0.5	V
V_{OL}	Output Low Voltage	IoL=4.0mA	0.4	V
V_{OH}	Output High Voltage	Ioh=-4.0mA		V
I_{IL1}	Input Leakage Current	Vin=5.25V	10	µA
I_{OL}	Tristate leakage Current	Vout=Vdd	10	µA

AC Characteristics (V$_{DD}$=4.75 V to 5.25V, V$_{SS}$=0 V,TA = 0 °C to 70 °C)

PCI Slave Read Transaction

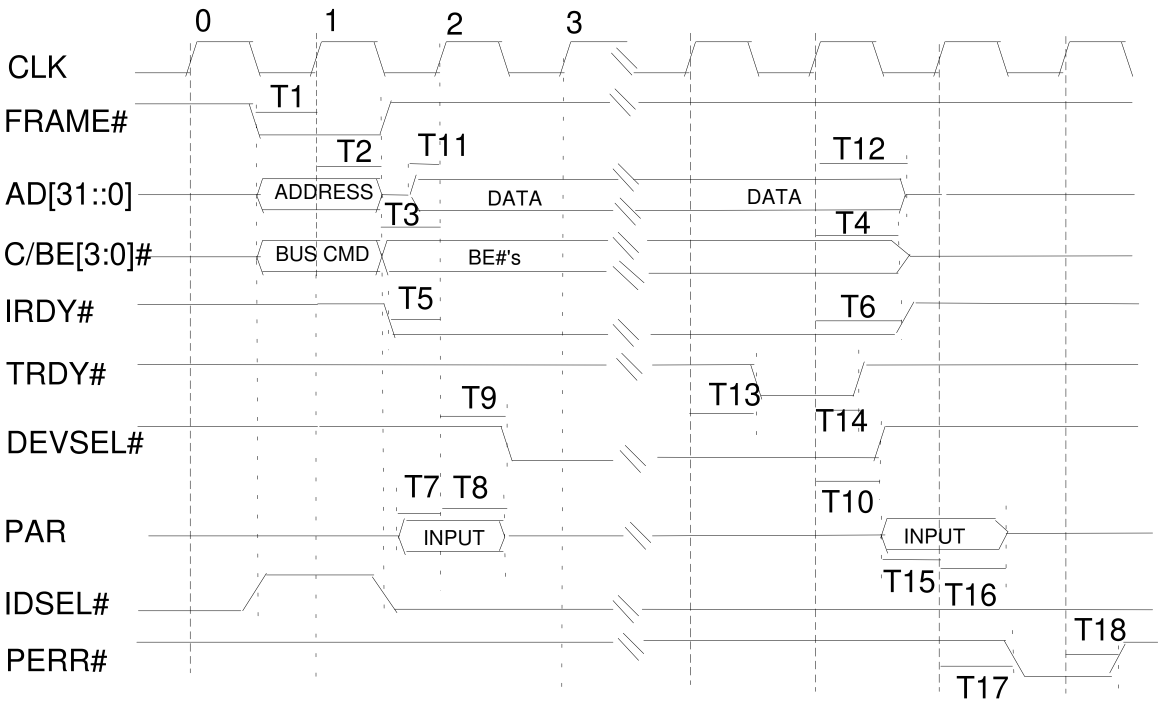


Symbol	Description	Min	Typical	Max	Unit
T1	PCI input signal set up time*	7			nsec
T2	PCI input signal hold time*	0			nsec
T3	BE Byte Enable set up time	7			nsec
T4	BE Byte Enable hold time	0			nsec
T5	IRDY# set up time	7			nsec
T6	IRDY# hold time	0			nsec
T7	PAR input setup time	7			nsec
T8	PAR input hold time	0			nsec
T9	DEVSEL# driven time	11	12	13	nsec
T10	DEVSEL# hold time	11	12	13	nsec
T11	output data hold time	18	19	20	nsec
T12	TRDY# driven time	11	12	13	nsec
T13	TRDY# hold time	11	12	13	nsec
T14	PAR output driven time	11	12	13	nsec
T15	PAR output hold time	11	12	13	nsec

Note: address, command, and FRAME# for slave access, IDSEL# for configuration read transaction

AC Characteristics (V$_{DD}$=4.75 V to 5.25V, V$_{SS}$=0 V,TA = 0 °C to 70 °C)

PCI Slave Write Transaction



Symbol	Description	Min	Typical	Max	Unit
T1	PCI input signal setup time*	7			nsec
T2	PCI input signal hold time*	0			nsec
T3	BE Byte Enable set up time	7			nsec
T4	BE Byte Enable hold time	0			nsec
T5	IRDY# set up time	7			nsec
T6	IRDY# hold time	0			nsec
T7	PAR input setup time	7			nsec
T8	PAR input hold time	0			nsec
T9	DEVSEL# driven time	11	12	13	nsec
T10	DEVSEL# hold time	11	12	13	nsec
T11	input data set up time	7			nsec
T12	input data hold time	0			nsec
T13	TRDY# driven time	11	12	13	nsec
T14	TRDY# hold time	11	12	13	nsec
T15	PAR input setup time	7			nsec
T16	PAR input hold time	0			nsec
T17	PERR# driven time**	11	12	13	nsec
T18	PERR# hold time**	11	12	13	nsec

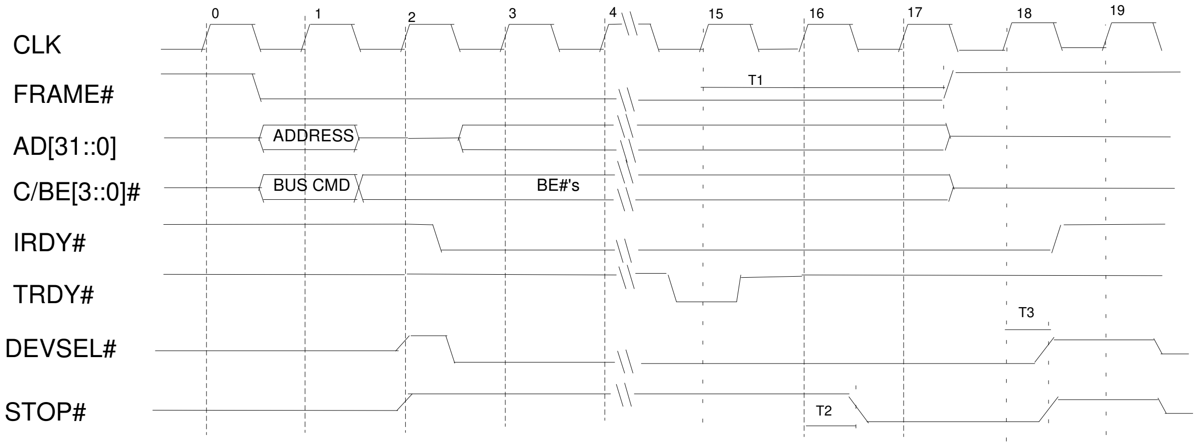
Note: address, command, and FRAME# for slave access, IDSEL# for configuration read transaction

**PERR# will be asserted if the parity error event occurred.

AC Characteristics (V_{DD}=4.75 V to 5.25V, V_{SS}=0 V,TA = 0 °C to 70 °C)

PCI Transaction Termination

Disconnect-C/Retry Type:

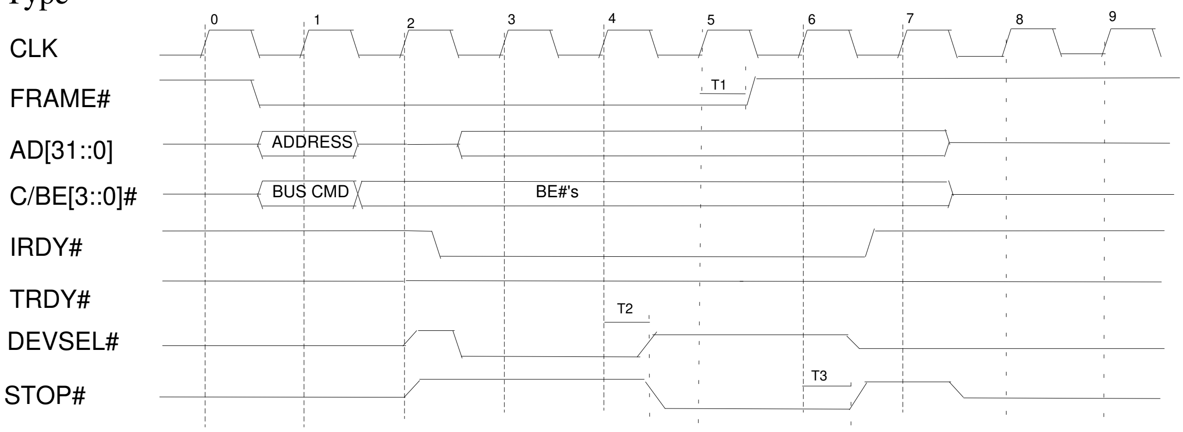


Symbol	Description	Min	Typical	Max	Unit
T1	FRAME# deasserted from clock 15	0			nsec
T2	Clock 16 to STOP# asserted time	11	12	13	nsec
T3	Clock 18 to STOP# and DEVSEL# hold time	11	12	13	nsec

Note: 1) The other timing requirements for PCI input signal are as the read transaction timing.

2) T1,T2 and T3 are used for the disconnect type C(host try to transfer more than one data phase).

Target-Abort Type



SYMBOL	DESCRIPTION	Min	typical	MAX	UNIT
T1	FRAME# deasserted from clock 15	0			nsec
T2	Clock 4 to DEVSEL# hold time	11	12	13	nsec
T3	Clock 6 to STOP# hold time	11	12	13	nsec

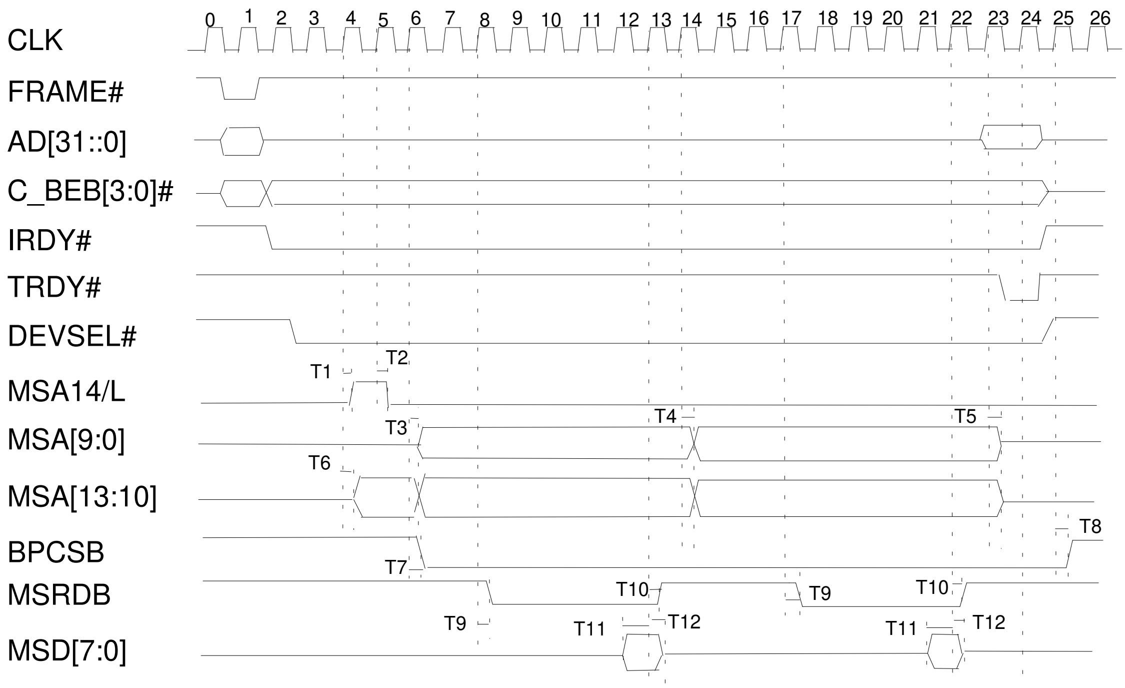
Note: 1) The other timing requirements for PCI input signal are as the read transaction timing..

2) T2 and T3 are used for the target abort type(host addressing error).

AC Characteristics (V$_{DD}$=4.75 V to 5.25V, V$_{SS}$=0 V,TA = 0 °C to 70 °C)

32KX8-220 BPROM/ FLASH MEMORY

Read cycle



SYMBOL	DESCRIPTION	Min	typical	MAX	UNIT
T1	clock 4 to MSA14/L valid	8	13	18	nsec
T2	clock 5 to MSA14/L deasserted time	8	13	18	nsec
T3	clock 6 to MSA bus valid	8	13	18	nsec
T4	clock 14 to MSA bus valid	8	13	18	nsec
T5	clock 23 to MSA deasserted	8	13	18	nsec
T6	clock 4 to MSA high nibble valid	8	13	18	nsec
T7	clock 6 to BPCSB valid	15	20	25	nsec
T8	clock 25 to BPCSB deasserted	7	12	17	nsec
T9	clock 8/ clock 17 to MSRDB asserted time	15	20	25	nsec
T10	clock 13/ clock 22 to MSRDB deasserted time	8	13	18	nsec

T11	MSD setup time from clock 13	7			nsec
T12	MSD hold time from clock 15	0			nsec

Note: 1) The other timing requirements for PCI signal are as the read transaction timing.

2) BPROM/FLASH memory access could be byte, word or double word access. The timing is the same.

AC Characteristics (V$_{DD}$=4.75 V to 5.25V, V$_{SS}$=0 V,TA = 0 °C to 70 °C)

Serial EEPROM Timing

SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
T1	EECS asserted to SK	500		nS
T2	EECS hold from SK	0	500	nS
T3	MSD2 OFF time	500	600	nS
T4	MSD2 ON time	500	600	nS
T5	MSD2 clock period	1	1.2	µS
T6	MSD1 set up time to MSD2 high	500	600	nS
T7	MSD1 hold time from MSD2 high	500	600	nS
T8	MSD0 valid from MSD2 high		300	nS

BootROM/Flash Interface

Read Cycle Timing (Byte mode)

SYMBOL	DESCRIPTION	MIN.	MAX	UNIT
TRC	Read Cycle Time	210	-	nS
TACS	Address valid to CS# asserted	0	5	nS
TCES	CE# valid to Data valid	-	210	nS
TCEH	Data hold from CE# deasserted	0	-	nS
TDLES	Data valid to LE enable	10	-	µS
TDLEH	LE enable high time	20	-	nS

Read Cycle Timing (Double Word mode)

Symbol	Parameters	MIN,	MAX.	Unit
TRC	Read Cycle Time	210	-	nS
TACS	Address valid to CS# asserted	0	5	nS
TCES	CE# valid to data valid	-	210	ns
TAD	Address valid to data Valid	-	210	ns
TDH	Data hold from address deasserted	0	-	ns

TCEH	Data hold from CE# deasserted	0	-	ns
TDLES	Data valid to LE enable	10	-	ns
TDLEH	LE enable high time	20	-	ns

Write Cycle Timing (Byte mode)

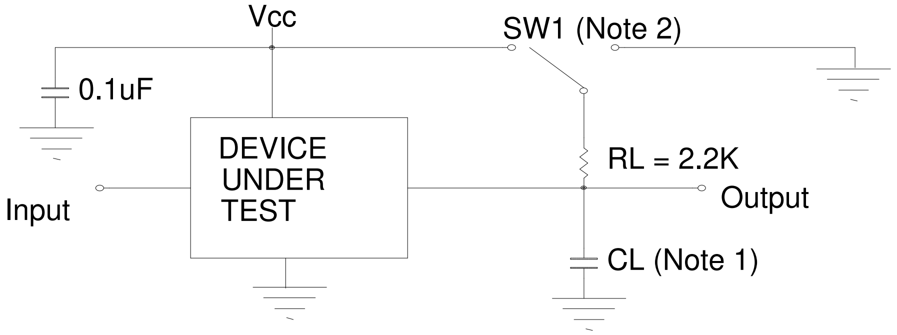
Symbol	Parameters	MIN,	MAX.	Unit
TDS	Data valid to BtCSB deasserted	55	-	ns
TDH	Data hold from BtCSB deasserted	10	-	ns
TWC	Write Cycle Time	130	-	ns
TWS	Address valid to BtCSB asserted	0	-	ns
TWP	BtCSB asserted width	95	-	ns
TWPH	BtCSB keep high from BtCSB deasserted	155	-	ns
TDLES	Data valid to LE enable	10	-	ns
TDLEH	LE enable high time	20	-	ns

$. Test Load

AC Timing Test Conditions

PARAMETER	TEST CONDITION
Supply voltage (V_{DD}/V_{SS})	5V±5%
Temperature	25°C/70°C
Input Test Pattern Levels (TTL/CMOS)	GND to 4.0V
Input Rise and Fall Times (TTL/CMOS)	5nS
Input and Output Pattern Reference Level (TTL/CMOS)	1.5V
Tristate Reference Levels	Float (V) + 0.5V

Output Load



Note 1: Load capacitance employed on output is 50 pF.

Note 2:

SW1=Open for push pull outputs during timing test.

SW1=VCC for VOL test.

SW1=GND for VOH test.

SW1=VCC for High-Z to active low and active low to High-Z measurements.

SW1=GND for High-Z to active high and active high to High-Z measurements.

Pin Capacitance

TA = 25°C f = 1 MHz

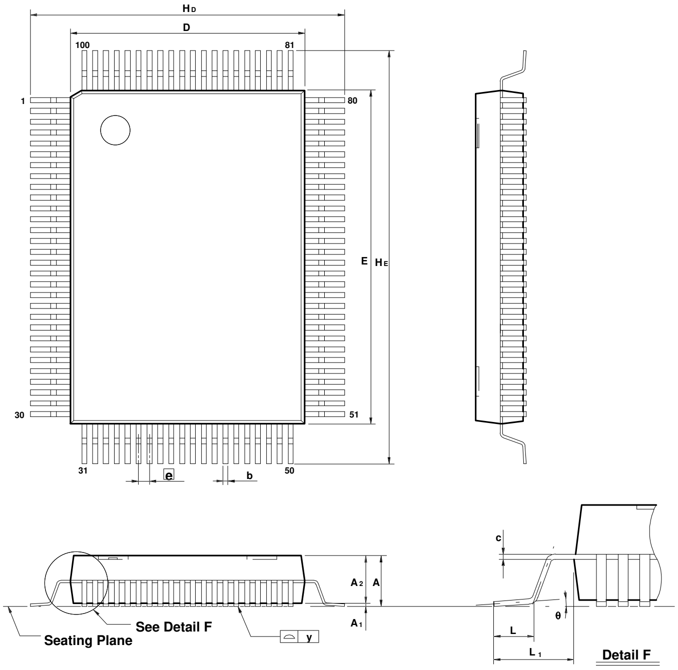
SYMBOL	PARAMETER	TYP	UNIT
C_{IN}	Input Capacitance	7	pF
C_{OUT}	Output Capacitance	10	pF

Derating Factor

Output timing is measured with a purely capacitive load of 50pF.

The correction factor when CL>50pF is +0,4 ns/pF.

$. Package Dimension



Symbol	Dimension in inches			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.130	—	—	3.30
A_1	0.004	—	—	0.10	—	—
A_2	0.107	0.112	0.117	2.718	2.845	2.972
b	0.010	0.012	0.016	0.254	0.305	0.407
c	0.004	0.006	0.010	0.101	0.152	0.254
D	0.546	0.551	0.556	13.87	14.00	14.13
E	0.782	0.787	0.792	19.87	20.00	20.13
e	0.020	0.026	0.032	0.498	0.65	0.802
H_D	0.728	0.740	0.752	18.49	18.80	19.10
H_E	0.964	0.976	0.988	24.49	24.80	25.10
L	0.039	0.047	0.055	0.991	1.194	1.397
L_1	0.087	0.095	0.103	2.21	2.413	2.616
y	—	—	0.004	—	—	0.102
θ	0°	—	12°	0°	—	12°

Notes:

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeters
4. General appearance spec. should be based on final visual inspection spec.